Design of CMOS Low-Noise Amplifiers

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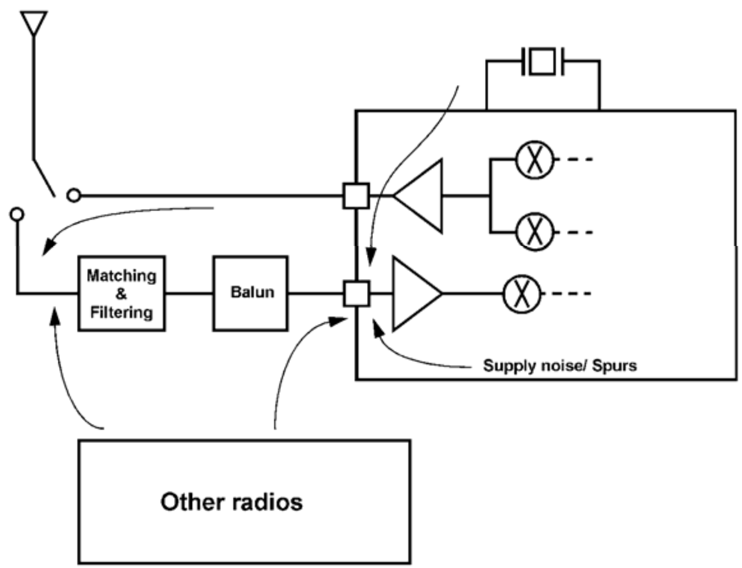
Outline

- Introduction
- Narrowband vs. Broadband Amplifiers
- Stability
- Practical LNA Implementations
- Layout Considerations
- Special Topics
  - Noise Cancellation Techniques
  - ESD protection
- Conclusions

LNA Design Constraints

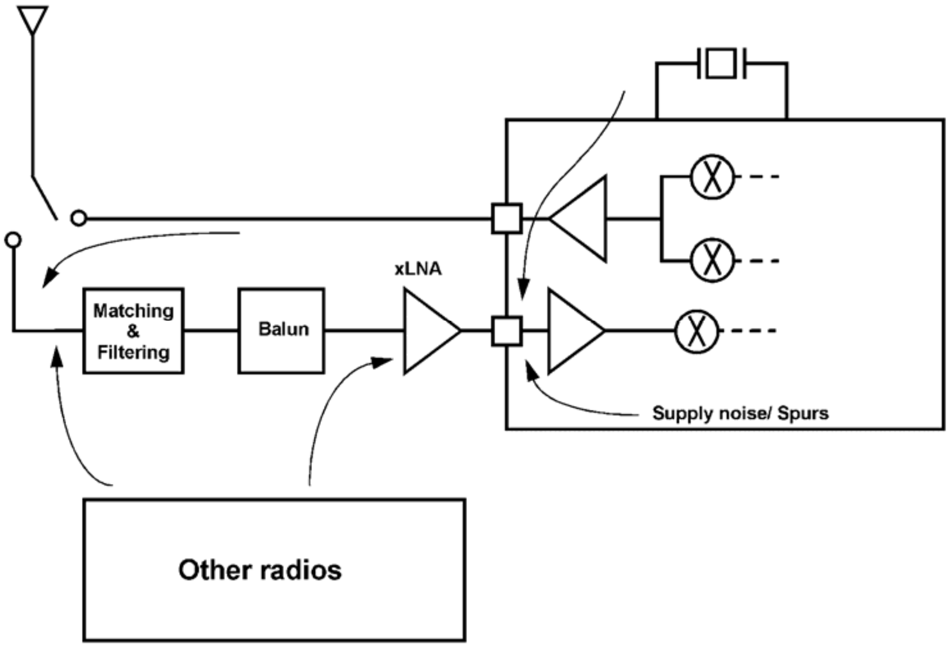
- Noise Figure
  - Sufficient gain
  - Degradation in Signal-to-Noise ratios as the signal passes through the receive chain
- Matching
- Ability to accommodate large blockers
  - High linearity and dynamic range
  - Large common-mode rejection
- Gain Control
  - LNA is part of the receiver ARC algorithm
- Stability
- Power Dissipation

Low-Noise Amplifier Design Constraints



- As the entry point to the receiver chain, LNA inputs are quite susceptible to interference
- Interference can be
  - In-band/image signals from other radios
  - Clock harmonics
  - Supply noise
- Some external filtering is necessary in any practical application
  - Loss!

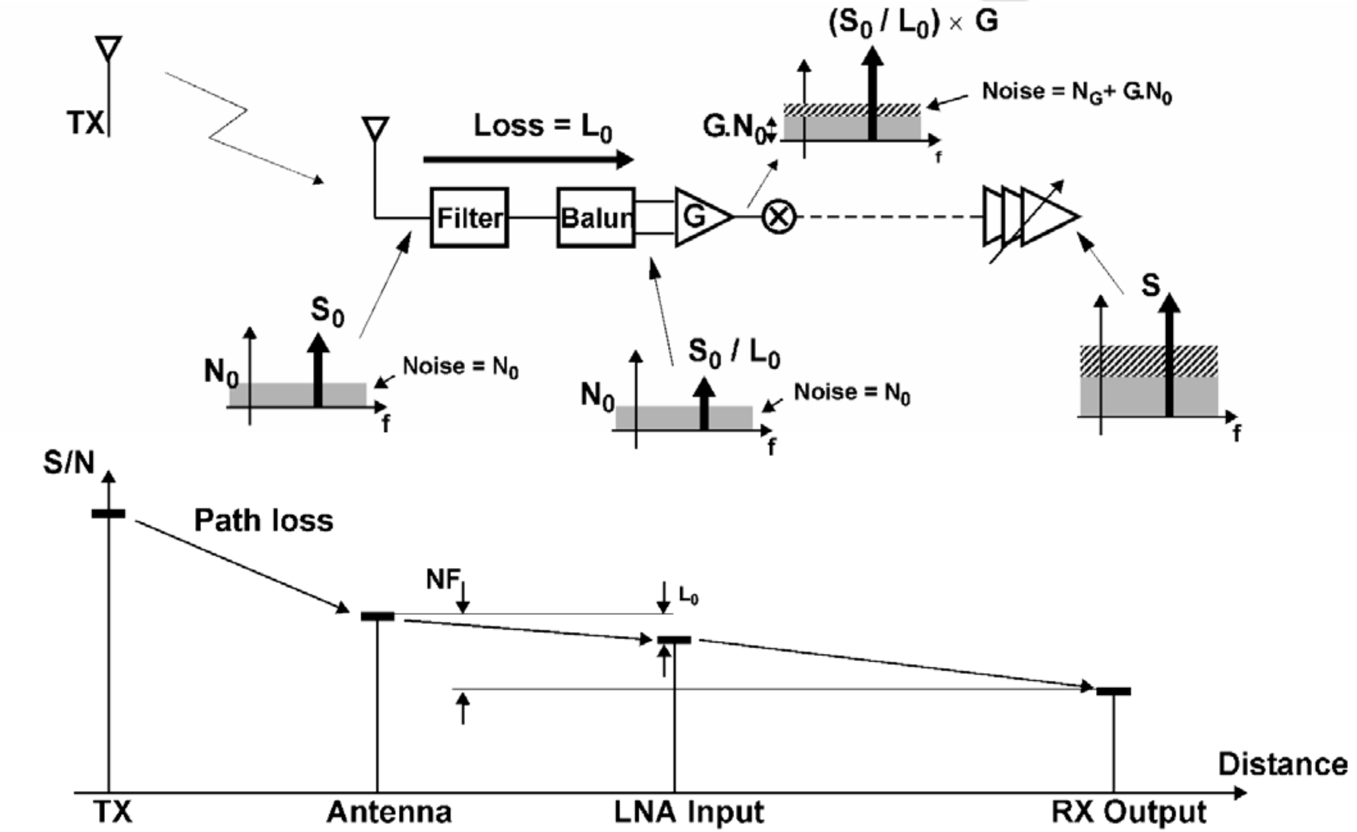
Low-Noise Amplifier Design Constraints



The use of external LNA may be required in order to

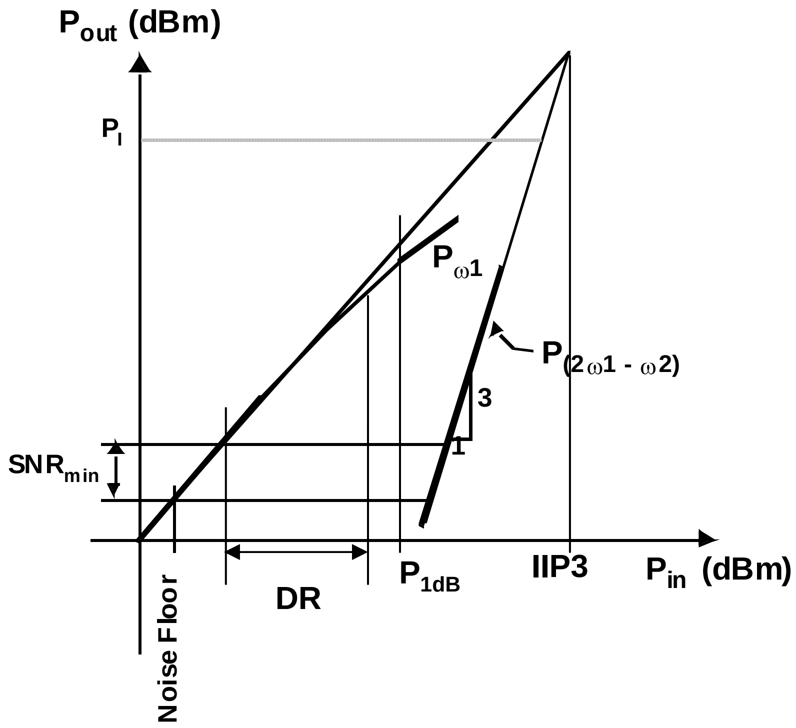
- Overcome any external loss due to filtering, etc.
- Increase the signal level relative to spurs

Link Budget



TX
Loss = L$_0$
Filter
Balun
G
(S$_0$ / L$_0$) × G
Noise = N$_G$+ G.N$_0$
G.N$_0$
f
S$_0$
N$_0$
Noise = N$_0$
f
S$_0$ / L$_0$
N$_0$
Noise = N$_0$
f
S
f
S/N
Path loss
NF
L$_0$
Distance
TX
Antenna
LNA Input
RX Output

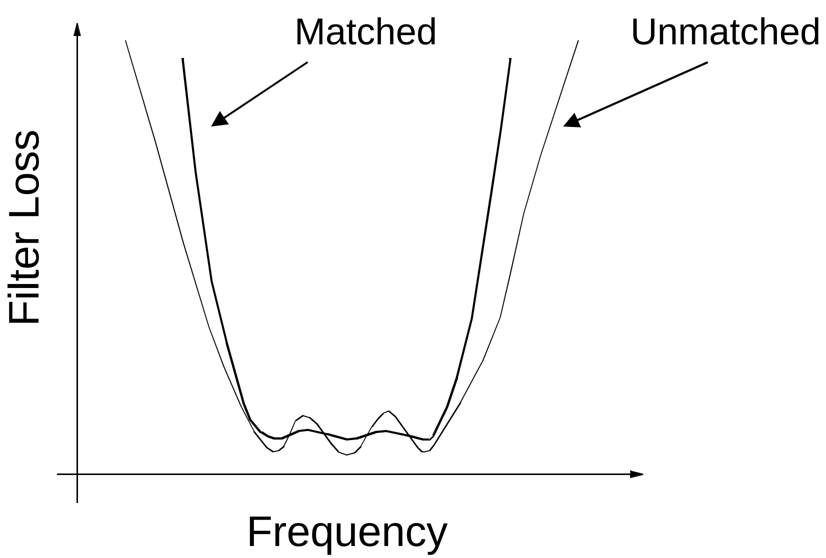
Dynamic Range



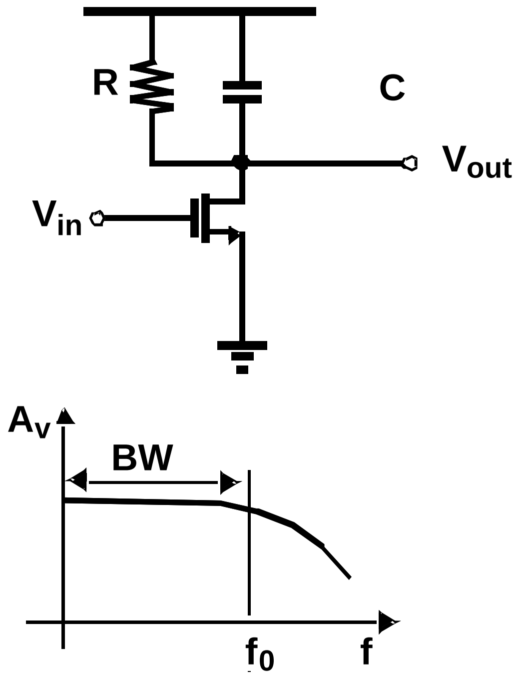
Matching

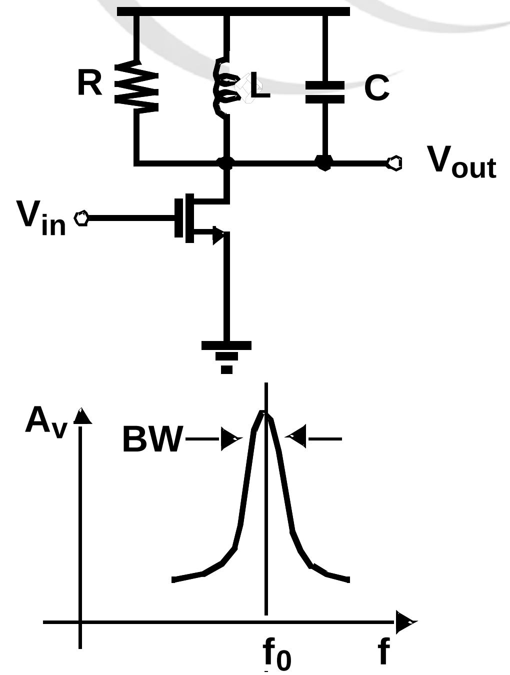
Matching is needed at the LNA input because

- To transfer max power from the source to the receiver (power matching)
- To optimize noise figure (noise matching)
- Antenna, external filters, etc. all require 50Ω termination
- Improper termination results in
  - Large bandpass ripple
  - Poor transition band



Narrowband vs. Broadband Design





$$\text{Gain . BW} = (g_m.R) \cdot \left(\frac{1}{R.C}\right) = \frac{g_m}{C}$$

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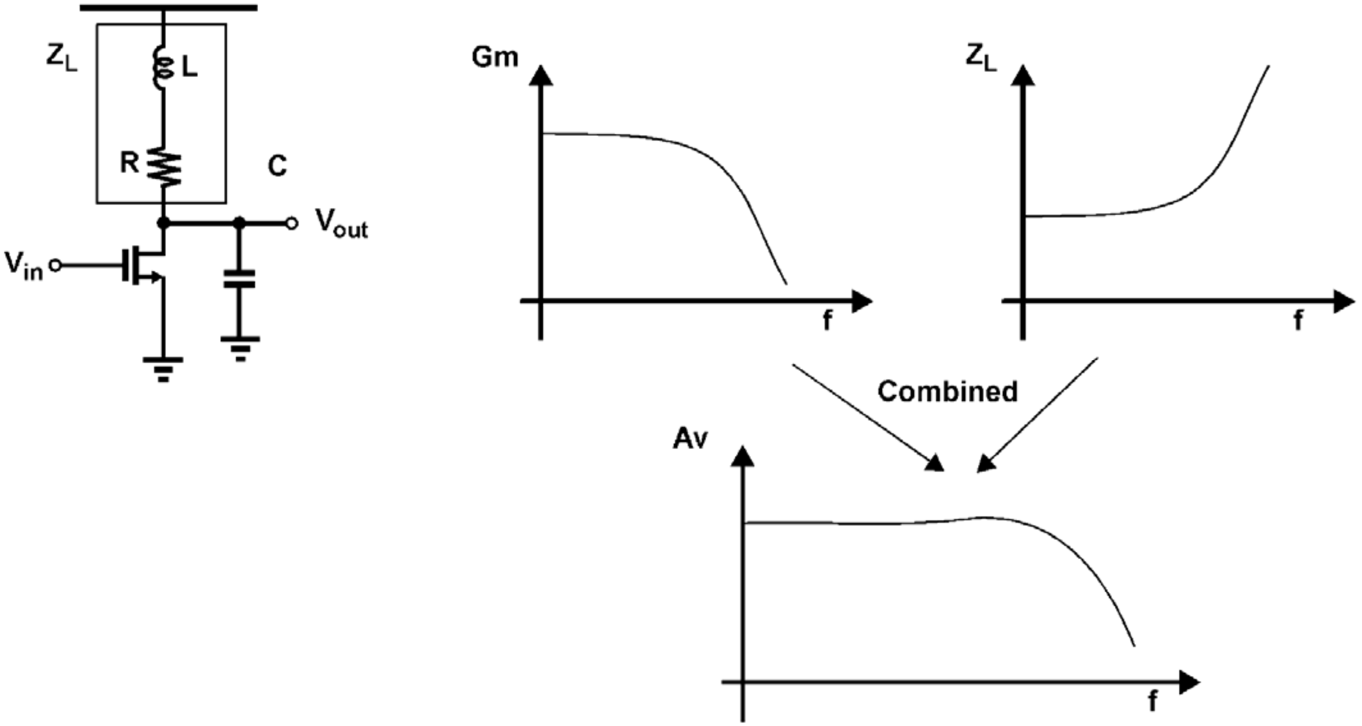
Using inductors at the output will bias the drain at Vdd and improve the amplifier headroom

- Better IIP3 and linearity

BUT:

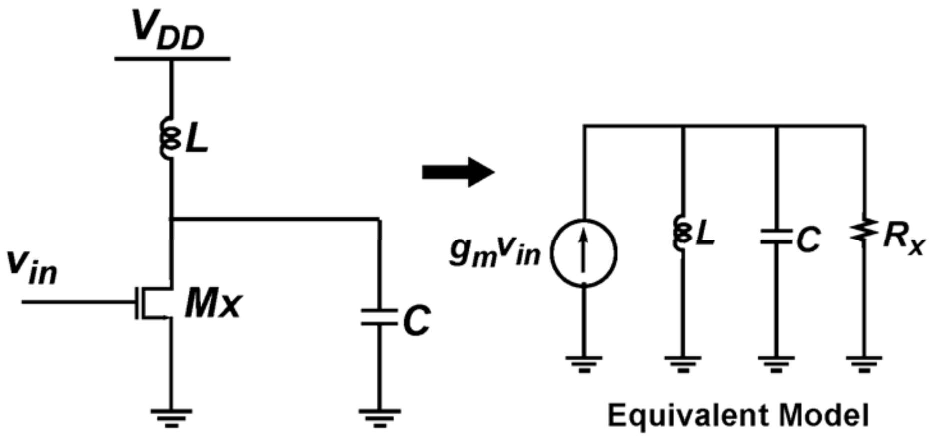
  - larger area due to on-chip inductors
  - Watch for device over-stress

Broadband Design -- Shunt Peaking



- At high frequencies compensate for the drop in g_m by increasing Z_L

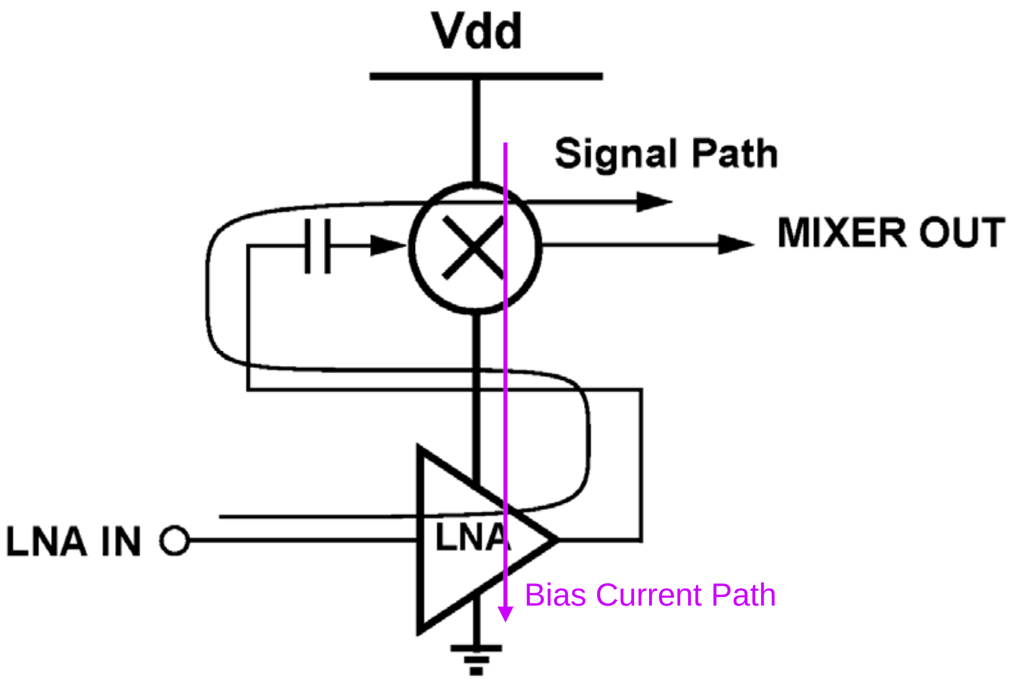
Typical Tuned RF Stage



$$g_m R_X \approx \left[\frac{2I_D}{V_{GS}-V_T}\right]\frac{Q}{\omega_o C} = \left[\frac{2I_D}{V_{GS}-V_T}\right] Q\omega_o L$$

- Power consumption in an RF amplifier is a function of the desired gain, transistor transconductance and the Q of passive elements
- Scaled CMOS processes have less on-chip parasitic capacitances which translates to higher equivalent load impedance

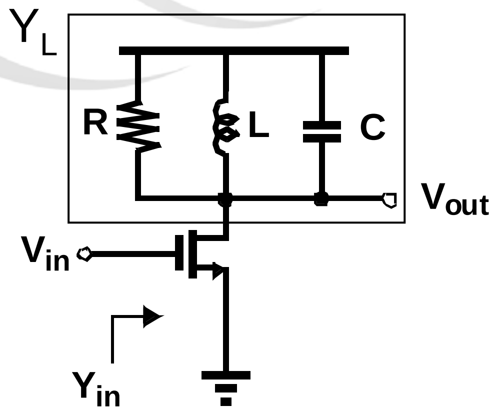
Power Savings: LNA Current Re-use



Zolfaghari et al, JSSC Feb 2003 (UCLA)

Stability

- Decent gain and headroom
- Problem is stability

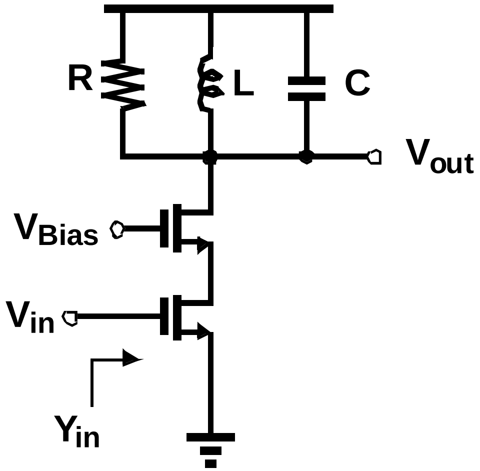


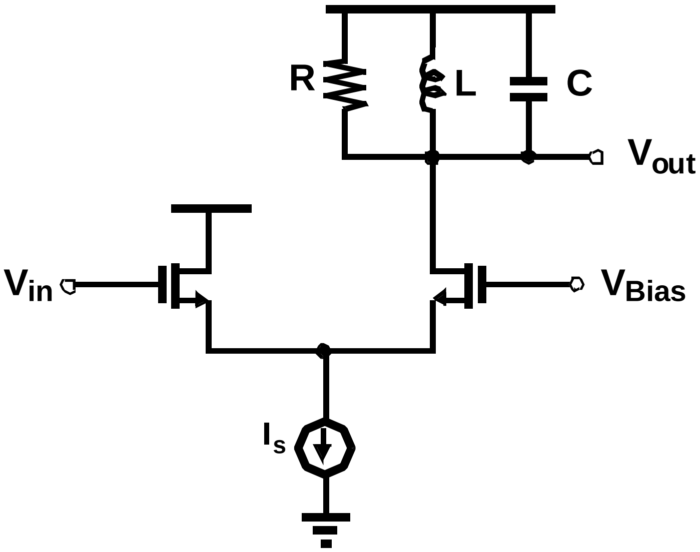
$$Y_{in} = Y_s + Y_{11} - Y_{12}Y_{21} / Y_T$$

$$Y_{in} = j\omega C_{gd} + g_m j\omega C_{gd} / Y_L$$

- This equation suggests that if the last term in Yin has a large enough negative real part, then over some range of frequencies, Yin may have a negative real part and the circuit may oscillate
- To avoid oscillation:
  - Reduce Y12: always desirable: cascoding, neutralization
  - Increase the real part of Ys and YL: trading gain for stability

Stability





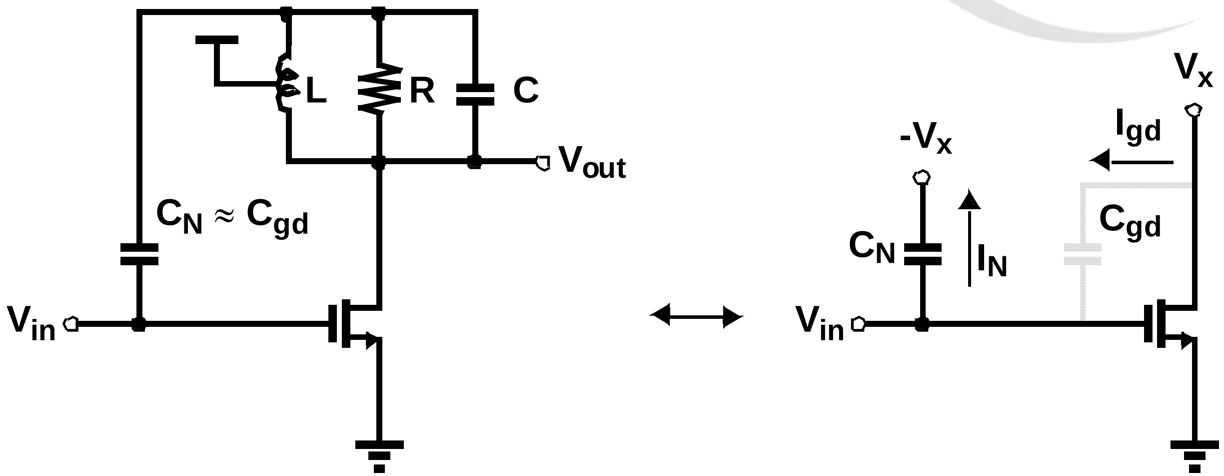
Cascode structure:

By providing isolation between the input and output nodes of the amplifier, the Miller effect of Cdg and its associated instability problems can be eliminate

Source-coupled amplifier:

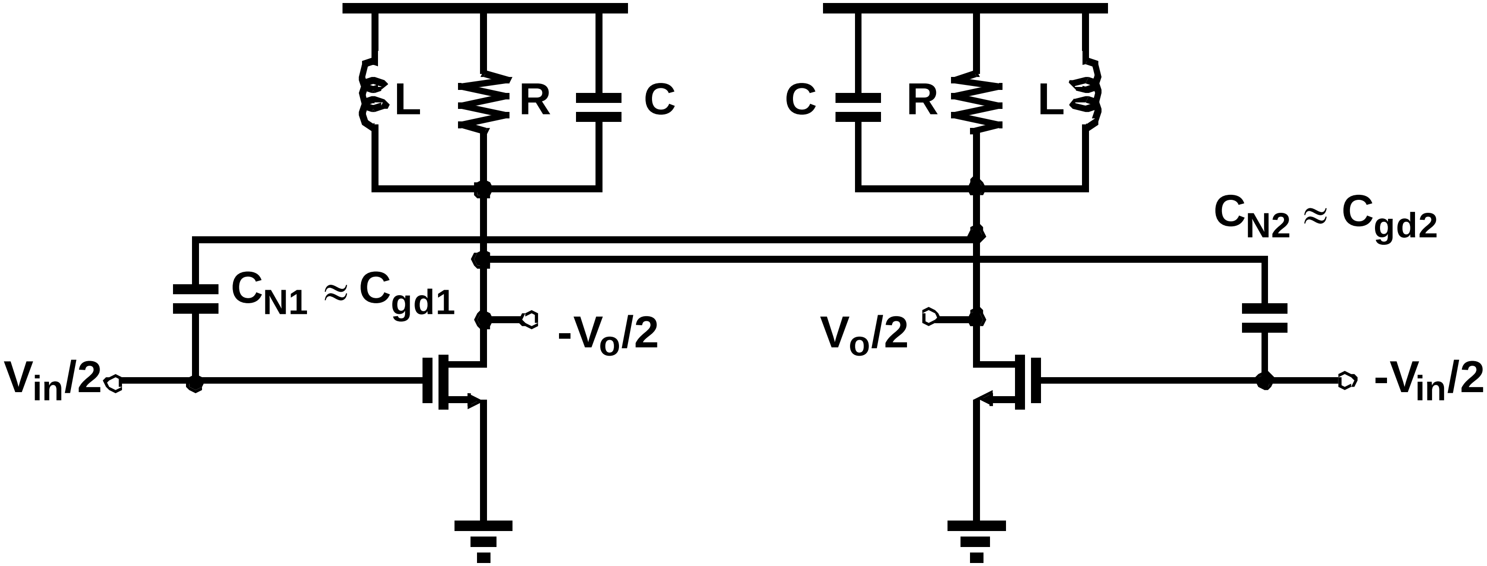
Reduces Y12 by further isolating input and outputs

Stability -- Neutralization



- If $C_N = C_{gd}$, then $I_N = I_{gd}$ and the net feedback current will be zero
- Problems:
  - matching C_N to C_{gd} over a wide frequency range is difficult. Neutralization is primarily considered a narrowband technique
  - Even harder to match the capacitors over process and Temp

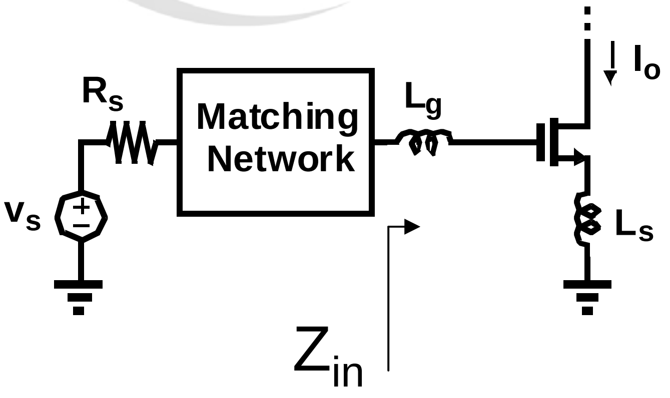
Neutralization – Differential Implementation



Common-Source (CS) LNA

- Simple small-signal model predicts Zin to be:

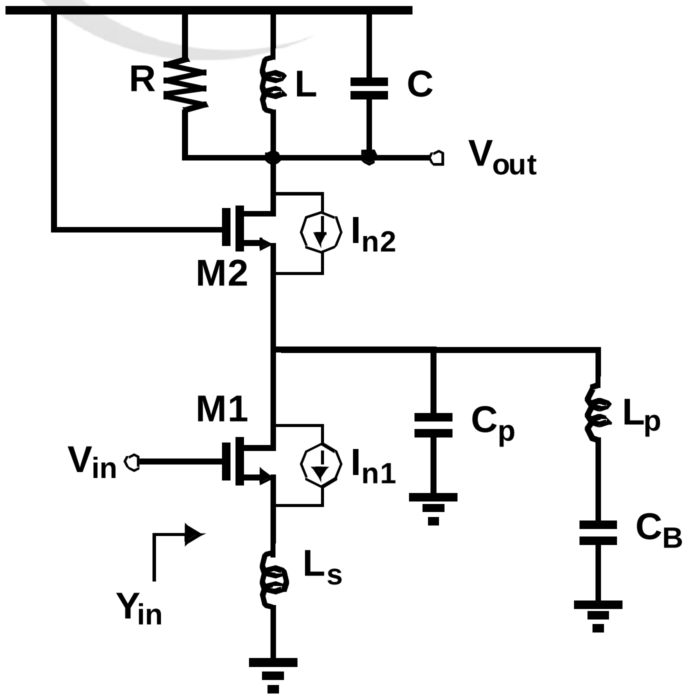
$$Z_{in} = g_m L_s / C_{gs} + j\omega L_s + 1 / j\omega C_{gs}$$



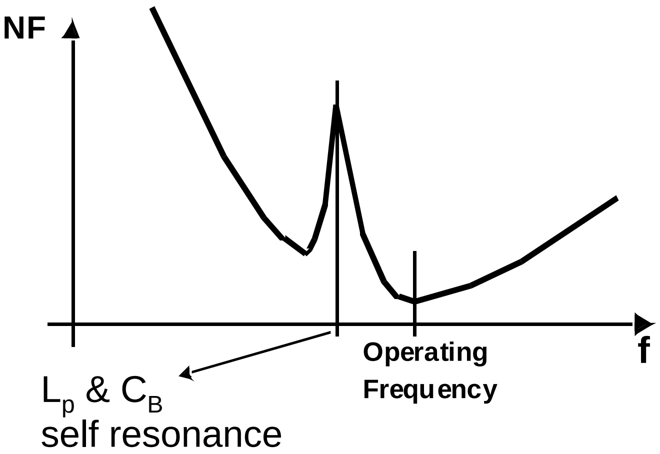
- At resonance frequency, Z_{in} has a real part that can be matched to the source impedance through the matching network
- Ls can be an on-chip Spiral or the package wirebond
- Noise Figure can be optimized by
  - proper sizing of the CS device
  - minimizing gate & substrate resistance through careful layout techniques

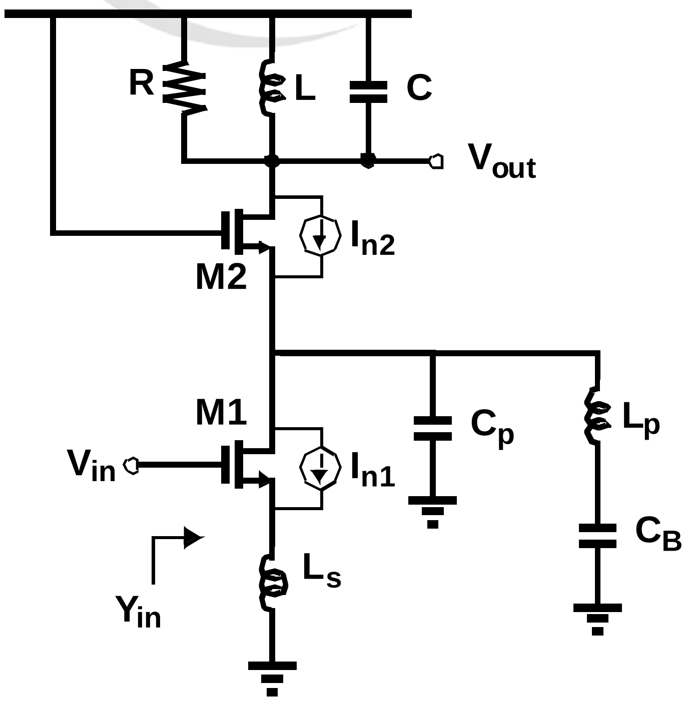
Practical CS LNAs

- In practice cascoding must be used to ensure stability
- The noise contribution of the cascode device will be insignificant only if C_p is small
- In practice C_p can be quite large due to multi-finger nature of the transistor layout
  - Can degrade NF by a few dB if ignored
- C_p can be tuned out using L_p and the dc blocking cap C_B



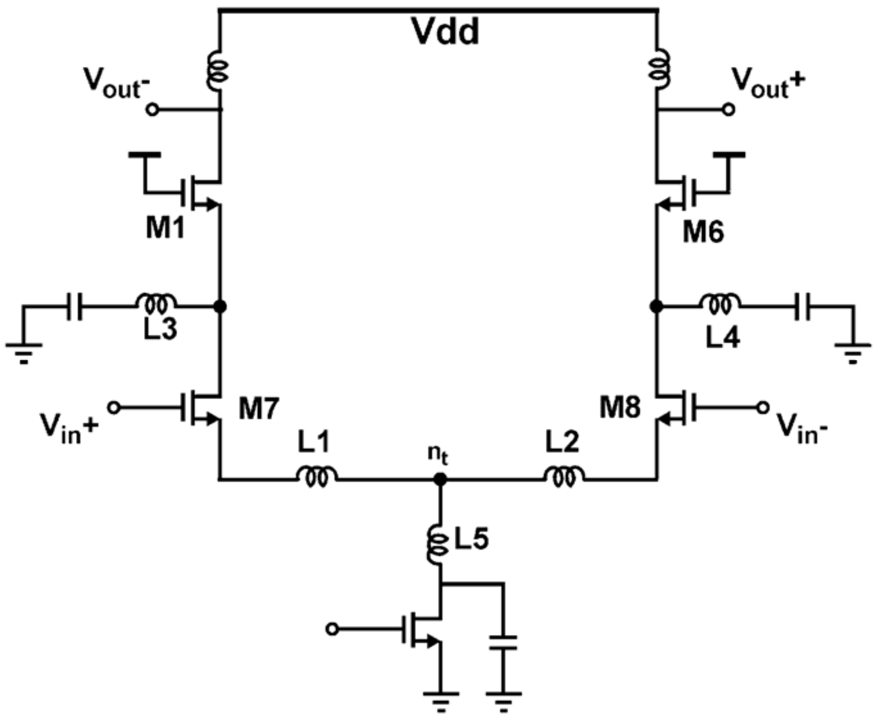
Practical CS LNAs -- *Continued*





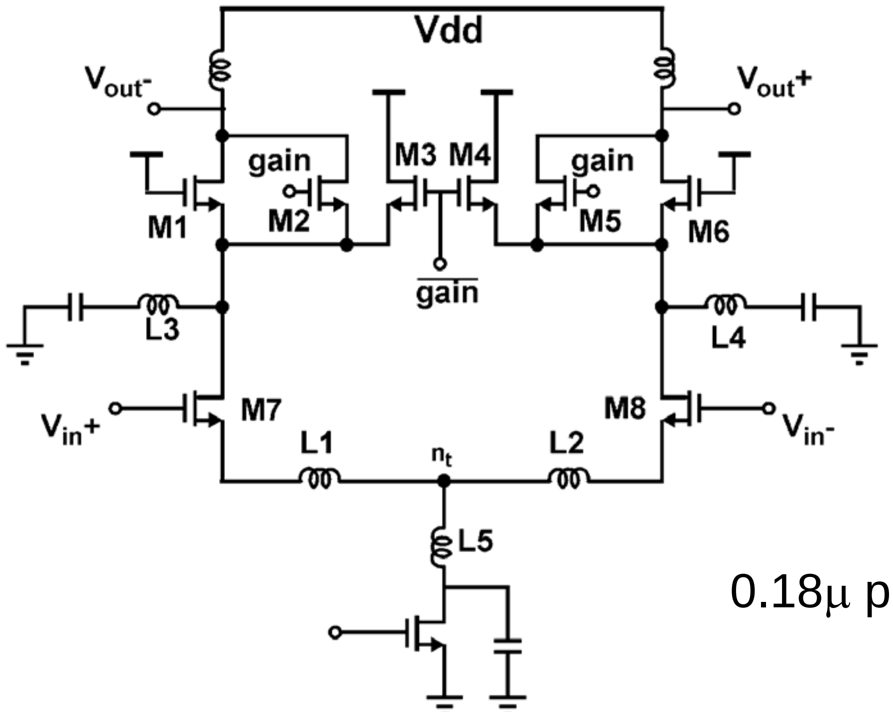
- CB needs to be sufficiently large so that the series resonance of Lp & C_B won't degrade the NF

Differential CS LNA



- L1 and L2 to help matching to 50Ω
- L3 and L4 to reduce cascode node contribution
- L5 to improve the common-mode rejection of the LNA by tuning out the parasitic capacitance at the tail node

Differential CS LNA with gain control

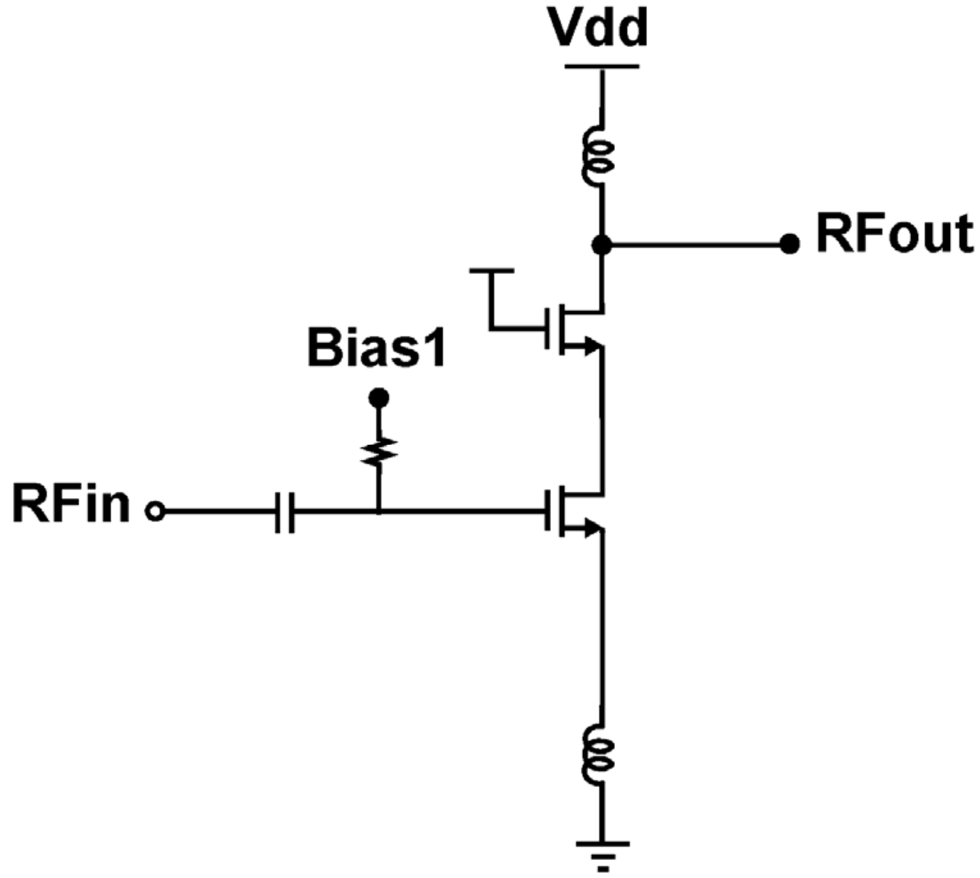


0.18μ process

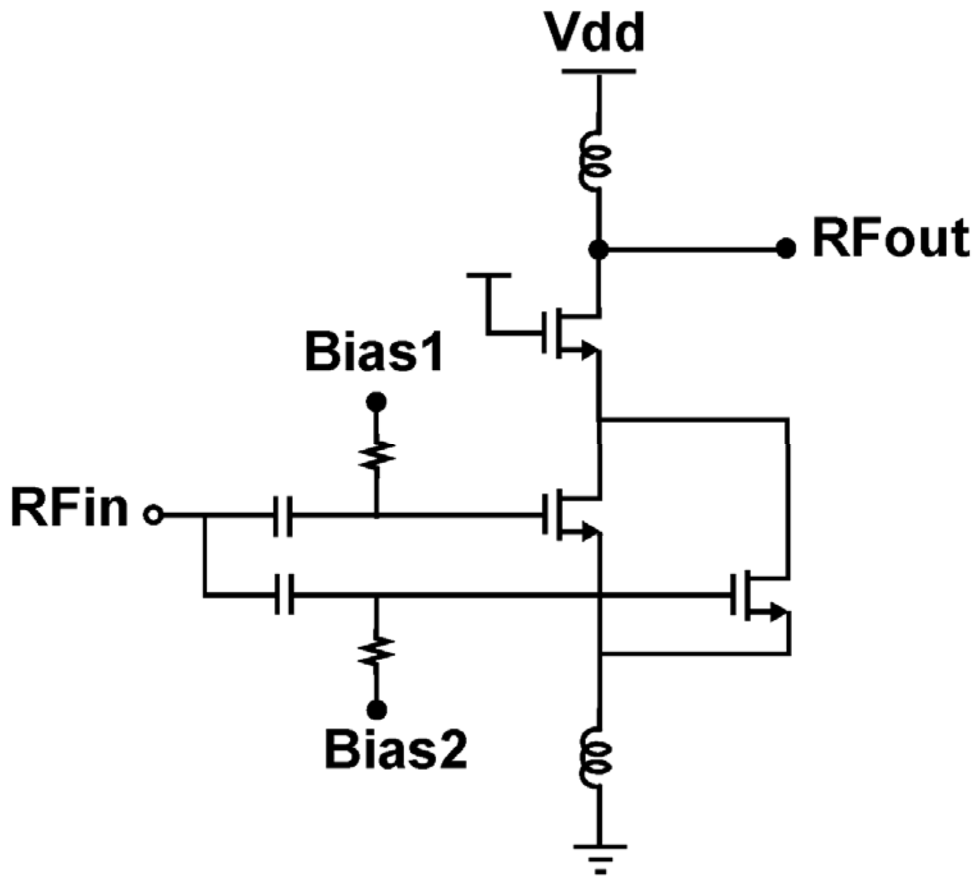
Overall Receiver NF = 4.5/5.5dB @ 2.4/5GHz

- At large inputs M3 and M4 will shunt part of the drain signal, thereby reducing the amplifier gain and avoiding signal compression

Gm Linearization



Gm linearization



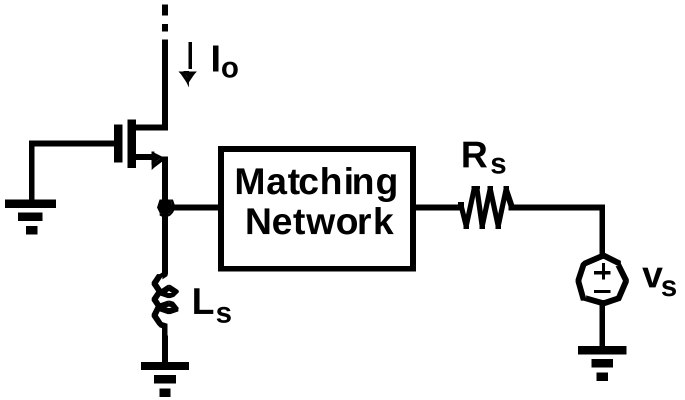
Kim et al, JSSC Jan 2004 (KAIST)

Common-Gate (CG) LNA

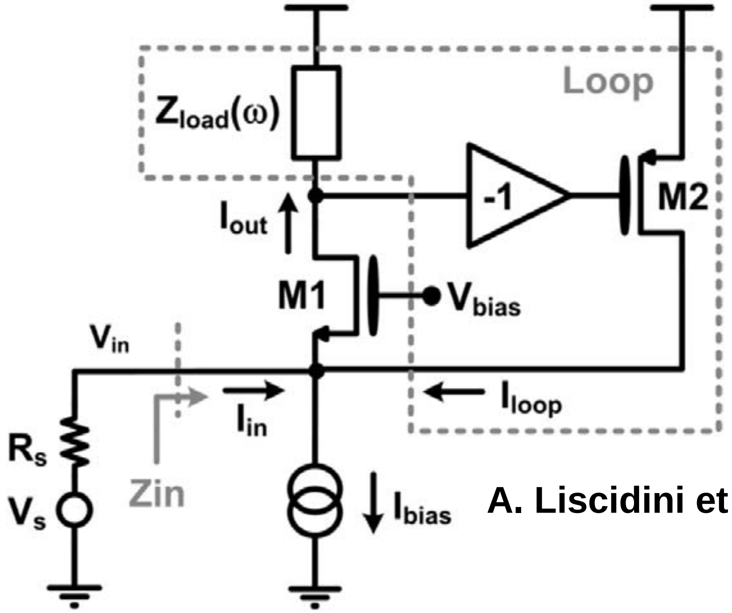
- Less sensitive to matching parasitics
  - All parasitics that are parallel to Ls can be easily tuned out
- Matching and gain and NF can not be independently chosen
- Noise Figure
  - Assuming channel thermal noise is the dominant source of noise

$$F = 1 + \gamma g_{d0} / g_m$$

  - γ ranges from 1 – 3 depending on the operating region and channel length of the amplifying device



Common-Gate (CG) LNA with Positive Feedback



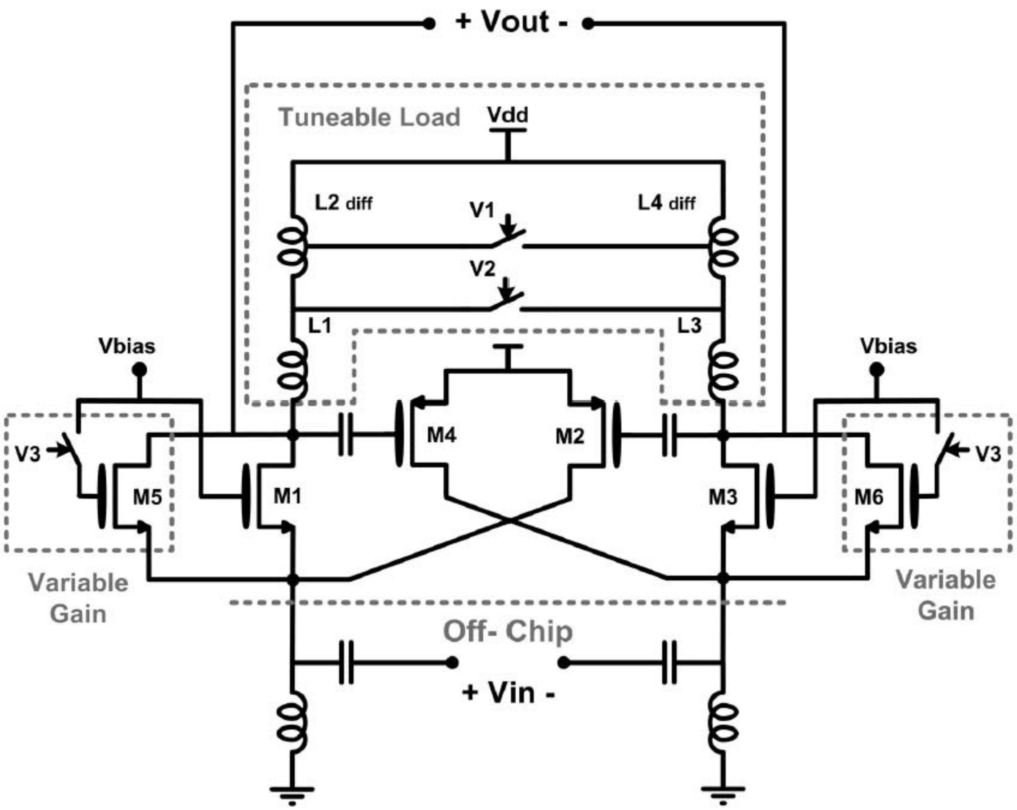
A. Liscidini et al., JSSC April 2006

- The feedback loop adds a degree of freedom to the design
- For a given match (given g_m) gain can be increased through the positive feedback
- Improved NF
- Ideal for multi-standard front-ends

BUT watch for

- Linearity hit
- Oscillation

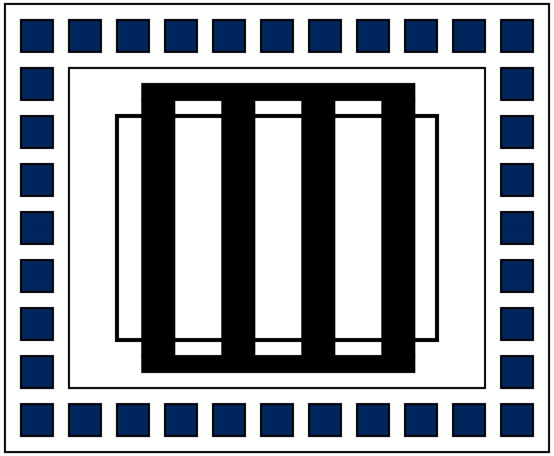
Multi-Band Positive Feedback Variable Gain LNA



- Fully differential implementation
- Switched inductors used for frequency tuning
- Variable gain is achieved by controlling gm of the amplifying device

Layout Considerations

- NF can be easily degraded by poor layout
  - Substrate taps to reduce substrate resistance



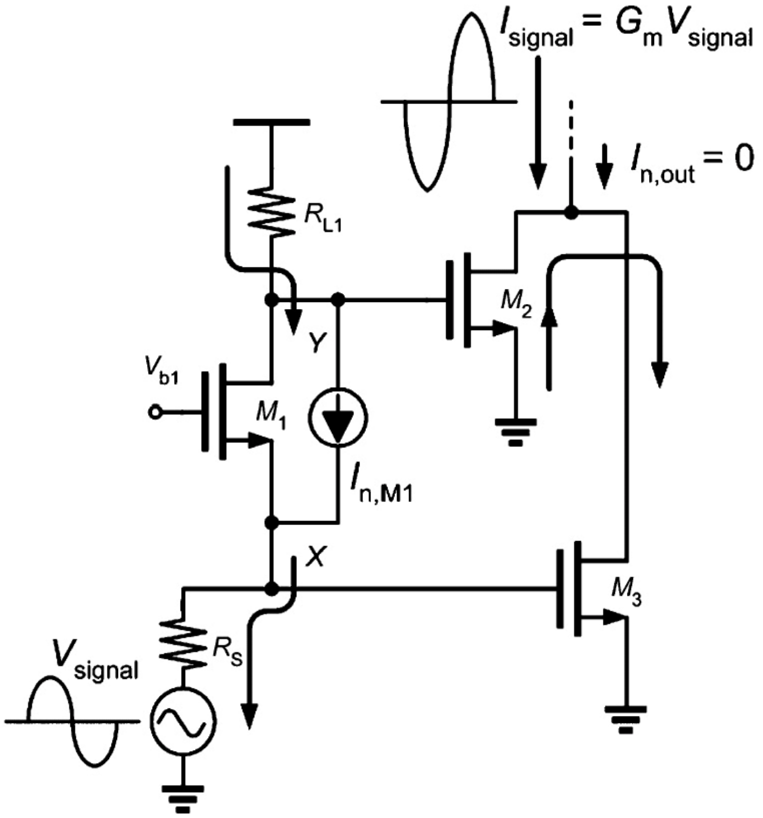
  - Watch for
    - gate resistance
      - Avoid long and skinny gates
      - Make gate contacts on both sides
    - Resistance along the signal path

Noise Canceling Techniques

- Noise voltages at nodes X and Y are fully correlated and they are 180 degrees out of phase.

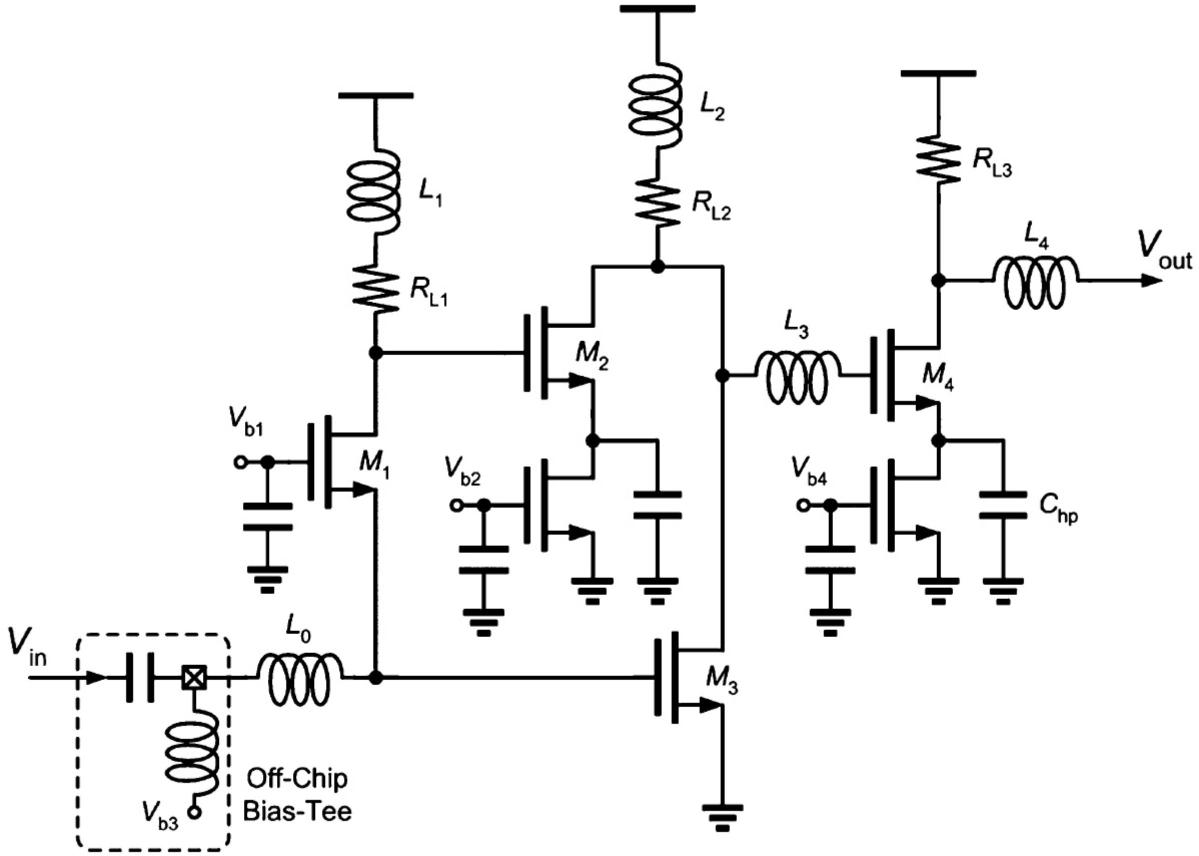
At the same time …

- Signal voltages at nodes X and Y are in-phase
- Can cancel noise while passing signal



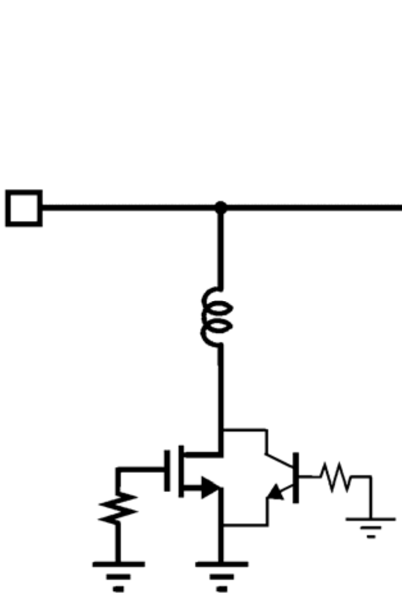
C. Liao et al, JSSC Feb 2007

Noise Canceling – Actual Implementation



C. Liao et al, JSSC Feb 2007

ESD Protection at the LNA input

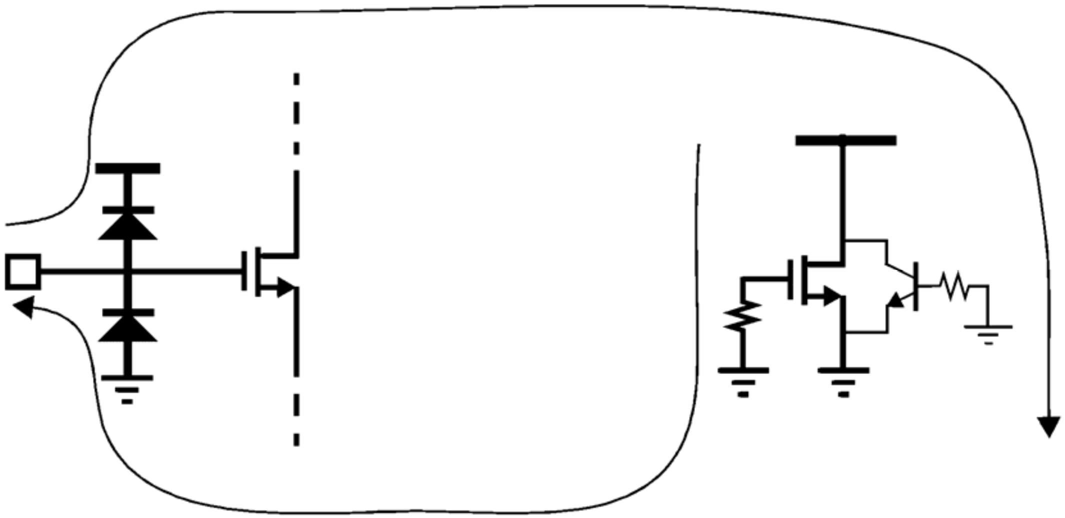


- Can use standard ESD protection at the input
- Equivalent capacitive load imposed on the input can be quite high
  - Can be tuned out by an on-chip inductor

BUT

  - Inductor must be able to handle the ESD current

ESD Protection



- In many practical applications PN diodes can be used to route the ESD current to a nearby (ESD protected) Supply or ground

Conclusions

- Designing integrated CMOS LNAs require detailed analysis of the trade-offs between
  - Gain
  - Noise
  - Power dissipation
  - Matching
  - Linearity
  - Stability
- Careful layout techniques are just as important
- Choice of architecture is very application dependent