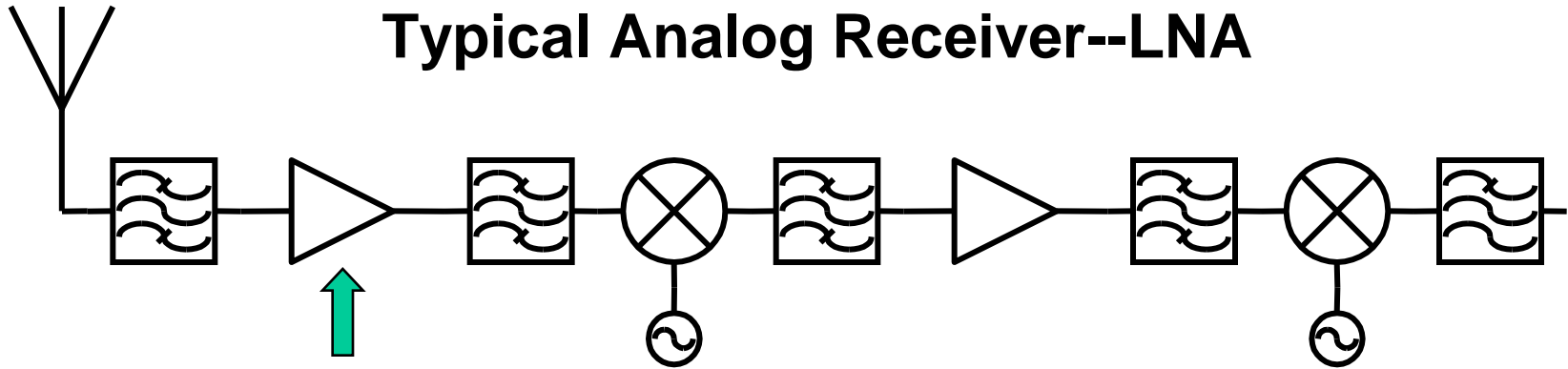




Some Really Simple Noise Modeling

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Besser Associates (sometimes)
Retired (mostly)

Typical Analog Receiver--LNA



Desired is a large dynamic range, that is:

- Low noise figure
- Large signal ability: IIP3, IIP2, P-1dB
- Good input and output match
- Low dc power required

Reality

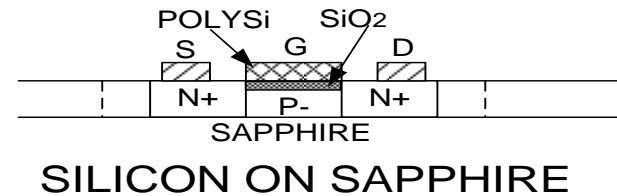
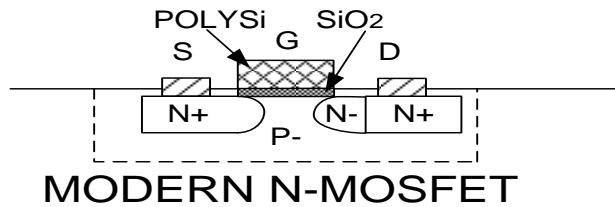
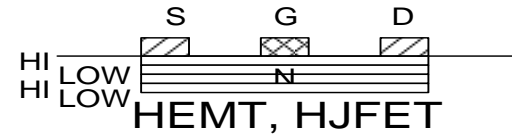
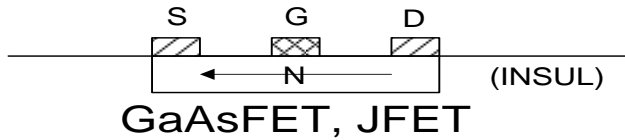
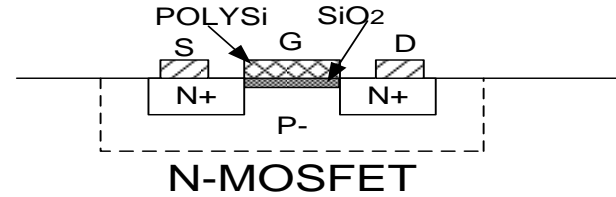
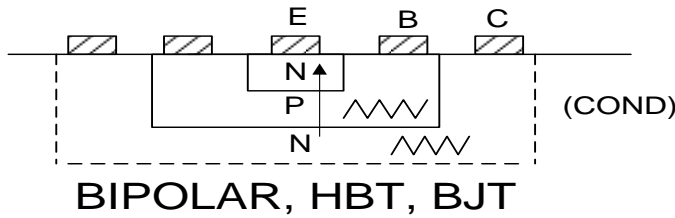
- dc input vs. power handling
- Best noise bias not good power
- Noise and gain match impedances are not the same. Also, matching for maximum power output lowers gain, hurts overall noise figure.

Why is LNA design such a pain?

Are some devices better than others?



DEVICE STRUCTURES

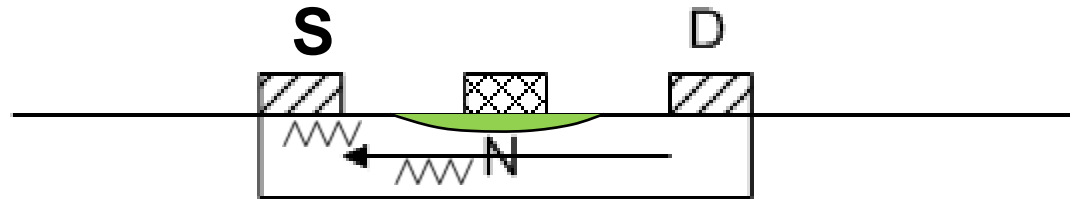


CMOS=BOTH N AND P CHANNEL FETS AVAILABLE

BICMOS=CMOS AND BIPOLAR TRANSISTORS AVAILABLE



Simple FET



GaAsFET, JFET



Final Comments on Transistor Noise

- The high input Q of a low noise FET makes the Q of the input tuning inductor very important. Small FETs → large inductor → parasitics, low Q
- Bipolar transistors have higher G_m at low current, Therefore, small, low I bipolar transistors are much easier to match.
- For example the 50 ohm, untuned performance—
 - 20 GHz F_t MOSFET 1.2mA for 3dB NF
 - Bipolar transistor .25mA for 3dB NF
- Bipolar transistors have a shunt resistor, r_{π} across their input that limits their low frequency current gain to β , and their noise performance to $F=1+1/\sqrt{\beta}$
- What about induced gate noise, noise correlation, and all that other stuff? They matter some, but the basic ideas are still the same, with the optimum noise match impedance shifted from these simple calculations.