



# Fifth IEEE Dallas Circuits and Systems Workshop

October 29 -- 30 2006  
The University of Texas at Dallas

CALL FOR PAPERS

## Circuits & Systems: Design, Applications, Integration and Software

### Organizing Committee

General Chair: Poras Balsara, UT Dallas

Technical Program Chair: Bogdan Staszewski, Texas Instruments

Publicity Chair: Dinesh Bhatia, UT Dallas

Publications Chair: Sudhind Dharmankar, Texas Instruments

Local Arrangements Chair: Arjun Rajagopal, Texas Instruments

Registration Chair: Luke Wu, Texas Instruments

Treasurer: Ping Gui, SMU Dallas

IEEE-DCAS Chair: Liming Xiu, Texas Instruments

### Program Committee

Bogdan Staszewski, Chair, Texas Instruments

Weiping Shi, Texas A&M

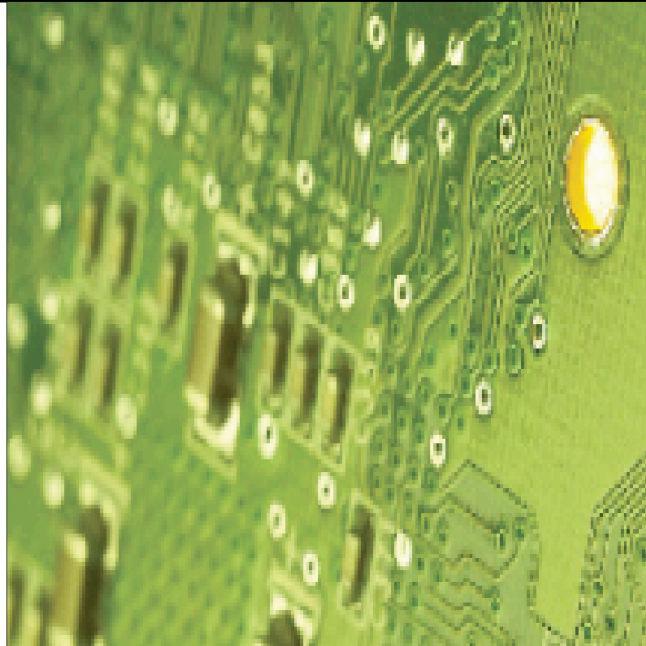
Mitch Thornton, SMU

Oren Eliezer, Texas Instruments

Andrew Marshall, Texas Instruments

Terry Blake, Texas Instruments

Vijay Angarai, LSI



Systems-on-Chip (SoC) with giga-scale integration of IP are the main drivers of the semiconductor industry today. From the handsets and multimedia consumer electronics devices to communication infrastructure, the SoC's create new challenges in design techniques, circuits, integration, power management, packaging and test. The IEEE Dallas Section, Circuit and System Society is conducting a two day workshop (DCAS-06) to provide a forum for sharing Design, Applications, Integration and Software Aspects of Circuits and Systems.

DCAS-06 is sponsored by the IEEE Circuits and Systems Society (Dallas Chapter), and will be held on the campus of The University of Texas at Dallas.

### Technical Program

The technical program committee invites researchers from academia and industry to contribute new and previously unpublished results in the following Circuits and Systems related areas:

*High Performance & Low Power Circuits*  
*Digital Signal Processors and Cores*  
*Baseband Communication Processors*  
*RF Processors and Circuits*  
*Multimedia Processors*  
*Reconfigurable Processors*  
*Low Voltage and Mixed Signal Circuits*  
*Mixed Signal Integration*  
*Clocking and Clock Distribution*  
*A/D and D/A Conversion*  
*High Speed I/O*  
*Power Management for SoC*  
*Signal Integrity and On-Chip Interconnects*  
*SoC Implementation Methodology*  
*SoC Verification Methodology*  
*SoC and IP Integration*

Papers will be accepted for lecture or poster presentation. All accepted papers will be printed in the conference proceedings and online at IEEE Xplore.

### Submission Guidelines

Authors are invited to submit a paper draft, not to exceed four pages, to the technical program chair Dr. Bogdan Staszewski (b-staszewski@ti.com). The Submission must include the title, authors names, affiliations, and contact e-mail. Authors are encouraged to follow the instructions posted on the workshop website.

### Paper Submission Details

Submission Deadline : August 4, 2006  
Acceptance Notice : August 18, 2006  
Camera Draft Due : September 1, 2006

<http://www.ewh.ieee.org/soc/cas/dallas/wks2006/>