Directions to UTD

From Campbell Rd., east of Waterview, turn north onto University Parkway. Come to the Guard's Station at top of parkway. The Guard can point out the Engineering & Computer Science Complex, direct you to the visitor parking in LOT J, and give you a parking permit. Enter at southwest door at the corner of Rutford Street and Drive A for the TI Auditorium

Local Map of Workshop Venue

Lunch and dinner arrangments have been made in the Galaxy room in the student union (SU) building.

UTD

The University of Texas at Dallas
Engineering and Computer Science
2601 North Floyd Road
Richardson, TX 75080-1407
972-883-2111

Fifth IEEE Dallas Circuits and Systems Workshop

October 29 - 30 2006
The University of Texas at Dallas

Design, Application, Integration, and Software

Sponsored by the Dallas Chapter of IEEE CAS, and by the IEEE Circuits and Systems Society

http://www.ewh.ieee.org/soc/cas/dallas/wks2006/

Technical Program
Sunday, October 29, 2006

10:45 AM - Opening Remarks

10:50 AM - High Throughput, Parallel, Scalable LDPC Encoder/Decoder Architecture for OFDM Systems
Yang Sun, Marjan Karkooti, Joseph Cavallaro
Rice University, Houston, U.S.A.

11:10 AM - Power-Supply Noise Attributed Timing Jitter in Nonoverlapping Clock Generation Circuits
Adam Strak, Hannu Tenhunen
KTH - Royal Institute of Technology, Sweden

11:30 AM - Optimal Gate Size Selection for Standard Cells in a Library
Vipul Singhal, Girishankar G.
Texas Instruments, Bangalore, India

11:50 AM - Exact Toffoli Network Synthesis of Reversible Logic using Boolean Satisfiability
Daniel Grosse, Xiaobo Chen, Rolf Drechsler
University of Bremen, Germany

2:00 PM - Grand Challenge: The Future of CMOS System-on-Chip Hardware and Software Application Development
Brian Von Herzen, Mike Lerer
Rapid Prototypes, U.S.A.

2:20 PM - A Built-in Tester for Modulation Noise in a Wireless Transmitter
Oren Eliezer, Ofer Friedman, R. Bogdan Staszewski
Texas Instruments, Dallas, U.S.A.

2:40 PM - Efficient Procedures for Analyzing Large-scale RF Circuits
Josef Dobes
Czech Technical University in Prague, Czech Republic

3:30 PM - Feedforward Interference Cancellation in Narrow-Band Receivers
Ranjit Gharpurey, Sahar Ayazian
University of Texas, Austin, U.S.A.

3:50 PM - Analog-to-Information Conversion via Random Demodulation
Sami Kirolos, Jason Laska, Michael Wakin, Marco Duarte, Dror Baron, Tamer Ragheb, Yehia Massoud, Richard Baraniuk
Rice University, Houston, U.S.A.

4:10 PM - A Fixed-Point Implementation for QR Decomposition
Chitranjan K. Singh, Sushma H. Prasad and Poras T. Balsara
University of Texas at Dallas, Richardson, U.S.A.

Sunday Posters

Design Methodology of On-Chip Power Distribution Network
Hirokazu Tohya, Noritaka Toya
ICAST Inc., Japan

Phase Noise Reduction in High Frequency Divider
Rahul Prakash, Siraj Akhtar* and Poras T. Balsara
University of Texas at Dallas, Richardson, Texas, *Texas Instruments, Inc. Dallas, Texas

Performance Optimization of Re-Convergent Manchester Carry Chain Adders
Kumar Yelamarthi, Henry Chen
Dayton, U.S.A.

Noise Analysis of Time-to-Digital Converter in All-Digital PLLs
Socrates Vamvakos, R. Bogdan Staszewski, Mahbuba Sheba, Khurram Waheed
Texas Instruments, Dallas, U.S.A.

An Approach to Interference Detection for Ultra Wideband Radio Systems
Tien-Ling Hsieh, Peter Kinget*, Ranjit Gharpurey
University of Texas, Austin, U.S.A.
*Columbia University, U.S.A.

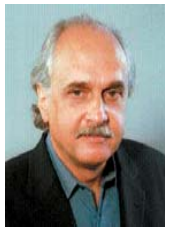
Dynamic Multi-Point Rational Interpolation for Frequency-Selective Model Order Reduction
Mehboob Alam, Arthur Nieuwoudt, Yehia Massoud
Rice University, Houston, U.S.A.

Novel Voltage-Mode Structurely Allpass Filters without External Passive Components
Nil Tarim, Fatih Golcuk, Oguzhan Cicekoglu*, Hakan Kuntman
Istanbul Technical University, Turkey, *Bogazici University, Turkey.

Tuning Word Retiming of a Digitally-Controlled Oscillator Using RF BIST
Imran Bashir, R. Bogdan Staszewski, Oren Eliezer
Texas Instruments, Dallas, U.S.A.

Technical Program
Monday October 30, 2006

Keynote Address
Short Distance Wireless
Prof. Jan Rabaey
University of California, Berkeley, U.S.A.
Time - 8:30 AM



Prof. Yannis Tsividis
Mixed-Domain Signal Processing
Columbia University, New York, U.S.A.
Time - 9:40 AM

Dr. Bill Krenik
Cellular Handset Integration
Texas Instruments, Dallas, U.S.A.
Time - 11:00 AM

Prof. Michael Frank
Reversible Computing & Truly Adiabatic Circuits: The Next Challenge for Digital Engineering
Florida State University, U.S.A.
Time - 3:20 PM

Prof. Boris Murmann
Digitally Assisted Analog Circuits
Stanford University, U.S.A.
Time - 1:45 PM

Monday Posters

Reliable Interconnect Grid for Ultra Deep Submicron
Ali Namazi, M. Nourani, M. Saquib
University of Texas at Dallas, Richardson, U.S.A.

A Technique for Device Stress Relief in CMOS Class-E RF Power Amplifiers
Xin Wang, Chih-Kai Kang, Ranjit Gharpurey
University of Texas, Austin, U.S.A.

All-Digital PLL with Variable Loop Type Characteristics
R. Bogdan Staszewski, John Wallberg and Poras T. Balsara*
Texas Instruments, Dallas, U.S.A., *University of Texas at Dallas, Richardson, U.S.A.

Random Sampling for Analog-to-Information Conversion of Wideband Signals
Jason Lasko, Sami Kirolos, Yehia Massoud, Richard Baraniuk
Rice University, Houston, U.S.A.

Ring Oscillator Performance and Parasitic Extraction Simulation in FinFET Technology
Mak Kulkarni, Andrew Marshall, C. Rinn Cleavelin, Weize Xiong, Christian Pacha*,
Klaus von Armin*, Thomas Schulz*, Klaus Schruefer*, Paul Patruno**
Texas Instruments, Dallas, U.S.A., *Infineon Technologies AG, Germany, **SOITEC S.A., France

Boolean Function Matching using Walsh Spectral Decision Diagrams
Jason Moore, Kenneth Fazel, Mitchell Thornton, D. Michael Miller*
Southern Methodist University, Dallas, U.S.A, *University of Victoria, Canada

Supply Voltage Adaptive Low-Power Circuit Design
Sami Kirolos, Yehia Massoud
Rice University, Houston, U.S.A.

Fractional-N Frequency Synthesizer- A Novel Approach
Xiao Pu, Axel Thomsen*
University of Texas, Austin, U.S.A., *Silicon Laboratories, Austin, U.S.A.

Spur-Free Fractional-N PLL Utilizing Precision Frequency and Phase Selection
Erkan Bilhan, Feng Ying, Jason Meiners, Liming Xiu
Texas Instruments, Dallas, U.S.A.

Complete Formal Verification of Multi Core Embedded Systems Using Bounded Model Checking
Ulrich Kuehne, Daniel Grosse, Rolf Drechsler
University of Bremen, Germany