Packaging of electronics is no longer making discrete components and interconnecting them, since it leads to bulky, costly and low-performance and low-reliability systems. The new and emerging paradigm is about package and systems integration enabled by thin film component integration leading to ultra miniaturized, lower cost, higher performance and higher reliability systems. This Package integration is taking place everywhere—at IC level, package or module level and at system level. At IC level, it is by means of a package overlay on CMOS; at module level, it is by means of SIP; and at system level, it is by means of SOP. The SOP paradigm changes the current chip-centric SOC methodology to a cheaper, faster-to-market, system-driven, IC-package-system co-design flow. The advantages of the SOP and SIP paradigms that are based on package integration appear overwhelming due to their design simplicity, lower cost, higher system integration and electrical performance, without the intellectual property issues that dominate SOC. While package integration is common, SOP and SIP are different. The 3D packaging is typically the stacking of similar or dissimilar chips. The SIP goes one step beyond by stacking packaged components leading to sub-system modules. The SOP is the ultimate 3D integration of thin film components at IC, package and system levels leading to heterogeneous digital functions.

This workshop reviews the latest R & D and manufacturing status of each of these 3 “hottest” electronic technologies around the world. It will also attempt to compare and contrast SOC, 3D stacking, SIP, SOP and MCM.