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## Member-Get-A-Member Program Gets An Upgrade For 2007

Submitted by Ralph W. Russell, II  
IEEE CPMT Society Strategic Director for Membership and  
Chapter Development

Beginning in September of this year, the Member-Get-A-Member (MGM) program will undergo several significant enhancements. First, the payout for recruited higher grade members will be raised from the current \$5.00, to \$15.00 per member. Further, recruiters will have the option of using their reward vouchers to pay for IEEE products or services (including their membership renewal), or, if they prefer, they can choose to use the vouchers to have a donation made in their name to the IEEE Foundation.

The MGM program has been one of our more successful recruitment programs. Please spread the word of these important changes and help to make this program even more successful in 2007. Find out more at [www.ieee.org/mgm](http://www.ieee.org/mgm).

To assist members who wish to participate in the program, some tools have been developed. These include a descriptive brochure of the MGM program with recruiting tips, and an IEEE-logo'd business card with space where the recruiter can fill in their name and member number. The brochures for the 2007 program will be available in September, while the business cards are available now. Both can be ordered online at: [www.ieee.org/ra/md/mdsupplyform.html](http://www.ieee.org/ra/md/mdsupplyform.html).

Please note that the vouchers for the 2006 MGM program, which will be issued during September, will be calculated under the 2006 program rules. No changes have been made to the Student-Get-A-Student (SGS) program.

## Chapter News

**Region 10 Chapter Activity Round-up**  
By Dr. P.B. Parikh, Region 10 News Coordinator

### **TAIPEI CHAPTER:**

**Prof. Lih-Shan Chen**- Chairman of Taipei CPMT Chapter has reported the following activities during this quarter.

As reported in our previous issue, CPMT Taipei Chapter co-organized the "2006 International Symposium on Advanced Packaging and Green Packaging Technology", with IMAPS Taiwan Chapter. This four day event was held from June 28th to July 1st, 2006 at the Taipei World Trade Center, Taipei, Taiwan. More than 120 participants took part in this seminar. Besides the technical program, there was an Exhibition for four days of the seminar.

Invited speakers at the seminar included

- i) **Dr. Ho-Ming Tong** - "IC Packaging Trends and Challenges from New Packaging Materials".
- ii) **Dr. Michael Pecht** - "Accelerated Testing; Ways to Understand Reliability Quickly and Accurately".

Dr. William T Chen- President of IEEE CPMT Society and Dr. Ho-Ming Tong - President of Advanced Semiconductor Engineering (ASE) Inc. visited Dr. Shen-Li Fu Chairman of IEEE CPMT Taipei Chapter on 2<sup>nd</sup> August, 2006 and had discussions on the affairs of the Society.

### **MALAYSIA CHAPTER**

**Dr. Ch Chew** –Chairman of Malaysia CPMT Chapter, has reported that the chapter activities have picked up and the chapter has become more eminent and diversified with joint efforts from the newly pulled-in committee members from FREESCALE, INTEL and INFINEON.

The following talks have been planned and being conducted during this quarter by the chapter;

- i) "Applications of FEA in Semiconductor packaging design"
- ii) "Analytical tools in Semiconductor Industry".

The executive committee members of the chapter are busy preparing for the International Conference on Electronics and Manufacturing Technology (IEMT 2006 – 8,9,10 Nov) and four informative DLPs. These are to be held for the first time in KL Asia with the support from CPMT SCV, IEEE and various industry sponsors.

Around 78 papers and more than 20 posters have been selected out of 130+ abstracts received till date. In addition to a well organized technical conference as above, the organizers have assured varieties of food, sceneries and cultural shows of Malaysia.

Further information for registration and conference details can be obtained from the link [www.ieee.org.my/iemt2006/](http://www.ieee.org.my/iemt2006/).

The Chapter Officers and the Committee members for 2006 are

Chair:	Dr. CH Chew, ON Semiconductor
Vice Chair:	Dr. Ishak Abdul Azid, University Science Malaysia
Treasurer:	Azhar Aripin
Committee Members:	Dr. Chee Choong Kooi, Intel Wee Teck Lim, ON Semiconductor Fuaida Harun, Infineon Shutesh Krishnan, ON Semiconductor LC Tan, Freescale

### **IEEE INDIA COUNCIL CHAPTER**

The chapter has launched a well organized membership drive since October 2005 through our contacts with the electronic component industry and the academic institutions. Effective presentations on IEEE CPMT Society activities in India and at global levels were made during the three co-organized events (seminars and conferences) during the year. One more such opportunity will be availed during the forthcoming annual IEEE India Council seminar in December 2006.

Due stress is being placed on increased awareness of the activities of the CPMT society and the need for knowledge sharing on latest technological developments in the areas of electronic component production and electronic equipment manufacturing activities including Surface Mount Technology.

## IEEE CPMT Phoenix Chapter Tutorial Update

Submitted by Dr. Mali Mahalingam

IEEE CPMT Phoenix Chapter

### Thermal Design and Management in Electronics

Thermal design and management challenges are common across a wide range of electronic products and applications. Road mapping by leading organizations (ITRS, SIA, and NEMI) identifies thermal management as one of the key enablers for the sustained growth in electronics industry. Higher density, increasing performance, robust reliability requirements and lower cost demand much from the thermal management professionals in creating thermal solutions. This half-day tutorial organized by the IEEE CPMT Phoenix Chapter was taught by four Phoenix area professionals and addressed: Modeling and Characterization, Design & Applications challenges in the Computational and Wireless Communication Products, and Emerging Technologies. Nearly sixty professionals took advantage of this professional learning opportunity.



Dr. Tom Lee, Freescale Semiconductor Inc., discussed “Simulation and Characterization Methods in Electronics Thermal Design and Management”. Thermal simulation and characterization are two essential tools to evaluate and optimize thermal performance of electronics products.

Experimental characterization usually can provide a direct and accurate way to measure device or package temperature; however, the efforts to prepare samples and the number of experimental matrix needed may be time consuming and sometimes costly. On the other hand, advancements in software and computing speed make modeling and simulation as effective methods in analyzing and predicting thermal performance. However, the uncertainty in material properties, modeling simplification and assumptions, plus various numerical meshing techniques may limit the accuracy of the results. Careful use of both experimental characterization and simulation can make up for the deficiency in each and provide realistic and accurate results. Infrared (IR) Thermal Imaging is a direct tool to measure the surface temperature, both for the area thermal field and for detecting the local hot spot. A simulation and modeling methodology generally includes model building, assigning material properties, assigning boundary conditions, meshing, numerical solution, and post processing for temperature and flow visualization. There are a variety of Finite Element Method-based and Finite Volume Method-based software tools available in the market. Each tool has its uniqueness and limitations. The recent trends for commercial codes are: enhanced interfaces with MCAD and ECAD tools; add-on capability for board-level thermal analysis; ability to create Compact Thermal Models (CTM); Improved parametric and design optimization capabilities; and supporting 64-bit processors for computational efficiency.



Dr. Chia-Pin Chiu, Intel Corporation, presented “Thermal Design and Management for High-Power Microprocessors”. Increasing microprocessor performance has historically been accompanied by increasing power and increasing on-chip power density both of which present a cooling challenge. With the transition to multi-core microprocessor architectures, dramatic increases

in Thermal Design Power (TDP) are not observed to occur when processor performance increases. Thermal designers still need to account for areas of thermal non-uniformity typically referred to as hot spots, where power densities of 300+ W/cm<sup>2</sup> are possible. These hot spots typically caused by a non-uniform distribution of power dissipation on the die will dictate reliability and performance. In addition to the die, the hot spots can also occur in the interconnect, package substrate, and socket contacts due to Joule heating. It must be noticed that processor current levels have increased over the past two decades. Industrial and academic researchers have correspondingly increased their focus on elucidating the problem of hot spots and developing innovative solutions in devices, circuits, architectures, packaging and system level heat sinking. The current strategy is to enhance heat spreading and reduce package thermal resistance. This is followed by additional system-level thermal solution such as liquid cooling and refrigeration.



Dr. Mali Mahalingam, Freescale Semiconductor Inc., presented “Thermal Design and Management for RFPAs in Wireless Applications”. Similar to Microprocessors being the key component in computing applications, Radio Frequency Power Amplifiers (RFPAs) are the key components in the wireless communication applications.

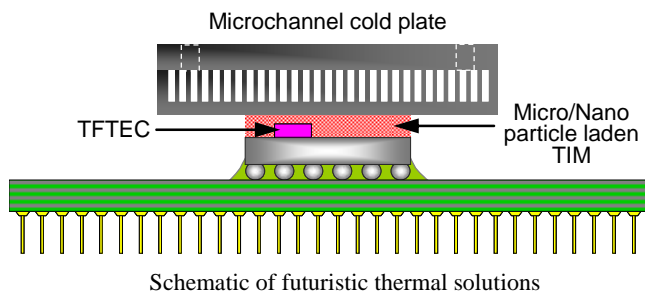
Trends in power levels for RFPAs used in both mobile products and fixed infrastructure equipment were reviewed. Thermal design and management at the component level are conduction dominated. The presentation addressed both the fundamental aspects of conduction heat transfer and the state of the art practices in creating successful solutions at the product level. RFLPA devices in a mobile phone, even as they dissipate small amounts of heat (~ 1+ W), are in a very limited space and require careful thermal solution; device layout, die thinning, and thermal vias in the Printed Circuit Board (PCB) play key roles in achieving effective thermal management. RFLPA devices in basestations dissipate large amounts of heat (~ 5W – 250 W) and pose many tough thermal challenges; at the device level they represent one of the highest thermal density among electronic devices (~ 3 kW/cm<sup>2</sup> at die level); die layout to reduce spreading resistance, die thinning, improved metallurgical bond to reduce bond resistance, engineering high thermal conductivity substrate materials, and reducing interfacial contact resistance by managing flatness & surface roughness all play key roles in the thermal management at the component level. For basestation equipment, at the system level, cooling is primarily by free and forced air convection utilizing large heatsinks.



Dr. Ravi Prasher, Intel Corporation, discussed “Micro/Nanotechnology in Electronics Thermal Management Applications”. There are two thermal problems in microprocessors: increasing total power dissipation and non-uniform heat generation that gives rise to multiple hotspots.

The design requirement for electronics cooling is to maintain the hottest location (hotspot) on the die (chip) below the specified temperature. Due to the presence of multiple hotspots, the thermal resistance near the die (package) is high; thus the focus of next-generation electronics cooling is on developing efficient cooling solutions near the package. Futuristic cooling solutions may be based on micro and nano technologies. The schematic of such a cooling solution is shown in below figure. These solutions might include a Thermal Interface Material (TIM)

made from micro and nanoparticles, a microchannel heat exchanger, and a Thin Film Thermoelectric Cooler (TFTEC) that is made of thin film superlattices, or nanocomposites, placed directly above the hotspots to provide localized cooling. To enable these micro/nanotechnologies, however various challenges must be met. The main challenges are a) to reduce the boundary/interface resistance between the nanoparticles and the host medium for nanoparticles-based TIMs and to increase the reliability performance of TIMs, b) reduce the assembly-related parasitic effects seen in TFTEC, thus improve the effective Figure of Merit, ZT and c) pumping requirements and pump reliability for microchannel cooling.



Schematic of futuristic thermal solutions

### Failure Analyses for Electronics Packaging

This half-a-day tutorial organized by IEEE CPMT Phoenix section was taught on Sept. 19<sup>th</sup> 2006 by four Phoenix area professionals. Basic methods, tools and techniques practiced in the failure analyses of electronic packaging were addressed with an in-depth discussion on acoustic microscopy. Applications in Eutectic die attach, Pb-free solders, Plastic Packaging and Flip Chip Interconnect were discussed. The tutorial looked beyond the limitations of current day's tools and techniques to address the needs of next generation interconnect and package technologies. Nearly forty five professionals took advantage of this professional learning opportunity.



Dr. Jonathan Harris, CMC Interconnect Technologies, discussed "How Interfacial Structure Can Play a Major Role in Package Reliability?" He explained what IMCs (Inter Metallic Compounds) are and the general role of IMC's microstructure on the reliability of package construction. Specifically, he elaborated on the role of intermetallic compound morphology in determining failure modes when mechanical stress is applied to the package. His examples were drawn from AuSi and AuSn eutectic attaches as well as Pb free solder SnAgCu. He also explained for each of these three examples how to control the microstructure of IMCs to minimize their impact on interfacial reliability.



Mr. Ken Tylor, Sonoscan, Inc., presented an "Introduction to Acoustic Micro Imaging and Its Applications". Ultrasound is a form of mechanical energy and is, therefore, sensitive to the elastic properties of the materials it travels through. It is particularly sensitive to locating air gaps (cracks, delaminations and voids). Acoustic Micro Imaging (AMI) uses high frequency ultrasound (5 – 300MHz) to image internal features and characterize physical defects that occur during the manufacturing process or environmental stress. In his presentation, Ken provided an over-

view of the basics of ultrasound, how it is used for Acoustic Imaging, and explored a wide variety of applications (die attach void, interfacial delamination in plastic encapsulated ICs, power devices and flip chip packages). He covered the role of AMI in industry standards and current developments for improved imaging techniques.



Dr. Dev Gupta, APSTL, presented "Failure Analyses for Flip Chip Packages". Dev emphasized on the philosophy of FA analyses for Flip chip packaging, from the traditional analyst approach, from the team (design, material. Process) approach and finally from the root cause analysis i.e a unified approach. Dev walked through the basics of Flip chip packaging technology (bump, substrate, assembly, accelerated test) and typical failures. He elaborated on two case studies – void and delamination.



Dr. Rajen Dias, Intel Corporation, discussed "Next Generation Analytical Tools for Package Failure Analysis" Advanced packaging solutions for high performance microprocessors involve use of multi-level interconnections, shrinking geometries and improved thermal solutions. These trends together with the introduction of low k dielectrics and Cu metallization in next generation Si technologies and new package substrate materials has resulted in severe die/package thermal - mechanical mismatch concerns. Packaging solutions for non CPU applications such as memory, chip sets, networking and communication chips are driven by miniaturization, stacked die for increase in functionality and Pb free applications. Understanding the defect and intrinsic failure mechanisms during the development and certification of these new package technologies is becoming extremely difficult and time consuming using traditional approaches to failure analysis. In his presentation, Rajen focused on advancements in three nondestructive tools – Scanning SQUID microscopy for detecting shorts, 3D x-ray radiography / tomography for imaging various levels of interconnections and thermal imaging for fault isolation in thermal failures. In addition, he also discussed analytical tools such as Laser Spallation for understanding interfacial adhesion and Laser milling for package delayering and microsurgery.

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**Additional Information at [www.cpmt.org](http://www.cpmt.org)**