- Computer, networking and telecommunication products are still driving performance and technology complexity for both semiconductors and packages.
- Embedded passives and optical waveguides on packages with on-chip electro-optical devices is finally ready for primetime.
- 3D packaging with through-hole vertical silicon vias and bump connection technology is making thin products even thinner.

The website contains many of the paper abstracts and presentation slides. To fully understand the comprehensiveness and value of this workshop, we encourage you to have a look.

Needless to say, Lake Como was a beautiful serene place to meet people and have a workshop that taught us so many new things. The next European workshop will be held in 2009 at Blarney, Ireland in County Cork: another wonderful place to learn and meet new friends. The 2008 Japanese TCSP workshop will be held in the beautiful Hakone resort region of Japan.

Check at the TC website (www.ewh.ieee.org/soc/cpmt/tc14/) for upcoming information.

Chapter Reports:

Backend Wafer Processing Technologies

Submitted by Dr. Mali Mahalingam, Tutorial Committee Chair, IEEE CPMT Society Phoenix Chapter

This half-a-day tutorial was taught on behalf of IEEE CPMT Society Phoenix Chapter on April 18th 2007. Dr. Mali Mahalingam, chair for the tutorials technical program worked with his fellow Phoenix CPMT officers in organizing this totorial. Four major areas of ***Backend Wafer Processing Technologies*** that precede and enable backend assembly and packaging were the focus of the tutorial. Forty six professionals took advantage of this professional learning opportunity.

Stacked Die Packaging and many consumer applications are driving ***Wafer Thinning*** technologies relentlessly. High performance applications demanding excellent thermal, electrical and mechanical performance for die attach are making continuous demands on ***Wafer Backside Metallization***. Flip Chip interconnect assembly is pervasive in high performance applications and now expanding to consumer applications thus propelling further growth in ***Wafer Bumping*** technologies. Numerous new challenges have arisen in ***Wafer Dicing*** due to use of Cu metallization and low-K dielectric materials in wafer fabrication. Each presenter presented an overview of basic technologies, discussed current challenges, and offered solutions in their respective areas.

Mr. Scott Drews, a Senior Applications Engineer for SEZ America, Inc. presented the topic of **Wafer Thinning.** As consumers demand greater product functionality in smaller packages, device manufacturers look for ways to integrate, through system-in-package (SiP), system-on-chip (SoC) and stacked die packaging. In order to maintain low die profiles in stacked die packaging, most manufacturers target final silicon thicknesses below 100um. While several methods exist for wafer or die thinning prior to packaging, manufacturers must take into consideration issues relating to process integration, waste abatement, reliability, die yield and cost-of-ownership when selecting which method (or combination of methods) to implement.

Dr. Jonathan Harris, President of CMC Interconnect Technologies, presented the topic **Wafer Backside Metallization.** Backside metallization of semiconductor devices followed by solder based die attach results in a die bond with excellent thermal, electrical and mechanical properties. The presentation focused on the back-side metallization of semiconductor wafers to achieve this type of high performance die attach. Both silicon and GaAs devices spanning applications in RF & Microwave, Power Control and Optical Devices were discussed. Various backside metallization systems, the design attributes for these metallization systems and the material science behind achieving key back side metallization requirements for each application were discussed. Deposition technologies including sputtering, evaporation and plating technology were discussed and compared.

Mr. Ted Tessier, Chief Technical Officer at Flip Chip International in Phoenix Arizona presented the topic of **Wafer Bumping: The Past, The Present and The Future.** After a rather lengthy period of development and adoption for high performance computing and automotive applications, wafer bumping and flip chip assembly technologies are now rapidly being accepted for use in consumer electronics and handheld communications applications. From these initial Flip Chip in Package beginnings, a number of bumping technologies have emerged to support a wide range of semiconductor device requirements and packaging applications. This presentation provided an overview of the history of wafer bumping technologies including the adoption of thin film redistribution options to broaden the applicability of wafer bumping to ICs designed with wirebond centric peripheral pad arrangements. The emergence of Wafer Level Chip Scale Packaging (WLCSP) was discussed and the differences between flip chip and WLCSP bumping technologies were compared.

Mr. Alan Magnus, a Member of the Technical Staff at Freescale Semiconductor Inc. in Tempe, Arizona, presented the topic of **Wafer Dicing.** The drive for low cost microelectronics with enhanced electrical performance has introduced wafer fabrication materials and advanced packaging requirements that present an ever increasing challenge for the wafer dicing operation. Some complications stem from the wafer fabrication materials such as multi-level interconnects of Cu metallization and low k interlayer dielectric materials. Packaging constraints play a role through die thickness and mechanical strength requirements, as well as bumping or back metal needs. Finally economic issues, whether reduced scribe widths to increase the number of good die per wafer,

or simply cost reduction at saw through increased feed speeds and blade life all contribute to the increasing difficulty of dicing wafers. This presentation provided an overview of the wafer dicing process and the available dicing technology options. More focused discussions were on mechanical saw and the key process parameters that need to be optimized in order to meet the growing process challenges.

The First CPMT Micromouse Best Packaging Award

Submitted by Allen M. Earman, CPMT-SCV Chapter Vice-Chair

It has been years since I witnessed an IEEE Micromouse contest – many years. The Micromouse competition has been around for decades. IEEE Spectrum Magazine first introduced the microprocessor-controlled, autonomous Micromouse in 1977 with the first competition held in June 1979. I was a graduating Senior at Virginia Tech in June 1979 and the *new* Micromouse competition was a much talked about topic in the EE department that year. Back then there were no "Tips & Tricks" webpages, or even articles on the subject. Still, more than 6000 teams across the United States submitted their entries to the IEEE competition that year.

Flash forward twenty-seven years to January 2006: As the Chapter Chair for the Santa Clara Valley chapter of CPMT, I was busy putting together my Chapter Goals for 2006. Along with the usual topics of "Improve Chapter Finances," and "Increase Chapter Membership," I was looking for something new to engage the IEEE student members at the local universities. Our chapter already was quite involved at the student level as we were in the final stages of establishing a CPMT Student Chapter at San Jose State University. In April of that year, the SJSU CPMT Student Chapter received its charter as only the sixth CPMT Student worldwide and only the third in the U.S. But,…What else could we do? More importantly, "What else could we do – within the range of our local chapter capabilities?" Enter the Micromouse. I don't recall precisely from where the idea came. Perhaps I was trying to remember what excited me all those years ago as an undergrad EE student – tempered with the hoary experience of 25 years in new product development. The idea gelled. What if the Micromouse was more than an apparatus for autonomous navigation of the maze? What if the Micromouse was a New Product? What would you need to consider if you were planning to engineer the device for introduction as a consumer product? How would you design and build it?

Being an active member of CPMT and involved in the packaging and reliability of new products in my work life, several things immediately sprang to mind: power consumption, thermal management, size/weight, RFI/EMC, and quality and reliability. This might work! The Santa Clara Valley Chapter could sponsor an Award for "Best Packaging" for a Micromouse Competition! Thus, began the idea that resulted in the first CPMT Micromouse Best Packaging Award presented at the Region 6 – Central Area Spring Meeting at California State University at Chico in April 2007.

As to be expected, something like this does not happen overnight. There were many steps of intermediate accomplishment on the way to the actual prize award. First, our local CPMT chapter agreed to our stated goals for 2006. Next, I needed the support of the Director and Student Activities Chair for Region 6. This process began as a series of e-mail messages describing the concept to the Region 6 officers. Some thought it an admirable concept, others thought it would detract from the primary Micromouse competition. After a few back-and-forth messages with ever increasing length and detail, it was suggested that I produce a Formal Proposal to Region 6 Executive Committee that could be reviewed and voted upon at the next ExCom meeting. The proposal was accepted with the conditions that I also provide a complete set of contest Guidelines, Entry Form, and that our CPMT chapter – as financial sponsor of the award – transfer the funds for the award to the Region 6 treasurer at the beginning of the 2007 fiscal year so they would be available for the competition in Spring 2007.

Since the first intra-school Micromouse competition is held at the Area-level – with the winner going on to compete at the Region-level, our chapter decided to sponsor the award for our Area, the Region 6-Central Area. The Best Packaging Award would, therefore, be an additional prize for the Area competition only. After all, we are only a local chapter. There are 23 universities in the Region 6-Central Area that have active IEEE Student Branch Chapters. And more than one team can compete from each school. So, the potential for a large field of entries was high. The next step was to *get-the-word-out* to the Central Area schools. Initially, the Region 6 officers said that our Contest Guidelines and Entry Form would be posted on the Region 6 Student Activities webpage.

Early March 2007: Eight weeks to the Central Area Spring Meeting. And no posting of the Best Packaging Award information on the Region 6 webpages. Panic starts to set in!

A few more e-mail messages later and I discover that Region 6 leaves these things up to the Area Chairs. A quick search for the Central Area webpage yields a single, short, unadorned page that simply notes the date and location for the Spring Area meeting. Well, at least now I know it will be held at Cal-State Chico! But, how do we get the word out for this new contest? To my rescue – and the rescue of the Best Packaging Award for 2007 – is the Region 6 Regional Student Representative, Lise Johnston. Lise led me through the learning curve for the IEEE e-Notice announcement tool and provided me with the full list Central Area Student Branch Chapters. With this new tool in hand, I quickly distributed the Best Packaging Award Guidelines and Entry Form to all of the Student Branch members in the Central Area of Region 6 – to 14,986 student members!

Mid-April 2007: Less than two weeks to go. Time to start thinking about the logistics of judging the competition. I had generated a Judges Form for scoring the contestants back in the Fall of 2006 along with the Contest Guidelines. And the Guidelines spelled out the evaluation criteria and scoring in detail. Power consumption would be derived from the Micromouse battery configuration – number of cells and rated capacity (Ampere-hours) per cell. Special Bonus points would be awarded for use of rechargeable and recyclable batteries. Thermal management would be evaluated by measuring the hot-spot temperature of the Micromouse with an infrared temperature probe. Initially, we would measure the Micromouse at both quiescent (on, but not running), and op-