

She is a role model to others both technically and professionally, and embraces her role as mentor. She devotes endless time to mentoring – and promoting the engineering career path to technical women professionals – by providing career guidance, engineering advice, and “lessons learned.” She actively supports the development, advancement, and recognition of IBM’s technical talent. She was recognized this year for her endless drive and passion for mentoring and people development and presented with the Women in Technology “Frances E. Allen Mentoring Award.”

Her work with the Society of Women Engineers has had an inspirational effect on today’s female engineering students, and she continues to promote engineering as a superb profession for young women to enter.

Pearsall continues to support the Cockrell School of Engineering with contributions to the Friends of Alec spanning more than 20 years.

About UT's Cockrell School of Engineering:

The University of Texas at Austin's Cockrell School of Engineering ranks among the top six public engineering schools in the United States. With the nation's fourth highest number of faculty elected members of the National Academy of Engineering, the School's more than 7,000 students gain exposure to the nation's finest engineering practitioners. Appropriately, the School's logo, an embellished checkmark used by the first UT engineering dean to denote high quality student work, is the nation's oldest quality symbol. The School maintains a Web site at www.engr.utexas.edu.

Chapter Reports:

Singapore REL/CPMT/ED Chapter Update

Submitted by Alastair Trigg, Chair - IEEE Singapore Rel/CPMT/ED Chapter

On 30th October the chapter organised a technical talk on “Thermal Microsystems for Electronics Thermal Management across Multiple Scales” by Professor Suresh V. Garimella, Director of NSF Cooling Technologies Research Center at Purdue University.

Mr Li Wei a student from the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU) in Singapore won the inaugural prestige 2007 IEEE Electronic Device Society Masters Student Fellowship. Only five awards, each worth US\$2000, are given worldwide per year.

The final preparations are underway for the CPMT flagship packaging conference in Asia, the 9th Electronics Packaging Technology Conference (EPTC 2007). This is being held in Singapore 10th to 12th December. Over 250 abstracts were submitted from 19 countries, and from those the EPTC Technical Committee selected 175 papers to be presented in 34 oral and 1 poster session. On 10th December there are six short courses and two technical forums. The Conference sessions begin on 11 December with two keynote presentations by Dr Ralf Plieninger, Senior Director, Packaging at Infineon and Prof. Herbert Reichl, Director of the Fraunhofer Institute for Reliability and Microintegration. Together with the contributed papers, there are two luncheon talks and seven invited talks. There is an equipment exhibition in con-

junction with the conference Full details of EPTC can be found at the website: www.eptc-ieee.net. During the course of EPTC, IEEE Singapore REL/CPMT/ED Chapter awards will be presented to outstanding students from Nanyang Technological University and Temasek Polytechnic.



Prof. Yeo, HOD of Circuits and Systems presenting the certificate to Mr. Li Wei on September 18th, 2007



From left: Prof. Yeo, Prof. Tan Cher Ming (Li Wei's supervisor), Li Wei and Prof. Pey Kin Leong who nominated Li Wei for the award.

The chapter's flagship conference on failure analysis, the International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2008) will be held in Singapore from 7th to 11th July 2008. The call for papers is available at ewh.ieee.org/reg/10/ipfa/ The deadline for abstracts is **18th January 2008**. In 2008 IPFA will be holding its first Photo Contest – *the Art of Failure Analysis 2008*. In addition to the popular IPFA equipment exhibition, there will be an additional opportunity for company promotion through sponsorship packages. Information on all aspects of IPFA is available on the website.

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www.cpmt.org/newsletter/

CPMT United Kingdom & Republic of Ireland (UK & RI) News

Submitted by Nihal Sinnadurai, Chapter Chair CPMT UK & RI
& Executive Chair ESTC-2008

In the UK & RI we have worked with a clear focus on the “customers” i.e. the members and engineers in our field who are interested in the activities we have planned over the years. To this end, we have worked with like-minded institutes in arranging conferences, seminars, tutorials and events in support of students. We have co-sponsored the many annual MicroTech events and Electronics Manufacturing Forums held in the UK.

The most constructive regional development which also benefits other Chapters in Region 8, is the collaboration agreement reached with IMAPS-Europe, whereby CPMT runs a biennial conference namely the Electronics System-Integration Technology Conference (ESTC-2008) in odd years, and IMAPS-Europe runs its European Microelectronics Packaging Conference (EMPC) biennially in the even years, with both being co-sponsored. This deal is now actively running and ESTC-2008 - to be held during 1-4 September 2008 at Greenwich, London - will be the first such collaborative CPMT Conference. CPMT UK&RI, which provided leadership as architect of the collaboration agreement, is in the heart of ESTC-2008.

We would like to see whole-hearted participation by Electronics Engineers and especially CPMT members in ESTC-2008.

ESTC-2008 will be held at Greenwich, the Prime Meridian and magnificent World Heritage and major maritime site on the banks of the River Thames in the great city that is London. The Conference and Exhibition will be hosted at the University of Greenwich in the buildings of the former Royal Naval College – which has a tremendous heritage: the Exhibition Hall will be immediately over the former palace of King Henry the Eighth, and the Queens House is where Sir Walter Raleigh placed his cloak over a puddle for Queen Elizabeth the First to step onto. Plenary sessions will be in the Great Painted Hall – providing a wonderful ambience for the technical presentations. The exhibition will be the quality event in microelectronics and micro-systems in Europe in 2008.



Greenwich, Prime Meridian and World Heritage Site

The Technical themes of ESTC-2008 are: • Advanced Packaging • Emerging Technologies • Manufacturing and Test Technology • Modelling, Simulation and Design • New Materials and Processes • Power Electronics • Technology & Reliability for Micro and Nano Systems • Assembly of Alternative Energy Sources • Optoelectronics • Electronics system-integration for healthcare.

There will be Special Sessions on:

• Greening the Blue Planet • Standards • Prognostics and Health Monitoring • Asia-Pacific Photovoltaics Developments • European Global Business Council

The Technical Committees are in place, the Call for Papers has been widely disseminated, invitations to exhibit have been sent to many companies globally and a brand new enduring website created. Please check out the website www.estc.biz. For General information contact: info@estc.biz or sinnadurai@estc.biz. For Exhibition and R&D Village bookings contact Carole Franks or Susanne Wolf at intercomm@dial.pipex.com.

Conference Reviews:

EDAPS 2007: A Workshop on Electrical Design of Advanced Packaging and Systems

Prof. Tzong-Lin Wu, National Taiwan University, Taipei, Taiwan

The 2007 EDAPS conference was held at National Taiwan University, Taipei, Taiwan from Dec. 15th to 18th, 2007. The conference was hosted by the Department of Electrical Engineering, Graduate Institute of Communication Engineering, and Center of Information and Electronics Technology, National Taiwan University, and was sponsored by the National Science Council, IEEE, IEICE, and leading companies in advanced packaging. The participants came from Canada, Hong Kong, Italy, Japan, Korea, Singapore, Taiwan, and the US (in alphabetical order). The number of attendees reached 271, including 27 invited speakers, which is a new record for EDAPS. Among the attendees, 49% are from academia and 51% from industry, which marks a great success in bridging academia and industry together.

The first day started with three tutorials on Signal Integrity, Power Integrity, and SiP Design, given by Mr. Moises Cases (IBM, USA), Prof. Madhavan Swaminathan (Georgia Tech, USA), and Prof. Joungho Kim (KAIST, Korea), respectively. Totally, 146 attendees signed in, including around 70 students and 60 engineers from local industry. On the second and third day, there were three featured keynotes, one luncheon talk, and twenty-three invited talks. The three talks were: “Global Paradigms, Models & Challenges” by Prof. Rao R. Tummala (Georgia Tech, USA), “3D Package Technology Integration” by Dr. Ho-Ming Tang (ASE Group, Taiwan), and “Meeting the Design Challenges Associate with SIP and IC/Package/PCB Co-Design” by Dr. Zoltan Cendes (Ansoft, USA). The luncheon talk was “Academic and Industrial Research: Using the IEEE’s XPLORE Database” by Dr. Paul Wesling. The invited talks covered the hottest topics including chip/system level design, electromagnetic simulation, electro-thermal analysis, integrated passive devices, as well as efficient yet accurate modeling techniques. On the fourth day, the invited speakers took the Taiwan High-Speed-Rail train (300 Km/hr at its highest speed) to Kaohsiung to visit ASE groups, which is the largest provider in assembly and test in the world. The feedback to the EDAPS 2007 committee were very positive. Many partici-