CPMT United Kingdom & Republic of Ireland (UK & RI) News

Submitted by Nihal Sinnadurai, Chapter Chair CPMT UK & RI & Executive Chair ESTC-2008

In the UK & RI we have worked with a clear focus on the "customers" i.e. the members and engineers in our field who are interested in the activities we have planned over the years. To this end, we have worked with like-minded institutes in arranging conferences, seminars, tutorials and events in support of students. We have co-sponsored the many annual MicroTech events and Electronics Manufacturing Forums held in the UK.

The most constructive regional development which also benefits other Chapters in Region 8, is the collaboration agreement reached with IMAPS-Europe, whereby CPMT runs a biennial conference namely the Electronics System-Integration Technology Conference (ESTC-2008) in odd years, and IMAPS-Europe runs its European Microelectronics Packaging Conference (EMPC) biennially in the even years, with both being co-sponsored. This deal is now actively running and ESTC-2008 - to be held during 1-4 September 2008 at Greenwich, London - will be the first such collaborative CPMT Conference. CPMT UK&RI, which provided leadership as architect of the collaboration agreement, is in the heart of ESTC-2008.

We would like to see whole-hearted participation by Electronics Engineers and especially CPMT members in ESTC-2008.

ESTC-2008 will be held at Greenwich, the Prime Meridian and magnificent World Heritage and major maritime site on the banks of the River Thames in the great city that is London. The Conference and Exhibition will be hosted at the University of Greenwich in the buildings of the former Royal Naval College – which has a tremendous heritage: the Exhibition Hall will be immediately over the former palace of King Henry the Eighth, and the Queens House is where Sir Walter Raleigh placed his cloak over a puddle for Queen Elizabeth the First to step onto. Plenary sessions will be in the Great Painted Hall – providing a wonderful ambience for the technical presentations. The exhibition will be the quality event in microelectronics and micro-systems in Europe in 2008.

Greenwich, Prime Meridian and World Heritage Site

The Technical themes of ESTC-2008 are: • Advanced Packaging • Emerging Technologies • Manufacturing and Test Technology • Modelling, Simulation and Design • New Materials and Processes • Power Electronics • Technology & Reliability for Micro and Nano Systems • Assembly of Alternative Energy Sources • Optoelectronics • Electronics system-integration for healthcare.

There will be Special Sessions on:
• Greening the Blue Planet • Standards • Prognostics and Health Monitoring • Asia-Pacific Photovoltaics Developments • European Global Business Council

The Technical Committees are in place, the Call for Papers has been widely disseminated, invitations to exhibit have been sent to many companies globally and a brand new enduring website created. Please check out the website **www.estc.biz**. For General information contact: **info@estc.biz** or **sinnadurai@estc.biz**. For Exhibition and R&D Village bookings contact Carole Franks or Susanne Wolf at **intercomm@dial.pipex.com**.

Conference Reviews:

EDAPS 2007: A Workshop on Electrical Design of Advanced Packaging and Systems

Prof. Tzong-Lin Wu, National Taiwan University, Taipei, Taiwan

The 2007 EDAPS conference was held at National Taiwan University, Taipei, Taiwan from Dec. 15th to 18th, 2007. The conference was hosted by the Department of Electrical Engineering, Graduate Institute of Communication Engineering, and Center of Information and Electronics Technology, National Taiwan University, and was sponsored by the National Science Council, IEEE, IEICE, and leading companies in advanced packaging. The participants came from Canada, Hong Kong, Italy, Japan, Korea, Singapore, Taiwan, and the US (in alphabetical order). The number of attendees reached 271, including 27 invited speakers, which is a new record for EDAPS. Among the attendees, 49% are from academia and 51% from industry, which marks a great success in bridging academia and industry together.

The first day started with three tutorials on Signal Integrity, Power Integrity, and SiP Design, given by Mr. Moises Cases (IBM, USA), Prof. Madhavan Swaminathan (Georgia Tech, USA), and Prof. Joungho Kim (KAIST, Korea), respectively. Totally, 146 attendees signed in, including around 70 students and 60 engineers from local industry. On the second and third day, there were three featured keynotes, one luncheon talk, and twenty-three invited talks. The three talks were: "Global Paradigms, Models & Challenges" by Prof. Rao R. Tummala (Georgia Tech, USA), "3D Package Technology Integration" by Dr. Ho-Ming Tang (ASE Group, Taiwan), and "Meeting the Design Challenges Associate with SIP and IC/Package/PCB Co-Design" by Dr. Zoltan Cendes (Ansoft, USA). The luncheon talk was "Academic and Industrial Research: Using the IEEE's XPLORE Database" by Dr. Paul Wesling. The invited talks covered the hottest topics including chip/system level design, electromagnetic simulation, electro-thermal analysis, integrated passive devices, as well as efficient yet accurate modeling techniques. On the fourth day, the invited speakers took the Taiwan High-Speed-Rail train (300 Km/hr at its highest speed) to Kaohsiung to visit ASE groups, which is the largest provider in assembly and test in the world. The feedback to the EDAPS 2007 committee were very positive. Many partici-

pants would like to attend EDAPS again in the future and will recommend EDAPS to their colleagues.

The chairman of EDAPS 2007, Prof. Ruey-Beei Wu, on behalf of the executive committee, would like to thank all the attendees, especially Dr. Alina Deutsch and Prof. Madhavan Swaminathan, the TC-12 EDMS Committee co-Chairs of IEEE CMPT Society, for their kind support in every aspect, which made EDAPS 2007 a wonderful experience. Meanwhile, Prof. Joungho Kim assumes the chairmanship of EDAPS 2008, which will be held in Seoul, Korea from Dec. 10th to 12th, 2008. Regarding the EDAPS 2008 information, please visit **www.edaps2008.org** for details.

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Technical Committee Reports:

TC-1 News from 2007

TC-1: Technical Committee on Electrical Contacts, Connectors, and Cable

Submitted by Dr. Dave Palmer, IEEE Fellow

The scope of this Committee is to be the focal point within the IEEE CPMT Society for electrical contacts, electrical connectors, and interconnecting cable. Its membership consists of individuals having an interest in the research, development, manufacture, and utilization of electrical contacts and devices that contain them. The Committee holds regularly scheduled meetings and functions through the Holm Organization and through task forces having specific objectives. The Committee sponsors or supports conferences, publications, educational, standardization, and other activities.

The 2007 IEEE Holm Conference on Electrical Contacts was held in Pittsburgh, September 17-19. This was the 53rd Annual conference in North America where professionals presented and discussed the latest developments in the field of electric contacts. This year there were 130 attendees and this resulted in a very successful conference.

The technical program had 35 presented papers in 9 sessions, the Ragnar Holm Award Lecture and the Mort Antler Invited Lecture. Papers were presented on electric contacts in switches, relays and connectors, new contact materials and coatings, arc fundamentals, thermal models, finite element analysis and corrosion. A special session was organized on Arc Fault Circuit Interrupter (AFCI). This is a new NEC standard to be implemented in all new residential house constructions in 2008. More details of the program and abstracts can be found in our web site.

On Monday night (9/17), we also had a successful social event at the Pittsburgh Grand Concourse, a restored train station with perfect atmosphere for friendly discussions while dining. The annual Monday social event is becoming a tradition when the conference attendees get to chat more freely with their conference friends. We had 96 attending the dinner social.

This year, the conference presented 3 awards:

a. The 2007 Ragnar Holm Scientific Achievement Award to Professor Ji Gao Zhang, Beijing University of Posts & Telecommunication, for his life time work on dust and electrical contact reliability, as well as his teaching contributions in China. He gave an award lecture "Effect of Dust Contamination on Electrical Contact Failure".
b. The 2007 Mort Antler Lecture Award to Professor Joachim Heberlein, University of Minnesota, who was the invited speaker to stimulate work on hot topics. His lecture was titled "The Characterization of the Dynamic Arc-Anode Interaction and Using Plasma Deposition of nanocomposites to Tailor Material Properties.
c. The 2006 IEEE Erle Shobert Prize Paper to Dr. John Shea, Eaton Corporation, for his paper "Glowing Contact Physics" being selected as the best out of 43 papers presented in the 2006 conference in Montreal.

TC-1 also runs a 3 day intensive course on electrical contacts bi-annually. The course has been very successful in teaching engineers the physics and practice of contact designs and selections. It is a favorite for switch, relay, circuit breaker, contactor, and connector engineers from automotive, power distribution and telecommunication fields. The 2006 course was held in Montreal and the 2008 course will be held in Orlando just before the Holm Conference.

The 2008 IEEE Holm Conference will be October 27-29 in Orlando. For more information on many special events organized by this committee such as annual IEEE Holm conference, conference presentation downloads, intensive course, international conference, CD-ROM library and link to other societies, please visit our web site at **www.ewh.ieee.org/soc/cpmt/tc1**.

Photo Gallery from 2007 IEEE Holm Conference ===>

Mort Antler Lecturer Prof. Heberlein and Tech. Comm. Chair Dr. Zhou

2007 Holm Award Prof. Zhang (L) & Conference Chair Dr. Shea (R)

2006 Prize paper Dr. Shea (L) & Prize Paper Chair Dr. Taylor (R)

ASTR 2007 Review

Submitted by Mark R. Chrusciel, ASTR Publicity Chair

The ASTR 2007 workshop on Accelerated Stress Testing and Reliability was recently held in the Washington DC area. This years theme was "Accelerated Life Testing, it's Roles, Challenges, Attributes, and Interaction with Qualification Testing".

Over the last few years, Accelerated Stress Testing (AST) has been embraced by an ever widening array of worldwide companies seeking to reconcile the need for the highest quality product with the necessary push for early time-to-market. The purpose of the AST Workshop is to share ideas on better ways of accelerating and detecting hidden defects, flaws, and weaknesses in electronic and electro-mechanical hardware that would result in failures during usage. Feedback from this years conference was very positive.

Plans are being made for ASTR 2008 to be held in Portland, Oregon in October of 2008. Theme and call for papers to be issued in the spring.

ASTR 2007 Committee

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58th Electronic Components and Technology Conference (ECTC) Update

Submitted by Dr. Rajen Dias, Asst. Program Chair

The 58th ECTC that will be held at Disney's Contemporary Resort in Lake Buena Vista, Florida, USA May 27 to 30, 2008, has received 616 technical abstracts, a record number. The technical program will feature over 300 high quality technical papers, presented in 36 oral sessions, two poster sessions and a special student poster session. The papers cover a wide spectrum of topics: advanced packaging, interconnections, electronic components, materials, processing, assembly, manufacturing, optoelectronics, quality and reliability, modeling, simulation and emerging technology that focuses on nano-technology, biomedical and flexible electronics.

The technical program is complemented by 16 professional development courses, a plenary session, a panel discussion session and a CPMT seminar session. In addition, there is a technical exhibit corner where over 50 leading companies, primarily in the electronics components, materials, thermal and packaging fields exhibit their latest technologies and products. The conference allows ample opportunities to network and meet leading experts in the field.

For more information on 58 ECTC, please visit **www.ectc.net**

Workshop Reviews:

6th Future Directions in IC and Package Design (FDIP 2007) Workshop

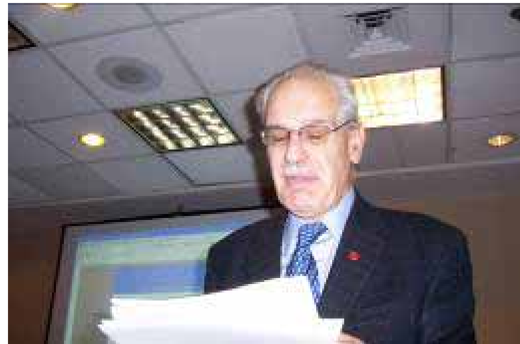
Organized by CPMT Technical Committee on Electrical Design, Modeling, and Simulation, TC-EDMS

October 28, 2007, Atlanta, Georgia

Submitted by Alina Deutsch, IBM T. J. Watson Research Center, Tel: 914-945-2858, email:deutsch@us.ibm.com, co-chair

Madhavan Swaminathan, Georgia Institute of Technology, email: madhavan.swaminathan@ece.gatech.edu, co-chair

This year's workshop was held on October 27, 2007, in Atlanta, Georgia. This was the sixth year for the meeting but it was still very well attended, with 60 participants. The workshop was divided into two sessions, namely System Design, and Power Distribution. The two sessions were chaired by George Katopis from IBM and Gregory Taylor from Intel. As in years past, the presenters were all invited distinguished experts in the field and this year's contributors gave excellent presentations.



George Katopis, IBM

Gregory Taylor, Intel

The System Design session was opened by **Dale Becker** from IBM who presented the talk "Signal Bandwidth for High Performance Computing". Dale defined a new system performance metric, the product of the number of bits in the off-chip signal bus and the data rate. Key issues he foresaw were the need for memory bandwidth increases, a factor of ten increase in Gbps/cm^2 due to increase in density of pins and data rate; power delivery and heat removal become more challenging; containing power distribution effective impedance and signal integrity in the presence of multiple power domains; self heating in I/O pins; importance of core noise in addition to Delta-I noise; ability to design advanced analog loss compensating circuits for drivers and receivers; and time and frequency domain analysis capability for jitter assessment for full channel. Dale saw processor clock frequencies leveling off, off-chip frequencies increasing as number of cores is go-

ing up, ASIC clock frequencies rapidly increasing. Designers need to use full-wave analysis for power distribution and via stub reflections, careful DC analysis to control electromigration, have good understanding of compensating receiver circuits, have good tools to perform optimal chip-package co-design and use common interfaces across companies to reduce cost per pin. Dale saw the cost per pair of differential I/O increasing by a factor of two when going from 3 Gbps to 10 Gbps.

Dale Becker, IBM

Prof. Tadahiro Kuroda from Keio University presented a very nice overview of 3D package interface methods, "Wireless Proximity Communications for 3D System Integration". He made a very compelling argument why inductive coupling is superior to capacitive and TSV (through silicon via) approaches. Inductive coupling has been successfully shown for 1000 I/O's with 1 Gbps data rate and 1 TBps total throughput and only 0.14 pJ per bit. Inductive coupling can be used through the silicon substrate even for thickness as high as 60um and thus multiple chips can be easily stacked without restriction on chip face orientation as found in capacitive coupling.

Capacitive coupling relies on a single metal layer while L-coupling inductors can utilize several on-chip layers and thus have higher efficiency. Prof. Kuroda indicated that this is a much lower energy solution (2 mW) than wire bonding (200 mW) or micro-bumping (20 mW) and still can have very high density of 1 mm^2/Tbps. TSV needs much higher real estate due to the use of ESD protection that is not needed by L-coupling. The resultant 3D stack is much thinner than when using TSV and has very high reliability of 10^{-13} BER. Alignment tolerances are not critical and the cost of L-coupling versus TSV development is much lower since no new technology is needed. L-coupling allows non-contact testing and AC coupling across various power levels. Extendability of this technology is gated by ability to thin the stacked chips and placement of the I/Os with respect to power mesh and density inside the on-chip wiring that could cause some interference. Time interleaving can be used for thicker chips or to increase effective I/O density.

Prof. Kuroda, Keio University

Professor Jayathi Murthy from Purdue University introduced the audience of electrical engineers to the modeling of thermal effects on-chip with her presentation "A Critical Assessment of the State of the Art in Multiscale Multiphysics Modeling of Microelectronics". She indicated that sub-micron thermal physics are generally not included in present day electro-thermal device simulations. When phonons' mean free path becomes comparable to transistor channel dimension, ballistic phonon effects become critical for hot-spot prediction. Thermal resistance of interfaces and surface physics are dominating as device sizes are dropping. Electro-thermal-mechanical analysis is becoming increasingly important but is currently not available. The solution she offered is to create compact models that account for local effects accurately that can be then included in CAD tools and allow to bridge from microscale to macroscale analysis. Such new tools are absolutely necessary as leakage may account for as much as 40% of total power dissipation. Sub-threshold leakage currents increase exponentially with temperature and can lead to thermal runaway. For every 10°C increase in temperature, a MOSFET's drive current decreases about 4% and interconnect delay increases approximately 5%. Because of all these penalties, electronics thermal management is emerging as a critical bottleneck that dictates the need for new tool development.

Prof. Murthy, Purdue University

Tawfik Arabi from Intel presented "Designing for Energy Efficient Mobile Platforms". He indicated that for laptops, Intel's goal is to reduce power by 10W between generations of products. Designers have made good progress in containing the CPU power which is 47% of total but then other factors such as voltage regulator, memory, power delivery are affecting the total power of the platform. A 10 W reduction can allow a 0.1 inch reduction in laptop thickness and Tawfik thought this was significant. He also noted that a 20% reduction in clock frequency leads to a 50%

drop in power consumption. The newer device technologies with metal gate and high *k* such as the 45 nm node show a reduction in f_{max} tolerance for the device. A large improvement in processor power reduction was obtained by introducing temperature gradient distribution across the die in the timing CAD tools. This was doable by partitioning the die into mega-blocks and then performing accurate modeling within the blocks and only global analysis at the chip level.

The remaining challenges are primarily at the platform level, such as the I/O power delivery sub-systems, I/O signaling, voltage regulators, that show impact for light load conditions, such as in idle state.

Dr. Tawfik Arabi, Intel

Prof. Swaminathan, GIT

Professor Madhavan Swaminathan from Georgia Institute of Technology presented "Modeling Challenges for Power Distribution Analysis". He traced the modeling activities from the early 1990's to today. He reviewed the various techniques used, how the simple effective impedance analysis of yesterday needs to be extended to a multi-scale chip-package co-design capability. He felt that low K material use results in increased electromigration exposure, especially at the interposer interface, managing coupling from high density digital circuits into the sensitive analog circuits is increasingly difficult, modeling of frequency dependent losses while predicting time-domain jitter needs new tool development. A new approach to solving the Courant condition was found at GIT by using Laguerre FDTD. This allows to easily handle scale ratios of $1{:}10^6$. Small 3D package vias show significant current density variation due to skin effect and proximity effect. Mobile platforms that use embedded passives encounter large vertical coupling through the partitioned power system. It was felt that many modeling tools are not addressing the issue of causality and this effects the timing prediction for fast signal propagation on long interconnects.

The last talk was given by the founder of Sigrity, **Prof. Jiayuan Fang**, "Power Delivery System Design Challenges and Explorations on How to Overcome Them". Prof. Fang felt that power distribution systems, PDS, modeling tools are now used by over 100 companies. There are still a lot of challenges, however. Most companies do not have design specifications for the power delivery systems. The designers cannot formulate the needed voltage fluctuations, the available chip current, the target impedance for PDS, the current switching conditions, the applicable frequency range. It is then hard to define the optimal location and number of power and ground vias, location and types of decoupling capacitors needed. This can lead to product failures or gross over-design with unnecessary cost.
Guidelines were given on how to establish design specifications for PDS, such as the use of a database storing previous generation product characteristics. New optimization facilities were also shown for best selection and placement of decaps to improve performance and reduce cost.

Prof. Fang, Sigrity

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2nd International Workshop on 3D System Integration Munich, Bermany

Submitted by Mr. Rolf Aschenbrenner, VP Conferences, IEEE CPMT Society

The 2nd International Workshop on 3D System Integration took place on 1-2 October 2007 at the Fraunhofer-Society, Munich, co-organized by IEEE CPMT. More than 90 engineers, scientists and entrepreneurs attended the 2-day workshop and discussed world-wide R&D activities, perspectives and challenges of 3D integration.

After the welcome and introduction by Peter Ramm, Fraunhofer Munich, the keynote address was given by Sitaram Arkalgud, director of SEMATECH (US), on "Paving the Roadmap For Through Silicon Vias". The first day continued focussing on Si-based technologies for 3D IC integration with excellent talks by speakers from ZyCube (Japan), STMicroelectronics (Italy) , EPFL (Switzerland), NXP (Netherlands), SINTEF (Norway), Semitool (US), IBM (Switzerland), CEA-Leti (France) and Fraunhofer IZM (Munich). After the opening talk of Robert Darveaux, Amkor (US), on "Developments of 3D Packaging" the second day´s talks

were given by speakers from AT&S (Austria), Techlead (US), Imbera (Finalnd), ASE (US), IMEC (Belgium), Schweizer Electronic (Switzerland), Panasonic (Japan) and Fraunhofer IZM (Berlin).

Picture: Speakers and chairs at the IEEE Workshop on 3D System Integration Munich 2007 (sitting right: Keynote speaker Dr. Sitaram Arkalgud (SEMATECH); row left and center, respectively: Chairman Dr. Peter Ramm and co-chair Rolf Aschenbrenner (Fraunhofer IZM))

2nd IEEE International Workshop On Advances in Sensors and Interfaces

IWASI 2007

Held 26/27 June 2007 - Bari, Italy

IWASI is a sensors interfaces conference, aimed at bridging the gap between sensor devices and their integration with electronics using newly developed technologies. The workshop focus is on the development of the electronics around the sensors so that efficient sensors can create a system that can easily be placed in the home, the car, or on the human body to improve the quality of life.

The Workshop provides a forum for the exchange of ideas and results in critical areas of design for quality in deep submicron era. Focus areas: • Sensor interfaces • New materials and new technologies for sensors • Sensor modeling and design techniques • Sensors for space, nuclear and particle physics, biomedical, automotive, environmental and other applications • Optoelectronic and photonic sensors • MEMS and MOEMS-based sensors • Post-processing electronics • Noise reduction techniques in sensors interfaces • Testing techniques for sensors systems • Sensor networks.

Photos from the 2007 IWASI

Prof. Daniela De Venuto being interviewed (left) and with the Mayor of the City and the Chancellor of the Politecnico of Bari (below)

Please review the papers from the 2007 IWASI in IEEE's IEL/Xplore system:

ieeexplore.ieee.org/xpl/RecentCon.jsp?punumber=4419989

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2008 IEEE

Systems Packaging Japan Workshop

Hotel de YAMA, Hakone, Japan

January 28 - 30, 2008

www.ewh.ieee.org/soc/cpmt/tc14/

Submitted by Evan Davidson, Japanese Liaison for TCSP

Call for Papers and Invitation

The Systems Packaging Japan Committee cordially invites you to participate in the 2008 IEEE Systems Packaging Japan Workshop (2008 SPJW), which will be held during January 28-30, 2008 at the Hotel de YAMA, Hakone, Japan. This workshop is held every other year in Japan and 2008 SPJW will be the twelfth one since the first workshop in 1986. State-of-the-art technologies in all areas of systems packaging from personal systems to high performance systems will be covered. Attendees are expected to be specialists in the field and to actively participate in all discussions. We look forward to meeting many of you at Hakone.

Topics:

● IT Network Systems ● Digital Consumer Products & Mobile Information Systems ● High Performance Servers ● Advanced Packaging & Components ● Bio/Nano Technologies ● Environmental Aspects

For more information about the workshop, please feel free to contact Mr. Kishio Yokouchi, the Program Chair at:

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Fujitsu Interconnect Technologies Ltd.,
E-mail: yokouchi.kishio@fict.fujitsu.co