Voids at Cu / Solder Interface and Their Effects on Solder Joint Reliability

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Acknowledgement:
Bala Nandagopal, Sue Teng, and Diana Chiang

Background (Literature)

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- Microvoids are present at the interfaces of Cu / solders (62Sn-36Pb-2Ag, Sn-3.5Ag, Sn-37Pb, Sn-3.5Ag-0.5Cu) after aging at 190°C for 100 h, 150°C for 500 h, even 100°C for 720 h. Higher aging temperature, faster voids grow.
- Kirkendall effect was attributed. Faster diffusion of Cu than Sn.
- Effects on solder joint reliability:
  - Impact strength reduced from 90 to 5 after 10 d @ 125°C.
  - Shear strength reduced little, fracture mode changed to interface.
  - Pull strength reduced more significantly than shear strength but less than impact strength.
  - Fractured most inside Cu_6Sn_5 not in Cu_3Sn.
- No voids in Sn-3.5Ag / Cu (rolled), a lot in Sn-3.5Ag/Cu (E'lytic).

Ref:
1.M.Date and K.N. Tu at UCLA, ECTC 2004, p. 668
2. T.-C. Chiu, et al, Texas Instrument, ECTC 2004, p. 1256
3. W. Yang and R. W. Messler, Jr., J. Electronic Materials, Vol. 23, (1994), p. 765
4. S. Ahat, et al, J Electronic Materials, Vol. 30, (2001), p. 1317.

Outline of This Work

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- X-sections of solder joints of various conditions
- Mechanical shock of high temperature aged BGA assemblies; Lead pull test.
- Estimate the risk for poor solder joint, based on Chiu et al data

BGA from ??? of ENIG Finish Attached to Motherboard with OSP Pads, Baked 20 days @ 125°C, Board Side

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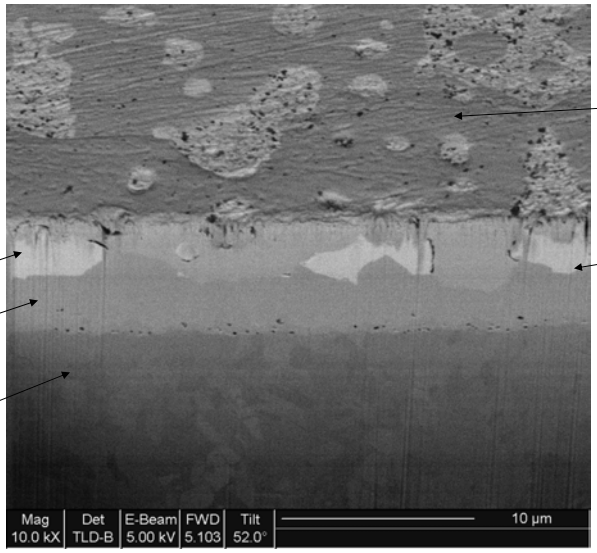

X-section by FIB (focus Ga^+ ion beam). A slow and costly method

Same joint shown the previous slide

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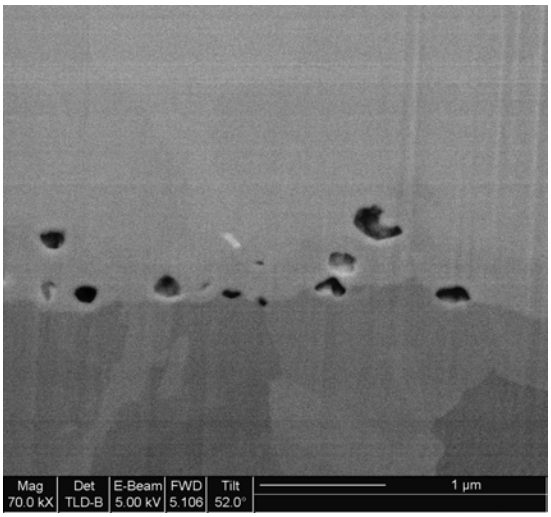

Voids are not tunnels, or pipes. They have about equal size in all three dimensions

One or two layer IMC?

Same joint shown the previous slide

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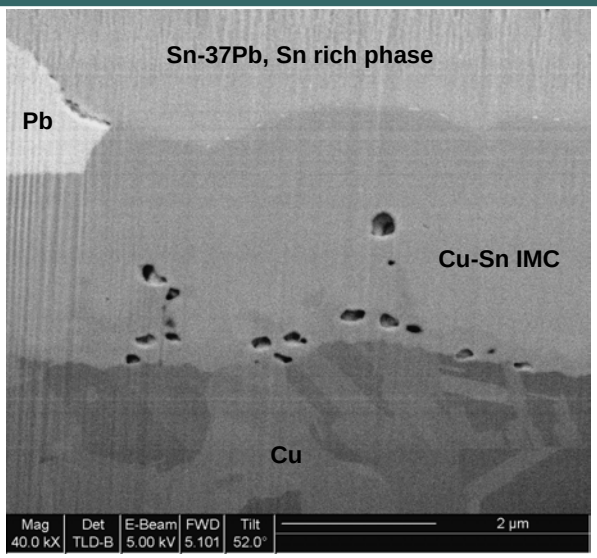

Voids are about 0.2 µm size, inside Cu-Sn IMC, close to Cu

The Same Joint, but on Package Side: ENIG

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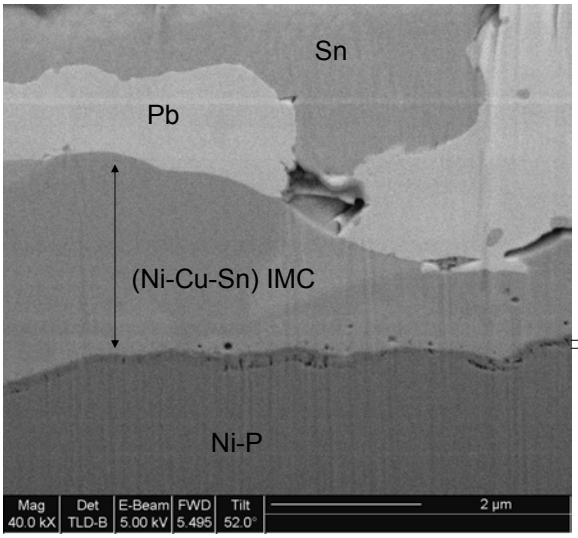


-**Some voids in the Ni-Cu-Sn IMC, and the P-enriched layer.**

-**The interface IMC contains Cu after baking, not before the baking.**

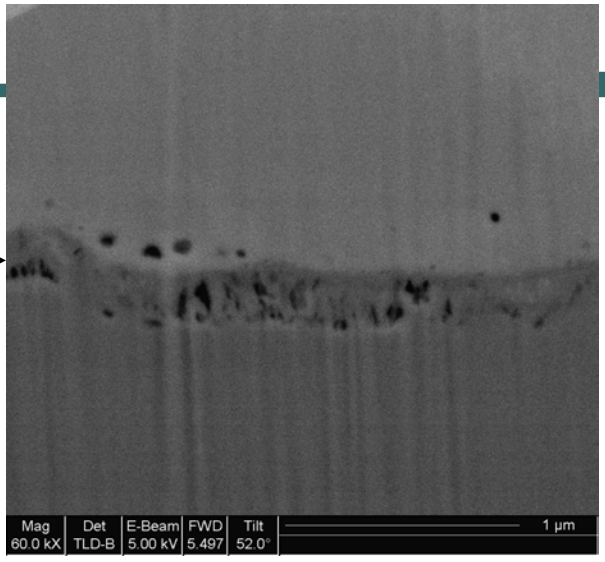
Phosphorus enriched layer

Same Sample

Ni-Cu-Sn IMC

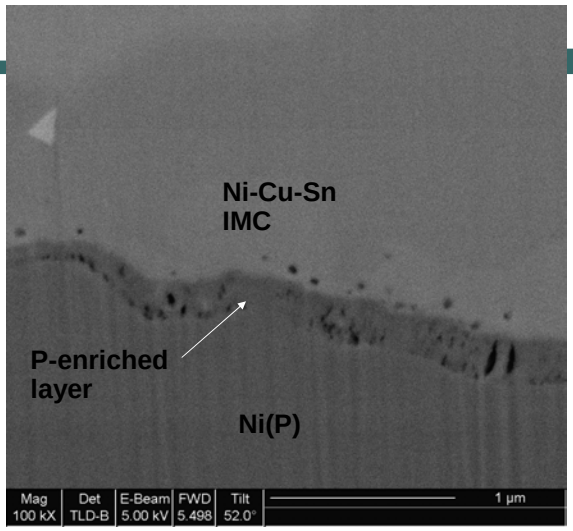
P-enriched layer

Ni(P)



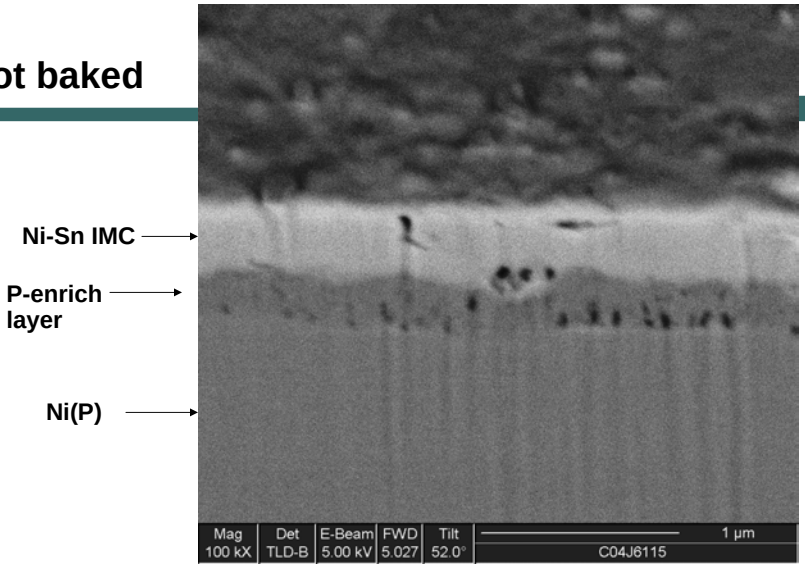
Voids are seen both inside the phosphorous enriched layer and inside the Ni-Cu-Sn IMC.

Same Sample



Another area. Most voids at ENIG side is much smaller in size, ~0.05 µm.

Not baked



The voids are present at the package side (ENIG) before the baking, similarly reported by Goyal et al (ECTC 2002). But the voids at PCB side (OSP Cu) are not before the baking.

Same type BGA shown previous slides, but with SOP finish, attached to motherboard with OSP pads, baked 20 days @ 125°C, board side

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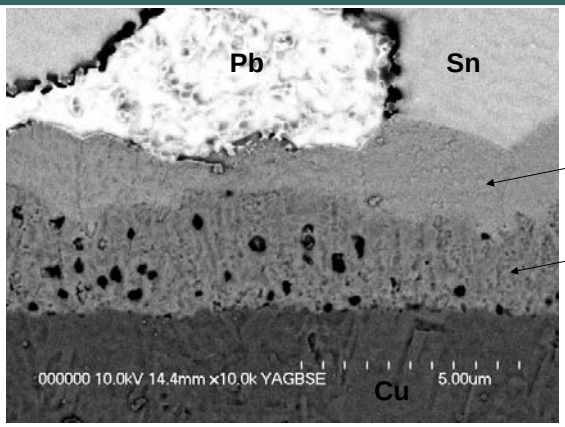

-Sample was lightly etched by Ar ion to remove the surface layer due to polish. A quick and low cost method than FIB.

Same type BGA and same thermal history, as shown in the previous slide

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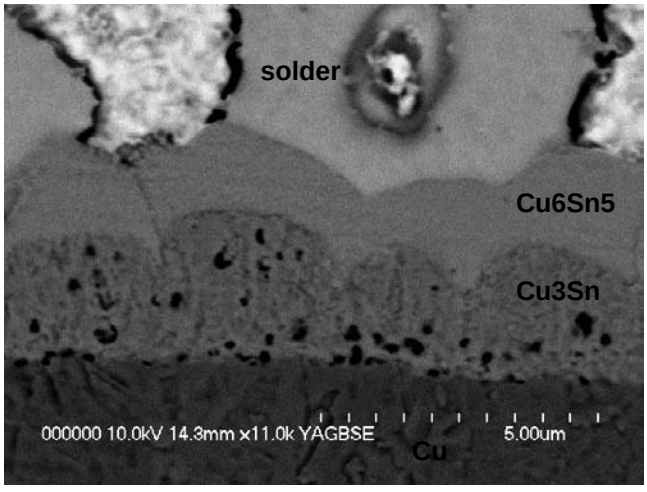

- Not all voids are aligned at the Cu_3Sn / Cu interface, some are at interior of Cu_3Sn, different from Chiu and Date
- Cu_3Sn and Cu_6Sn_5 have the same wave pattern

BGA from NEC with SOP Finish Attached to Motherboard with OSP Pads, Baked 20 days @ 125°C, **Board Side**

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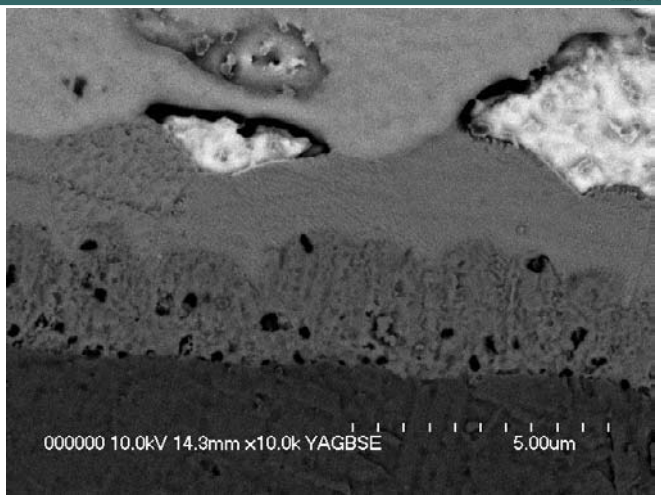

In Chiu's paper, voids at the interface reached 70% of the joint interfacial area after 20 d @ 125°C. Here at most, 30%. Considering three dimensions, the voided area may be only 9%.

Same joints as in the previous slide, package side: SOP

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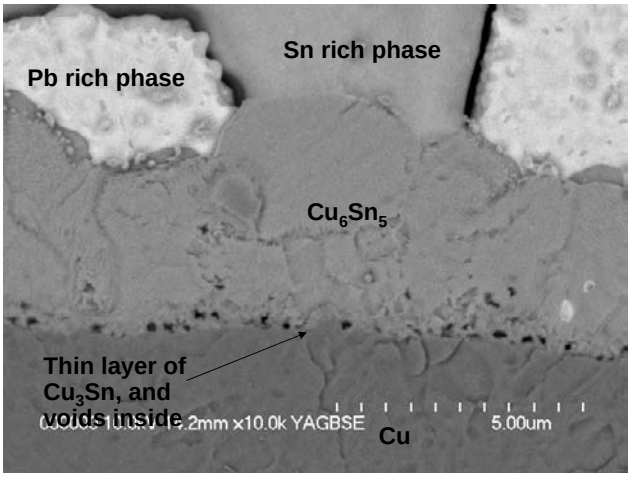

On the package side, the Cu_3Sn layer is very thin. Fewer voids, confined within the Cu_3Sn layer.

Sn-Pb bump on Laminated Cu (not Electroplated), Baked 20 days @ 125°C

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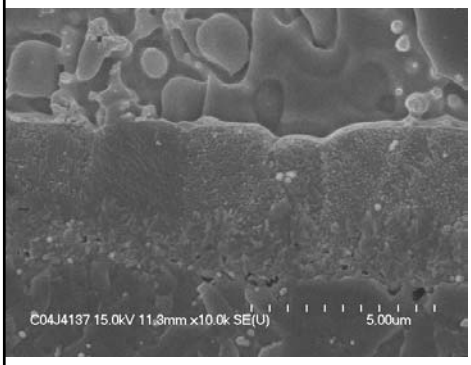
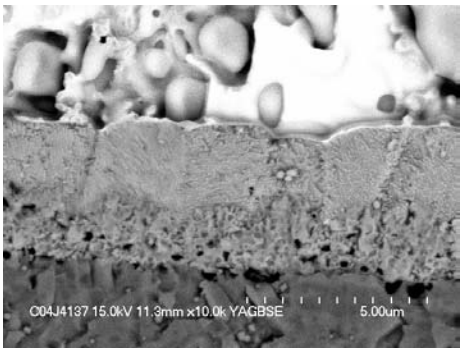


2nd electron image



backscattering electron image

Yang et al (J. Electronic Mater., Vol. 23, (1994), reports that voids occur only in electroplated Cu, not in cold rolled Cu. Here we have a laminated Cu (non-electroplated). We see voids . Also voids are better seen in backscattering electron image than in 2nd electron image, as shown here.

Sn-Pb bump on Laminated Cu (not Electroplated), Baked 20 days @ 125°C

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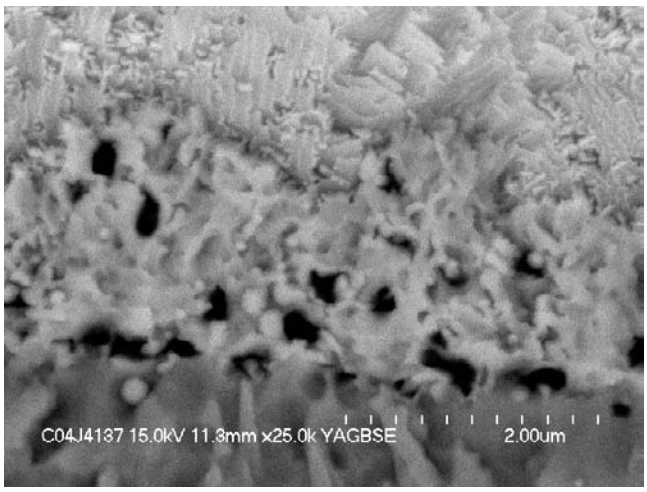

Zoom in, backscattering electron image. The sample is over-etched

Alloy 42 lead, coated 2 um Cu, plated Sn-1Bi solder. Baked 5 days @ 145°C

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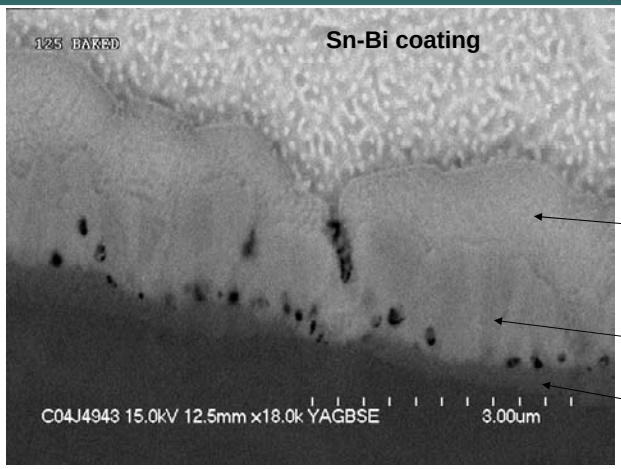

1. Voids are seen in Cu_3Sn
2. Cu_3Sn and Cu_6Sn_5 are 1.5 µm thick each.
3. There seem some residue Cu left

Alloy 42 lead, coated 2 um Cu, plated Sn-1Bi solder. Baked 5 days @ 145°C

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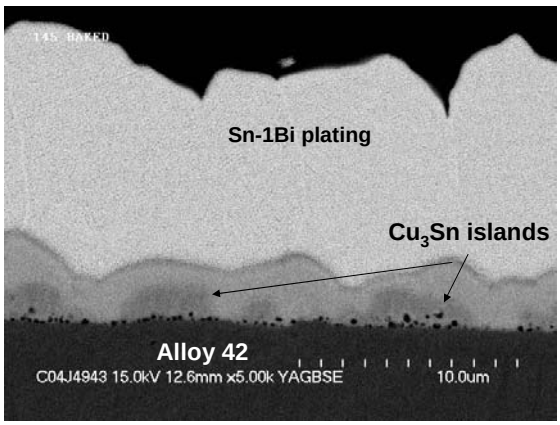

1. **Voids are exclusively inside Cu_3Sn.**
2. **Cu_3Sn appears as islands, usually it is a continuous layer. It may be due to the limited supply of Cu.**

Alloy 42 lead, coated 2 um Cu, plated Sn-1Bi solder. Baked 5 days @ 145°C

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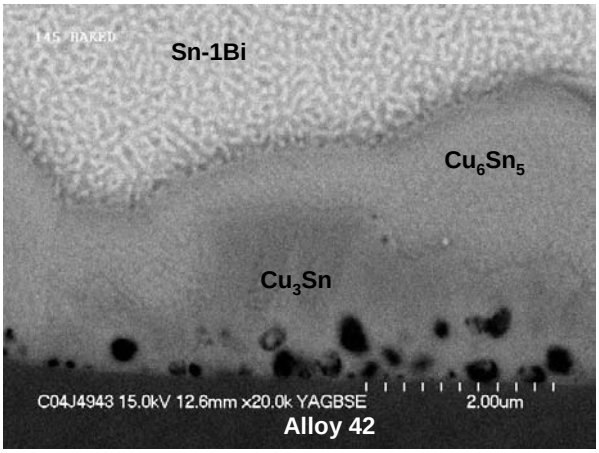

Alloy 42 lead, coated 2 um Cu, plated Sn-1Bi solder. Baked 5 days @ 125°C

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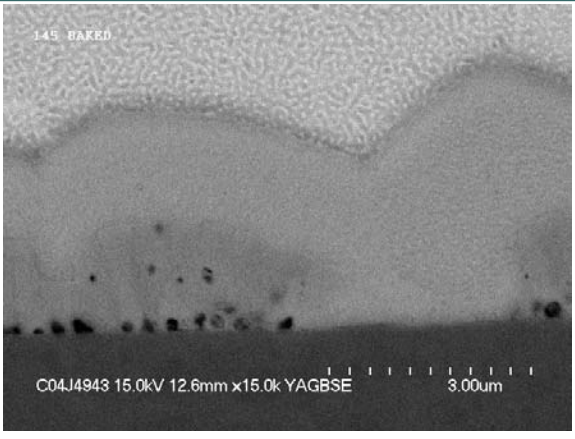

Voids are only present inside Cu_3Sn islands. See here, there is no voids outside the Cu_3Sn islands.

Alloy 42 lead, coated 2 um Cu, plated Sn-1Bi solder. Baked 5 days @ 125°C

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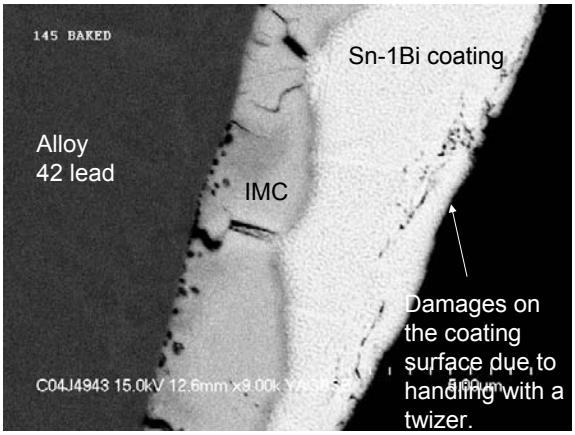

This photo shows cracks inside the IMC due to handling. The cracks started from the voids inside Cu_6Sn, and extended through Cu_6Sn_5, and stop at the Cu_6Sn_5 / Sn-1Bi coating interface.

Exactly the same component, but it is Sn-Pb Coated Cu Alloy Lead, 5 days at 145°C

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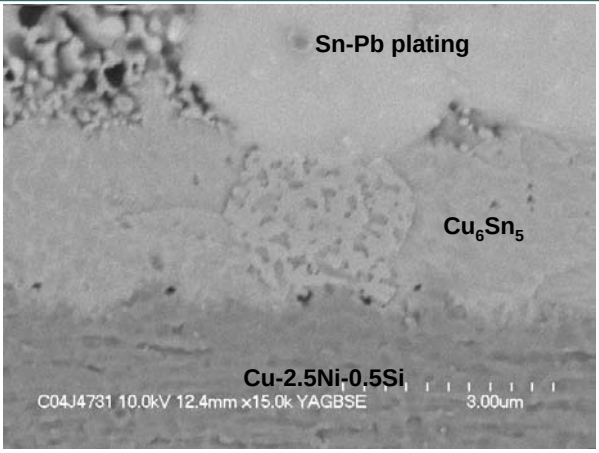

Very few voids at the interface.
The interfacial intermetallic is mostly Cu_6Sn_5, Very thin Cu_3Sn layer.
There are minor Ni composition in IMC.

Sn-Pb Coated Cu Alloy Lead, 5 days at 145°C

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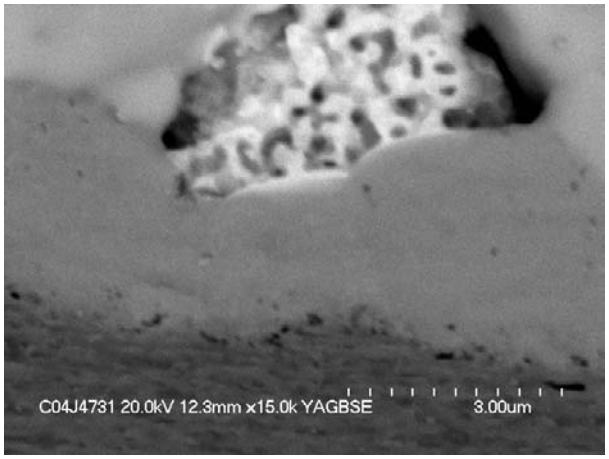

Very few voids at the interface, also Cu_3Sn is not visible

Sn-Pb Coated Cu Alloy Lead

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- Lead frame:
  97wt% Cu, 2.6 wt% Ni, and 0.5 at% Si
- 2nd layer IMC (close to solder)
  55 at% Cu, 1.5 at% Ni, 43.5 at% Sn => Cu_6Sn_5 structure
- Very thin 1st layer of IMC
- The Ni may suppress the formation of Cu_3Sn
- Lead frame Cu alloy is not electroplated, which may be attributed to the few voids

OSP / SAC solder / Electrolytic Ni, -25C ⇔ 125C, 2000 cycles, OSP / SAC side

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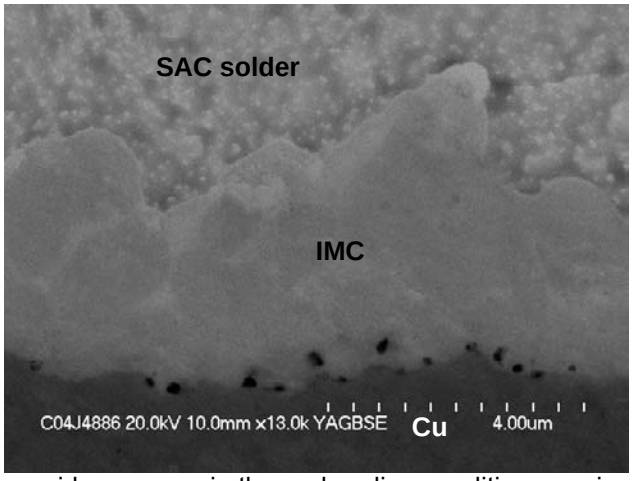

- Here, voids are seen in thermal cycling condition, previously voids were reported in isothermal baking.
- Two shades at the interface are two IMCs

OSP / SAC solder / Electrolytic Ni, -25C ⇔ 125C, 2000 cycles, OSP / SAC side

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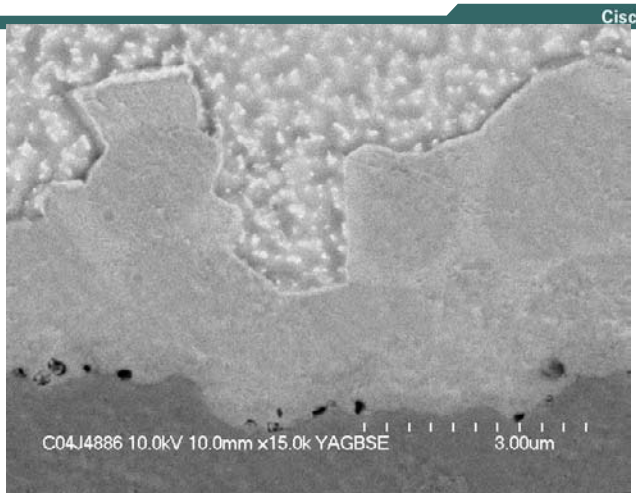

The temp profile had a 5 min ramping from -25°C to 125°C, 15 min dwell at 125°C, 5 min ramping to -25°C. The accumulated time at 125°C in 2000 cycles is about 20 days. Chiu's data suggests a 70% voided area.

Matte Sn over Cu-3Ni lead, attached onto motherboard (OSP), -40 ⇔125°C, 500 cycles, board side

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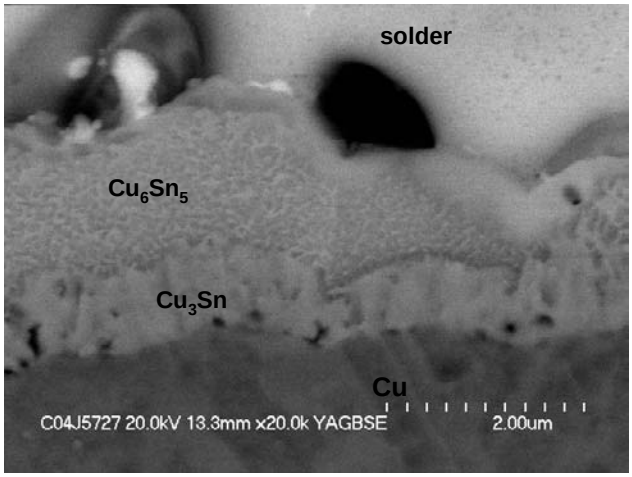

-Voids and Cu_3Sn are present on the board pads
- Couldn't detect any Ni in Cu-Sn IMC.

Matte Sn over Cu-3Ni lead, attached onto motherboard (OSP), -40 ⇔125°C, 500 cycles, lead side

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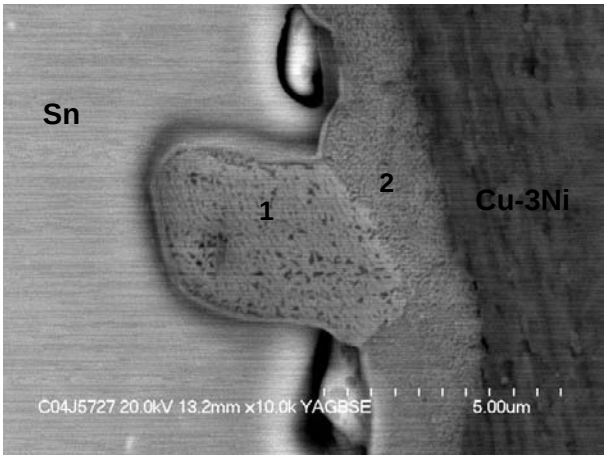

Neither voids nor Cu_3Sn on the lead side
Area 1: 57.7 at%Cu, 43.3 at% Sn
Area 2: 54.7 at%Cu, 1.2 at% Ni, 44.1 at% Sn

Matt Sn over Cu-3Ni lead, attached onto motherboard (OSP), -40 ⇔125°C, 500 cycles, lead side

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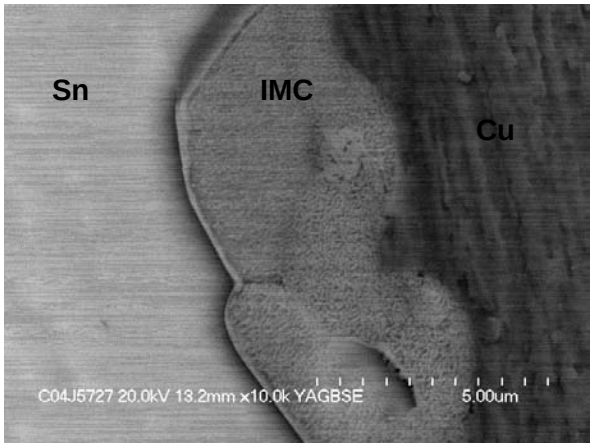

The Ni atoms in the lead frame suppress the formation of Cu_3Sn, and therefore the formation of voids.

Matt Sn over Cu-3Ni lead, attached onto motherboard (OSP), -40 ⇔125°C, 500 cycles

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- Lead:
  97.27 wt% Cu, 2.73 wt% Ni
- Matrix:
  93.4 wt% Sn, 5.5 % Pb, 0.77 wt% Cu
- IMC at PCB side:
  1st layer: 58 at%Cu, 42 at% Sn
  2nd layer: 83 at% Cu, 17 at% Sn
- IMC at lead side:
  one layer: 57.9 at% Cu, 1.25 at% Ni, 40.85 at% Sn

Shock Testing Set up

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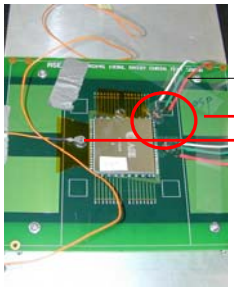
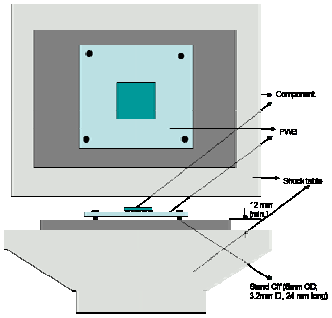


Shock Set-up

5'X5' Configuration

Strain Gages

Accelerometers



Package on board

Board mounted to the base plate by stand offs

Base plate secured to the Shock table

Insitu daisy chain monitoring of package during shock test

Acceleration and Strain Response

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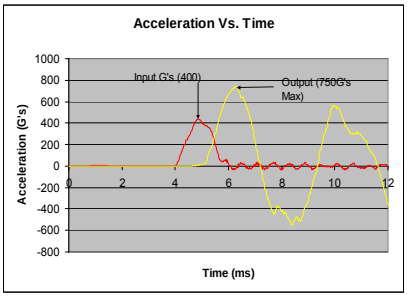
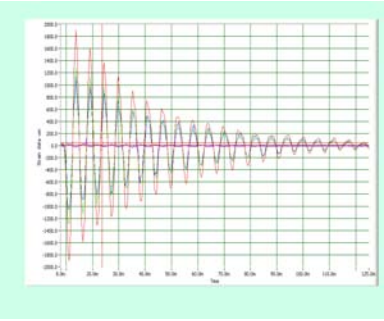


Strain Data Vs. Time



Max. Principal strain ~ 1900 us

Shock test repeated 6 times with no failures

BGA of SOP Finish Attached to Motherboard with OSP Pads, Baked 20 days @ 125°C

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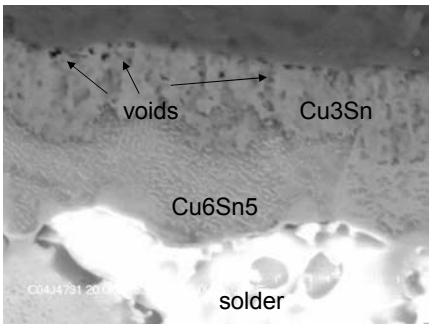
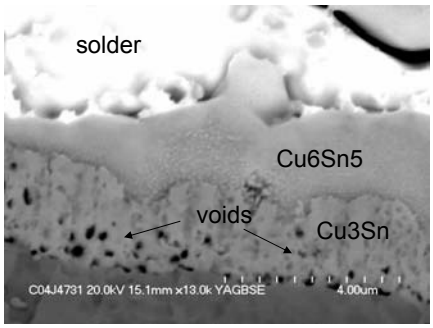
Pkg side interface



Brd side interface



There seem more voids at the board / solder interface than at the pkg / solder interface

BGA of SOP Finish Attached to Motherboard with OSP Pads, Baked 20 days @ 125°C, shocked 6 times at 400g.

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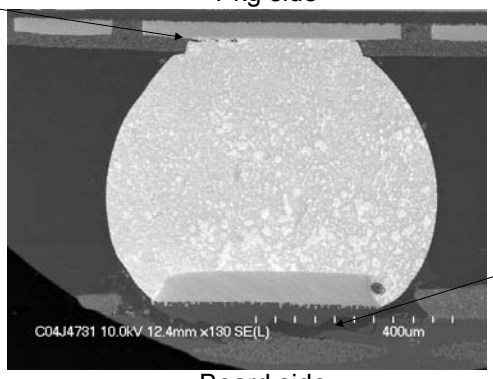
Cracked inside solder, close to the solder/pad interface

Pkg side



Delaminated under the pad, resin/glass interface

Board side

Cracked at two locations: (1) Pad on the motherboard side, delaminated at the glass / resin interface. (2) inside solder close to IMC at pkg side, in the solder mask defined area.

The vast amount of voids in IMC at the board side are not the weakest links in the shock

BGA of SOP Finish Attached to Motherboard with OSP Pads, Baked 20 days @ 125°C, shocked 6 times at 400g.

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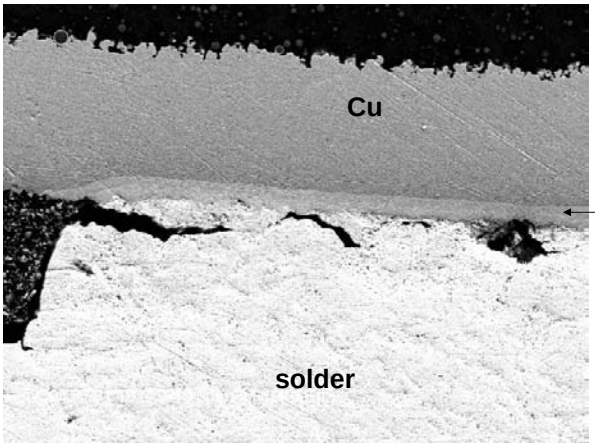

Crack within solder, not in IMC. The crack path is preferentially at boundaries between Sn-rich phase and Pb rich phase.

Matte Sn over Cu-3Ni lead, attached onto motherboard (OSP), -40 ⇔125°C, 500 cycles. Pulled lead.

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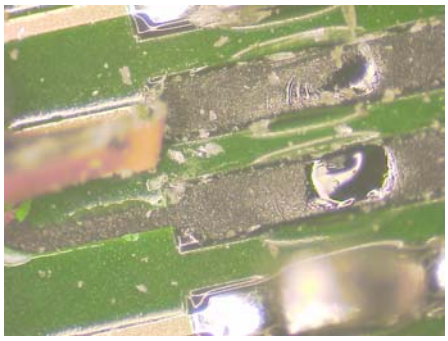
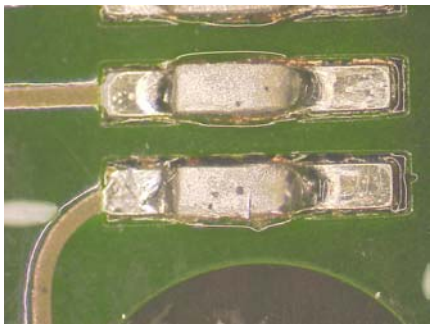


As-soldered, pad peeled off



After ATC, pulled at the interface of solder / lead

Matt Sn over Cu-3Ni lead, attached onto motherboard (OSP), -40 ⇔125°C, 500 cycles. Pulled lead.

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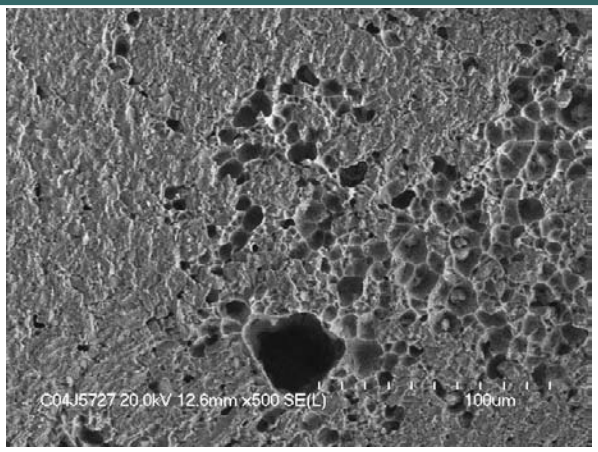

Toe side, interfacial fracture **Lead side, dimples**

As shown in previous slides, the voids are present at PCB/solder interface, not at lead/solder interface. But the failure here occurred at the lead/solder interface.

Matt Sn over Cu-3Ni lead, attached onto motherboard (OSP), -40 ⇔125°C, 500 cycles. Pulled lead.

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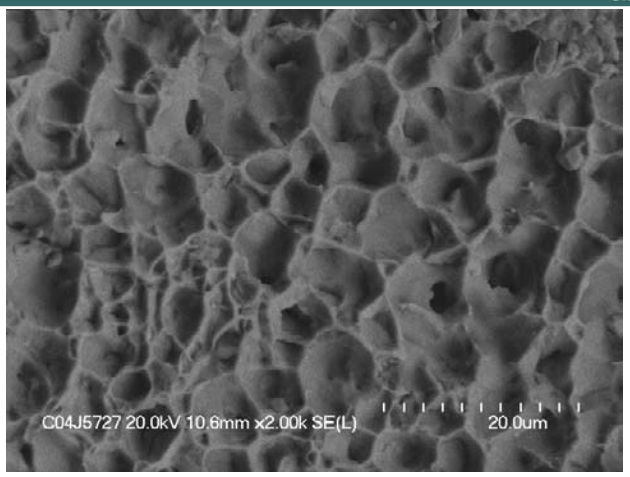

Dimples, classic plastic deformation

Matt Sn over Cu-3Ni lead, attached onto motherboard (OSP), -40 ⇔125°C, 500 cycles. Pulled lead.

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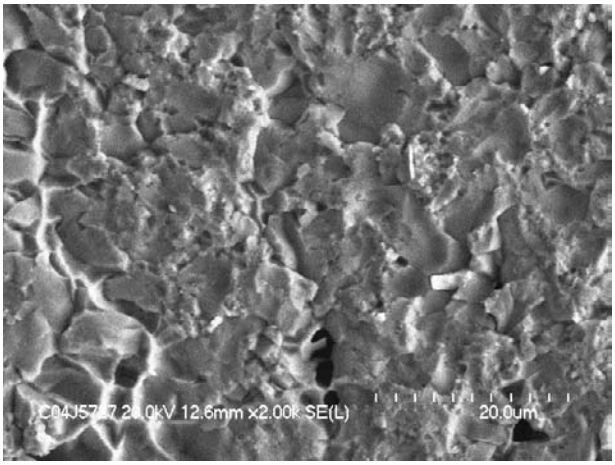

Brittle interfacial fracture at the interface between lead and solder
Fracture surface: 55.2 at% Cu, 1.2 at% Ni, 44.6 at% Sn => Cu_6Sn_5

Summary of SEM X-section

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- Voids are seen in high, low, or even zero densities among these samples. The void density relates to the formation and thickness of Cu_3Sn IMC; voids are confined inside Cu_3Sn.
- The voided area is not as much as that observed by Chiu et al for the same baking conditions
- Voids are seen in thermal cycling condition, as well as in isothermal baking condition.
- Voids are seen in non-electroplated Cu.
- Ni atoms in lead frame may suppress the formation of Cu_3Sn, and the voids.

Summary of Mechanical Tests

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- Shock: the voids in the IMC layer on the board side are not weakest links in the shock test. The weakest link in ??? BGA packages is either the pads or the solder mask defined portion of solder joint.
- Lead Pull: didn't occur at the voided interface (PCB/solder). The lead/solder interface is the weakest link.

Curve-fit Chiu's Void vs Aging Data: Results

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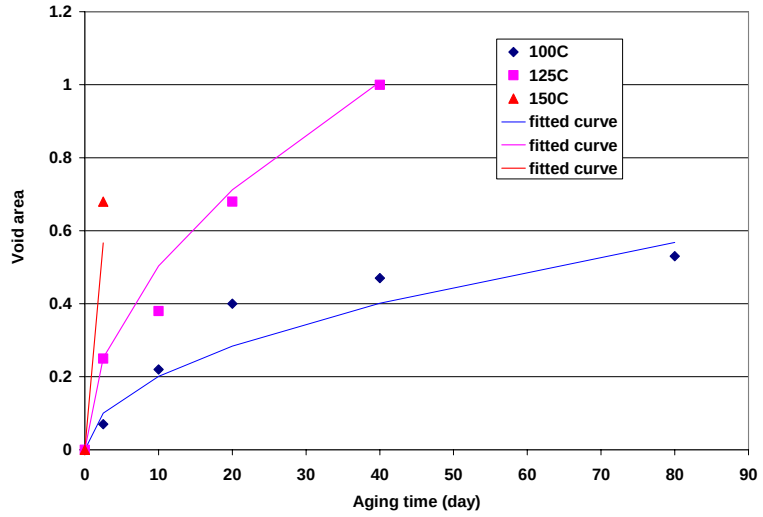

Curve-fit Chiu's Void vs Aging Data: Equation

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- Assume:
  A = C t^0.5 exp(-Q/RT)
  A: ratio of voided area to the joint area
  t: time in days
  T: temperature in K
  R: Gas constant
- Result of curve fitting:
  Q (activation energy) = 0.47 eV
  C = 145590 (day$^{0.5}$)
- Prediction:
  At 50°C, for reaching 50% of voided area, it needs about 6000 days, or 16.5 years.

Screening Test

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- $A_1 = C\ t_1^{0.5} \exp(-Q/RT_1)$
  $A_2 = C\ t_2^{0.5} \exp(-Q/RT_2)$
  $A_1 = A_2$
  $t_2/t_1 = \exp[2G/R\ (1/T_2 - 1/T_1)]$
- 15 years at 50°C is equivalent to 4.8 days at 140°C.
- Bake BGA at 140°C for 4.8, then shock test at (e.g. 200G).
- Either no failure, or the failure location is not at the solder / pad interface, pass.

Conclusions

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- Voids exist at the interface between Cu pad / solders. The density of the voids does not depend only on baking condition, but also on Cu plating and minor alloy element (e.g. Ni).
- The effects on the solder joint impact strength, according to this initial study, is not significant.
- Accelerated baking may be used to screen the bad assemblies.