


DIMENSIONAL IMPRINT TECHNOLOGY

IMPRINT PATTERNING

Dr. Craig Davidson
CTO



Why Imprint Patterning ?

*Imprint Patterning*TM addresses two well recognized shortcomings of printed circuits today:

Circuit Density & Cost

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Concept & Technology

The Problem

- A. A growing performance gap between interconnect requirements driven by semiconductor advances and the performance of printed circuit boards

“VLSI designers will face three crises in the coming years: the power crisis, *interconnection crisis*, and the complexity crisis” (JSAP Intl., #3, 2001)

“There is an increased awareness...that packaging is becoming a differentiator in product development” (ITRS, 2001)

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Concept & Technology

The Problem

- B. Printed circuit board performance is limited by the yield/cost ratios of a maturing interconnect industry.


“The U.S. PWB strategy...has been one of incremental change...technology investment has not been a primary consideration.” (ITRI 5000, 1999)

“No significant improvement in hole to pad registration, outer layer minimum line/space, soldermask registration, impedance control.” (“A Case Study of Supplier Capabilities”, Evans, IPC Conf., Sep, 2002)

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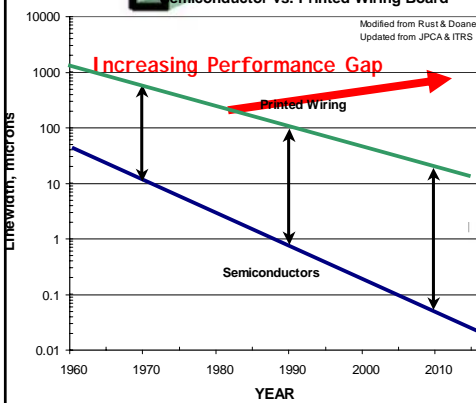


Mature PCB Technology

LINEWIDTH CAPABILITIES

Semiconductor vs. Printed Wiring Board

Modified from Rust & Doane
Updated from JPCA & ITRS



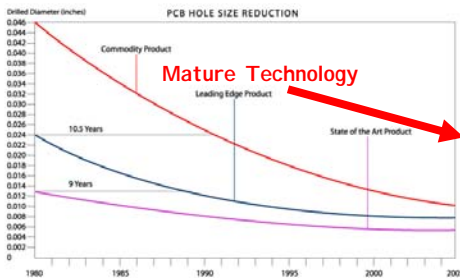
Increasing Performance Gap

Printed Wiring

Semiconductors

“VLSI designers will face three crises in the coming years: the power crisis, **interconnection crisis**, and the complexity crisis” (JSAP Intl., #3, 2001)

“We have **reached the limits** of traditional approaches to Packaging.” (“Key Messages”, ITRS, Dec 2004)



PCB HOLE SIZE REDUCTION

Mature Technology

Drilled Diameter (inches)

Commodity Product

Leading Edge Product

State of the Art Product


10.3 Years

9 Years

YEAR

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Concept & Technology

Photolithography & Laser Drilling:


both are fundamental PCB fabrication processes. And, both contribute *significantly* to density constraints, cost, and yield loss.

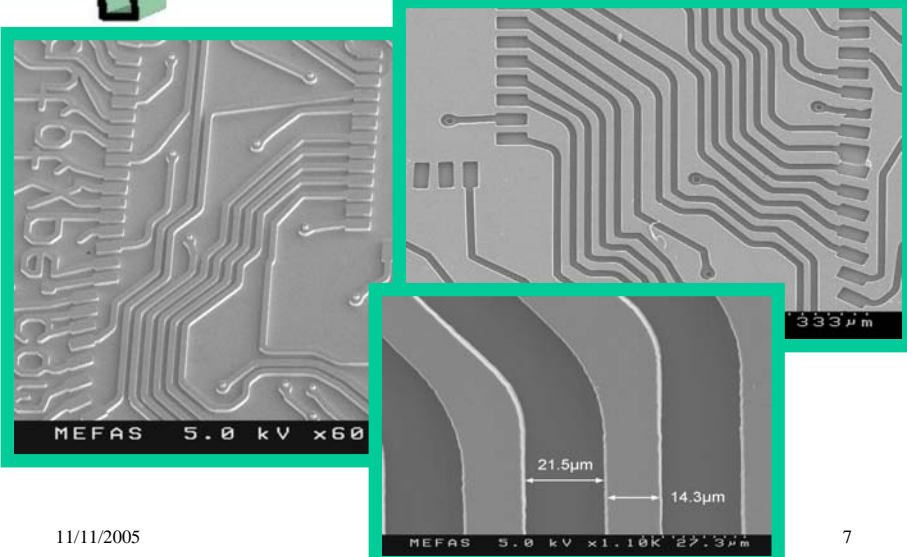
Imprint Patterning

replaces photolithography and laser drilling with a simple, cost-effective microreplication step.


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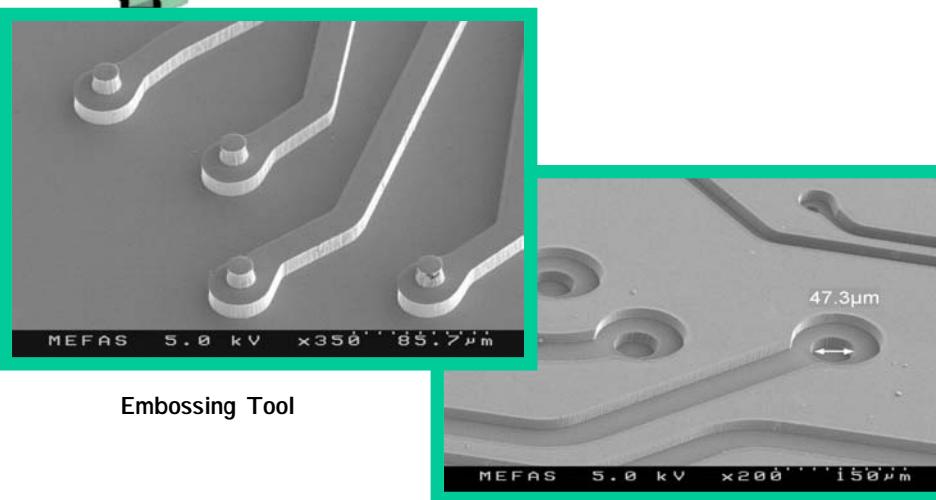
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 **HDI Toolfoil & Imprint**



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 **HDI Microvias**



Embossing Tool

Embossed Dielectric

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Cost Benefits

- 25-60% reduction in process costs
 - Reduction in process steps
 - Materials' savings
 - Eliminate equipment (capital investment)
 - Reduced facilities requirement (e.g. clean rooms)
- Reduced cycle times (improved cash conversion cycle)
- Reduced environmental impact !!
 - Less Power, Less Water, Less Waste

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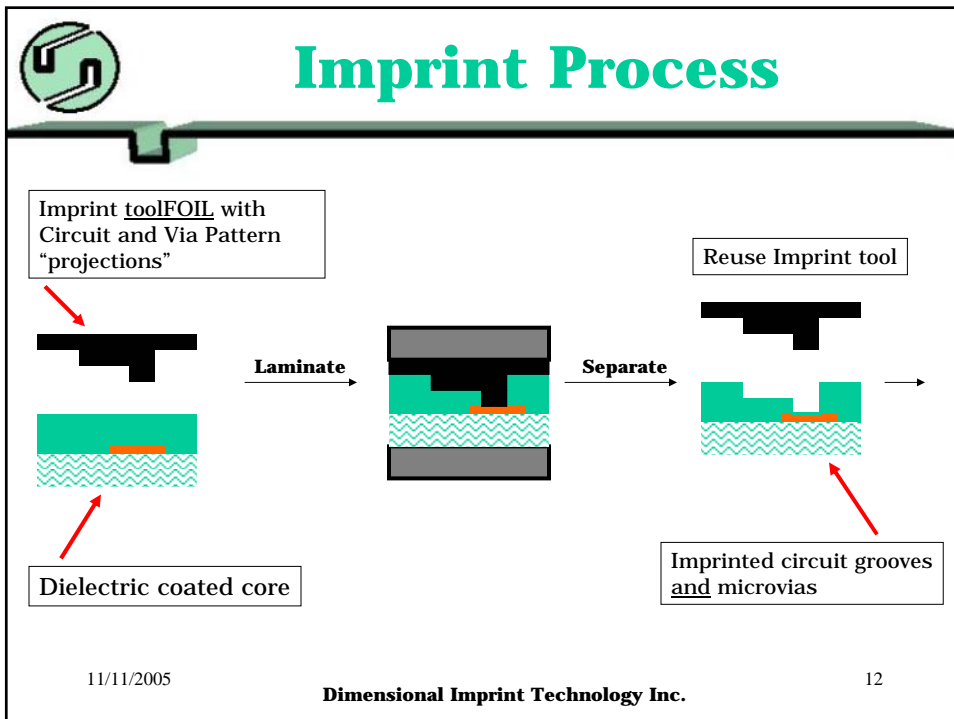
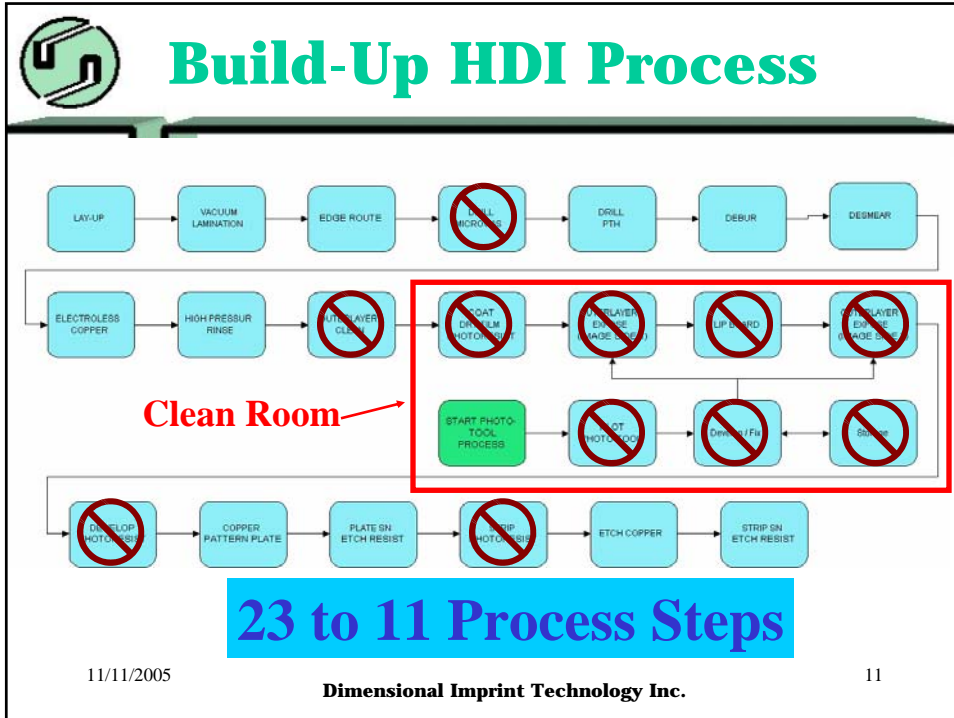
Performance Benefits

- ~40% increase in wiring density (cm/cm²) with significantly improved yields (i.e. high quality)
- Reduced tolerance on line characteristics and impedance (better circuit performance; reduced variation)
- Reduced electrical parasitics
 - Eliminate capture/target pads
 - Reduce trace discontinuities through design
 - Higher via-density capability (power & ground distribution)
- Precision electrical elements
 - Filters, inductors, delay lines, etc.

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Imprint Process (cont.)

The diagram illustrates two steps of the imprint process. In the first step, labeled "Desmear", a substrate with a patterned surface is shown. A thin layer of material is being removed from the surface. In the second step, labeled "Metallize", the same substrate is shown with a thicker, uniform layer of material being deposited over the entire surface, covering the previously removed areas.

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Metallization Method: Full Build Cu


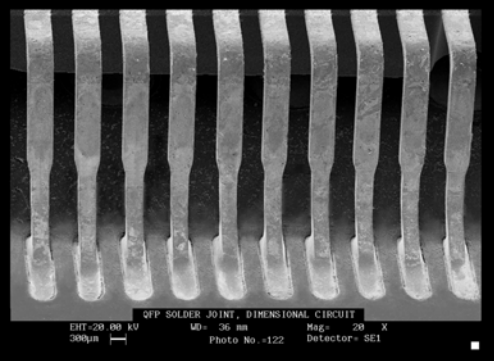
The diagram illustrates the steps of the Full Build Cu metallization method. It starts with a substrate having a patterned surface. The process involves several steps: 1. Electroless Cu: A thin layer of copper is deposited on the surface. 2. Electrolytic Cu: A thicker layer of copper is deposited on top of the electroless copper. 3. Squeegee etch resist: A blue resist layer is applied and then etched away, leaving a patterned resist. 4. Etch Cu: The copper is etched away from the areas not covered by the resist. 5. Strip Resist: The remaining resist is stripped away, leaving a patterned copper surface.

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Imprinted Circuit Pads

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Intellectual Property

Inventor	Doc. No.	Issued	Claims
G. Gregoire	RE38,579	2004	45
G. Gregoire	6,460,247	2002	19
G. Gregoire	6,005,198	1999	24
G. Gregoire	5,451,722	1995	1 (CIP)
G. Gregoire	5,390,412	1995	18
G. Gregoire	5,391,353	1994	
G. Gregoire	5,334,279	1994	14
F. Parker	4,912,844	1990	19

148 Citations in the Patent Literature

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