DIMENSIONAL IMPRINT TECHNOLOGY

IMPRINT PATTERNING

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CTO

Why Imprint Patterning ?

Imprint Patterning™ addresses two well recognized shortcomings of printed circuits today:

Circuit Density & Cost

Concept & Technology

The Problem

A. A growing performance gap between interconnect requirements driven by semiconductor advances and the performance of printed circuit boards

> "VLSI designers will face three crises in the coming years: the power crisis, ***interconnection crisis***, and the complexity crisis" (JSAP Intl., #3, 2001)
>
> "There is an increased awareness...that packaging is becoming a differentiator in product development" (ITRS, 2001)

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Concept & Technology

The Problem

B. Printed circuit board performance is limited by the yield/cost ratios of a maturing interconnect industry.

> "The U.S. PWB strategy...has been one of incremental change...technology investment has not been a primary consideration." (ITRI 5000, 1999)
>
> "No significant improvement in hole to pad registration, outer layer minimum line/space, soldermask registration, impedance control." ("A Case Study of Supplier Capabilities", Evans, IPC Conf., Sep, 2002)

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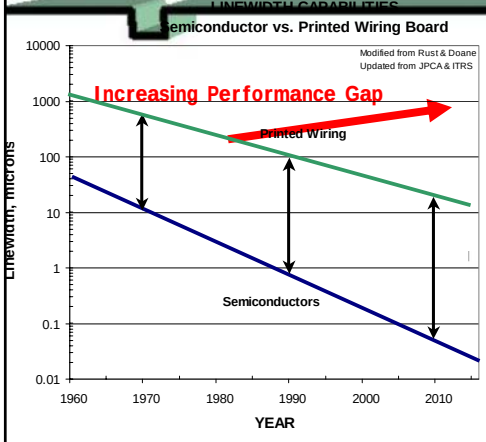
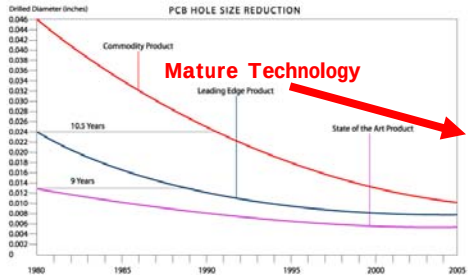
Mature PCB Technology



"VLSI designers will face three crises in the coming years: the power crisis, **interconnection crisis**, and the complexity crisis" **(JSAP Intl., #3, 2001)**

"We have **reached the limits** of traditional approaches to Packaging." **("Key Messages", ITRS, Dec 2004)**

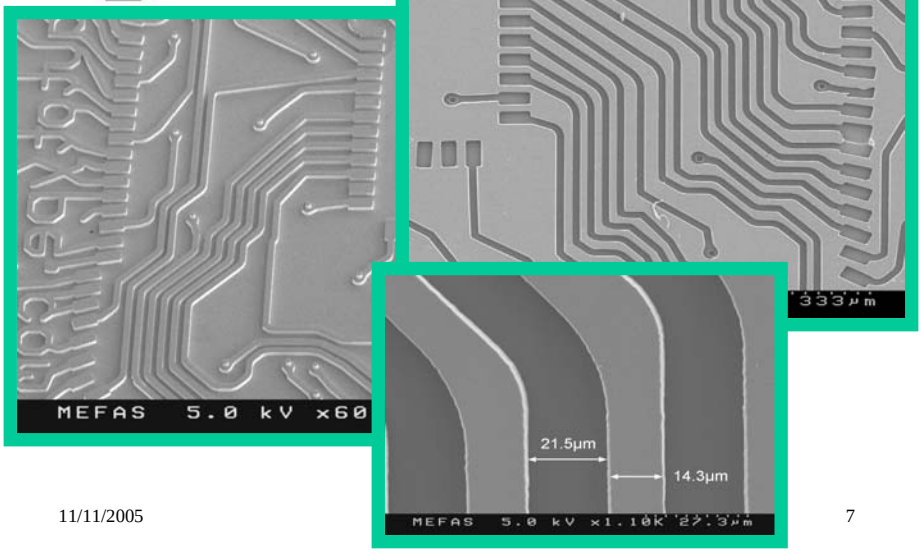


Concept & Technology

Photolithography & Laser Drilling: both are fundamental PCB fabrication processes. And, both contribute *significantly* to density constraints, cost, and yield loss.

Imprint Patterning replaces photo-lithography and laser drilling with a simple, cost-effective microreplication step.

HDI Toolfoil & Imprint



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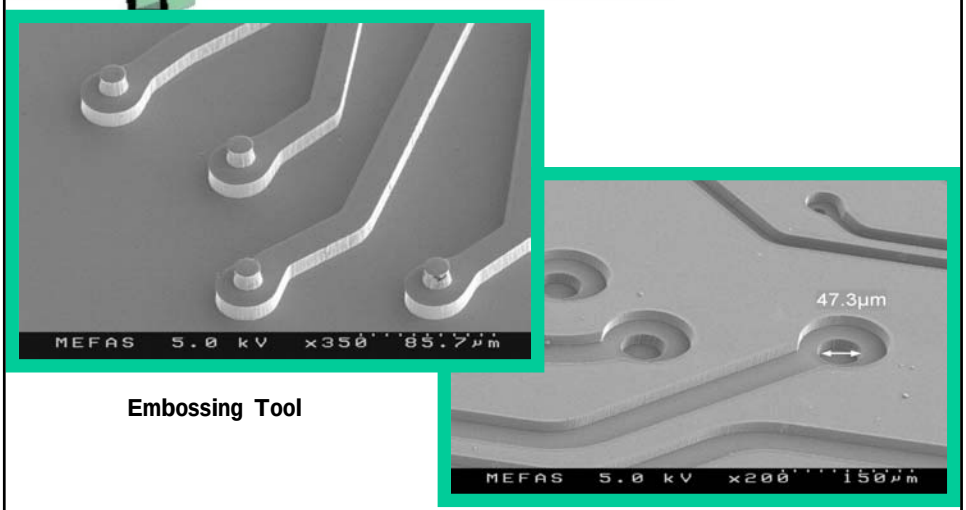
HDI Microvias



Embossing Tool

Embossed Dielectric

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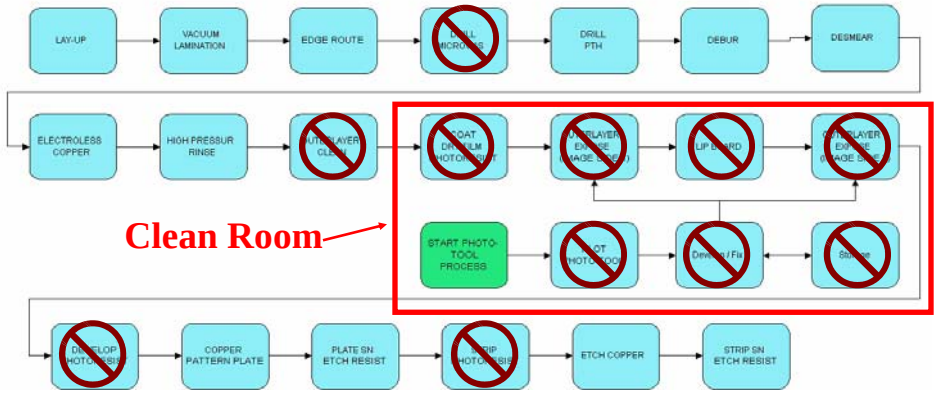
Cost Benefits

- 25-60% reduction in process costs
  - Reduction in process steps
  - Materials' savings
  - Eliminate equipment (capital investment)
  - Reduced facilities requirement (e.g. clean rooms)
- Reduced cycle times (improved cash conversion cycle)
- Reduced environmental impact !!
  - Less Power, Less Water, Less Waste

Performance Benefits

- ~40% increase in wiring density (cm/cm^2) with significantly improved yields (i.e. high quality)
- Reduced tolerance on line characteristics and impedance (better circuit performance; reduced variation)
- Reduced electrical parasitics
  - Eliminate capture/target pads
  - Reduce trace discontinuities through design
  - Higher via-density capability (power & ground distribution)
- Precision electrical elements
  - Filters, inductors, delay lines, etc.

Build-Up HDI Process



23 to 11 Process Steps

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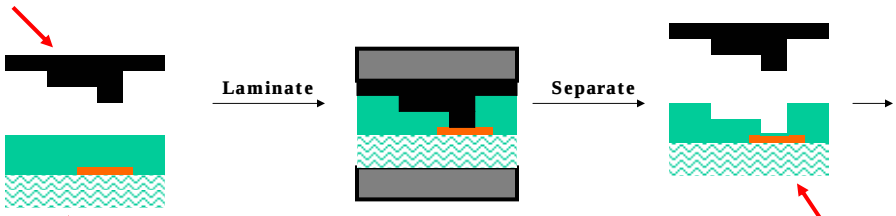
Imprint Process

Imprint toolFOIL with Circuit and Via Pattern "projections"

Reuse Imprint tool



Dielectric coated core

Imprinted circuit grooves and microvias

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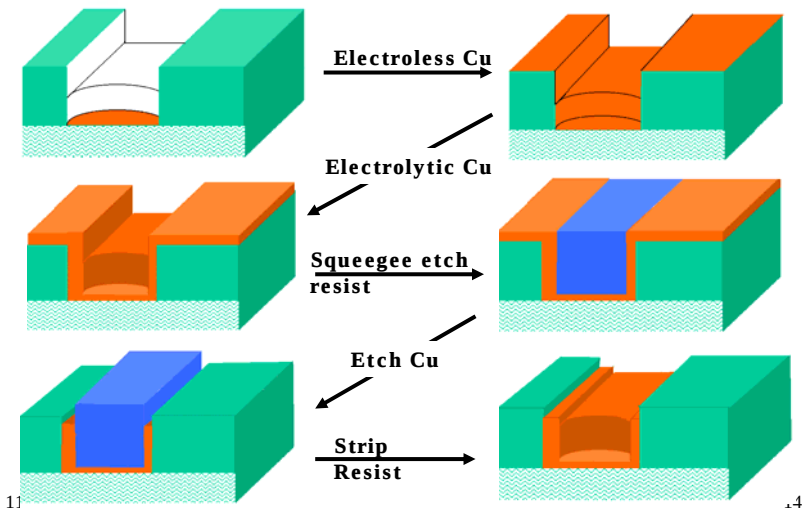
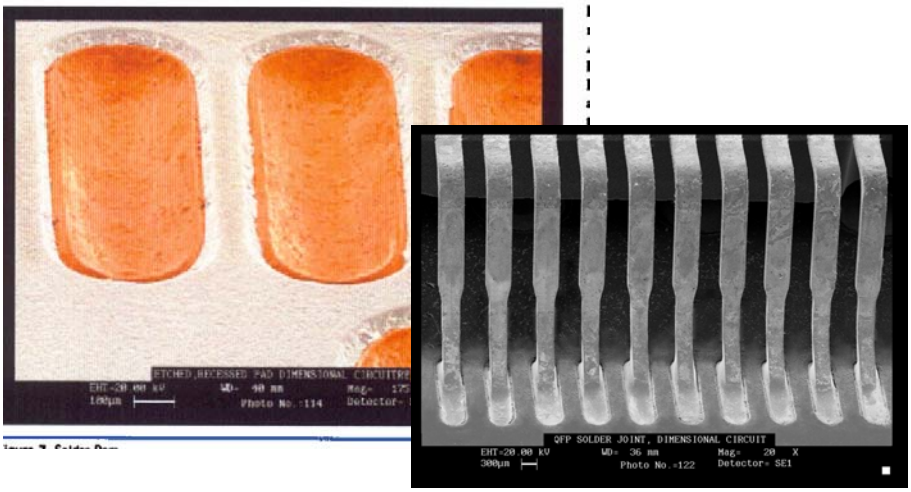
Imprint Process (cont.)

Metallization Method: Full Build Cu



Imprinted Circuit Pads



Intellectual Property

Inventor	Doc. No.	Issued	Claims
G. Gregoire	**RE38,579**	**2004**	**45**
G. Gregoire	**6,460,247**	**2002**	**19**
G. Gregoire	**6,005,198**	**1999**	**24**
G. Gregoire	**5,451,722**	**1995**	**1 (CIP)**
G. Gregoire	**5,390,412**	**1995**	**18**
G. Gregoire	5,391,353	1994	
G. Gregoire	5,334,279	1994	14
F. Parker	4,912,844	1990	19

148 Citations in the Patent Literature