Drop Testing of Components in Portable Applications

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NSC Interaction with HUT

- Reliability of CSPs in Drop Test (ending CY05)
- Effects of Microstructure and Underfill on High Frequency Signal Propagation in Pb-Free Solder Interconnections (ending CY06)
- Impact Of Miniaturization on Manufacturing and Reliability of Electronics (IMR) (ongoing) - Joint funding with National Technology Agency (Tekes), Nokia, Aspocomp, Ecoteq, Atotech, MAS, and National Semiconductor

- Students:
  - Dragos Burlacu, PhD candidate, to be graduated Summer 2006
  - Mikko Alajoki, Laboratory of Electronics Production Technology at HUT, graduated Fall 2004
  - Tommi Heinonen, Laboratory of Electronics Production Technology at HUT, to be graduated in autumn 2005
  - Pekka Marjamaki, PhD candidate – drop test modeling
  - Toni Mattila, PhD candidate – intermetallics
  - Pirjo Kontio, Research Engineer
All Work and No Play Makes for a Dull Stay

Artic noon
Northern Lights
Reindeer driver license
Rovaniemi
Lappish ceremony for crossing the Arctic Circle
Snowmobiling

Ice breaker cruise, icicle time
Kemi, Gulf of Bothnia

Extreme Thermal Shock!!!

Ice breaker view, Gulf of Bothnia, Jan. 02

Jump into Gulf of Bothnia for a swim in artic gear; wind chill factor ~ -40°F
Outline

• Motivation and Objectives

• Materials and Methods

• Results
  – Statistical Analysis
  – Failure Analysis

• Conclusions

Drop Testing

• Orienting an object w/r to an assumed gravitational field and allowing it to drop from a specified height onto a flat, rigid surface

• Significant test in several industries:
  – Nuclear industry, where the integrity of containers carrying radioactive waste must be insured during accident scenarios
  – Other applications where products are “dropped” while being used – handheld devices such as cell phones, computer mice, laptop computers, calculators, electronic instruments, etc.

• In each case, manufacturers want to develop a reputation for building rugged products, where they can be dropped and will still function properly
Background

- Portable electronic products are more likely to be severely damaged by the mechanical shocks produced by dropping the equipment than by thermomechanical stresses generated during typical use of the products.
- The first papers presented results on the reliability of electronic products under fast mechanical loading:
  - Drop impact produces excessive bending and vibration [1-4].
- Board level drop tests to evaluate the reliability of surface mount electronic components under mechanical shock loading:
  - The failure is strongly dependent on the design of the test board and material used [5-11].
- Development of standardized tests (e.g. JEDEC: JESD22-B111 in 2003 [12]):
  - To evaluate and compare drop reliability of different SMD components, metallization, solders etc. in an accelerated test environment [13-16].

Objectives

- Evaluate the drop test performance of lead-free wafer level chip scale packages (WL-CSP).
- Establish sound and well-understood relations between:
  - The reliability results (statistical analysis).
  - The observed failure modes (cross-sectional samples).
  - The associated metallurgies of solder interconnections (board side and component side metallizations, solder bump and solder alloy).
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WL-CSP: Micro SMD

• “The die is the package”
• Smallest footprint per I/O count
• High I/O density
• Best in class electrical performance
• Easy board assembly
• Level 1 moisture sensitivity performance
• No need for underfill material
• Interconnect layout at 0.5 mm pitch
• No interposer between the silicon IC and the printed circuit board
• Offered in 0.17mm and 0.3mm ball size (Sn/Pb and Sn/Ag/Cu)
• Epoxy backcoating provides conventional black marking surfaces

• Analog and Wireless products
Process Flow

1. Incoming wafer
2. 2nd passivation
3. Bumping
4. Back side coating
5. Laser mark
6. Test (Wafer sort)
7. Saw
8. Tape and reel

Side View of Assembled Package

- 0.3 mm balls, 280 μm top pad opening; 300 μm board pad opening
- Ersascope image of collapsed bumps
**Materials**

- Micro SMD 64-bump
  - 0.5 mm pitch and 0.3 mm diameter
  - 8x8 area array
  - No underfill
- Printed wiring boards
  - 1+6+1 stack up (JEDEC standard)
  - Double sided; one side used at a time
  - Micro-vias on one side only
- Solder alloys
  - Sn4Ag0.5Cu
  - Sn37Pb

**Experimental Design**

- Four variables each having two levels
  - Under bump metallization
    - (Al)Ni(V)|Cu
    - Electroless Ni(P)|Au
  - Solder bump alloy and solder paste
    - Near eutectic SnAgCu
    - Eutectic SnPb
  - PWB protective coating
    - CuOSP
    - Electroless Ni(P)|Au
    - Immersion Ag
  - Pad structure
    - Microvia-in-pad
    - No microvia-in-pad
- 6 to 9 fully furnished boards per variable
- Statistical testing with the ANOVA
Drop Test Set Up

- According to the JESD22-B111 standard (JEDEC: Board Level Drop Test Method of Components for Handheld Electronic Products)
- Peak deceleration of 1,500 g for 0.5 ms (half-sine pulse)
  - Drop height: 84 cm / 33 in
  - Failure criterion: 1 kΩ for 200 nanoseconds, 4 times in 6 consecutive drops

Deceleration Profile

Measured deceleration history during the 84 cm / 33” drop
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Average Drops To Failure

Average number of drops to failure at different locations of the board
Board Behavior After The Drop Impact

- Board starts to vibrate after the impact
- Bending is a sum of the board's natural modes i.e., eigenmodes
- The leftmost eigenmode has the strongest effect on the bending, while other modes have clearly smaller effect.

The eigenmodes represent vertical displacements of test boards.

Strains On The Board

Longitudinal Strain $[\times 10^6]$ vs. Time / ms

Strains at different locations on the board are shown.
Average Drops To Failure

Average number of drops to failure at different location of the board

- The three components in the middle of the board are the first ones to fail
- Average drops-to-failure was calculated based on these three components

Conclusions Based On The Statistical Analysis

- Statistically significant difference was found only between the component side metallizations:
  - Components with the (Al)Ni(V)/Cu UBM are more reliable than those with the electroless Ni(P)/Au UBM
  - No statistically significant differences between the PWB protective coatings
  - No statistically significant differences between the soldering pad structure

- No statistically significant difference was found between the PWB finishes with the (Al)Ni(V)/Cu components. However, with the electroless Ni(P)/Au components the assemblies with the Cu/OSP board finishes are more reliable than the assemblies with the electroless Ni(P)/Au board finish.

- The most reliable material combination:
  - (Al)Ni(V)/Cu component metallization, SnPb solder bump, Sn37Pb solder paste, Cu/OSP PWB finish and no microvia-in-pad board structure
Microvia-in-Pad

Weibull plots for the lead-free microvia-in-pad assemblies
(Legend: component metallization + solder bump material + printed wiring board finish)

No Microvia-in-Pad

Weibull plots for the lead-free no microvia-in-pad assemblies
(Legend: component metallization + solder bump material + printed wiring board finish)
UBM Comparison

Weibull plots for the no microvia-in-pad assemblies
(Legend: component metallization + solder bump material + printed wiring board finish)

Weibull Parameters

<table>
<thead>
<tr>
<th>Component metallization</th>
<th>Bump alloy</th>
<th>Solder paste</th>
<th>PWB surface finish</th>
<th>Pad structure</th>
<th>$\eta$</th>
<th>$\beta$</th>
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<tbody>
<tr>
<td>(AlNi)Cu</td>
<td>SnAgCu</td>
<td>Sn3.8Ag0.7Cu</td>
<td>Electroless Ni(P)/Au</td>
<td>Microvia-in-pad</td>
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</tr>
</tbody>
</table>
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Failure Modes After Drop Testing

Ni(V)|Cu  Ni(P)|Au
Failure Modes After Thermal Cycling

Microstructures After Reflow

Optical Microscopy: Polarized Light Images
Evolution of the Microstructures During Thermal Cycling

- Gradual expansion of recrystallization
- Cracks nucleate and grow along the grain boundaries especially between the recrystallized and the non-recrystallized part of the interconnections

Microstructures After Failure In Drop Testing

- No recrystallization
- Deformation twins
Strain-Rate Sensitivity

![Graph showing strain-rate sensitivity for Sn2Ag0.5Cu](image)

Effect of deformation rate on stresses

The stresses increase with increased deformation rate due to reduced plastic deformation.

[13-14]
• Stresses are larger on the component side than on the PWB side
• Thus, cracks tend to nucleate and propagate on the component side of the interconnections

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• Motivation and Objectives
• Materials and Methods
• Results
  – Statistical Analysis
  – Failure Analysis
    • Failure modes in drop tests vs. those in thermal cycling
    • Impact of under bump metallization
    • Impact of PWB protective coating
    • Impact of solder alloy
• Conclusions
Failure Modes On The Component Side

Ni(V)|Cu

Ni(P)|Au

Component Side IMC Layer

Ni(V)|Cu
Cracks propagate mostly through Cu₆Sn₅ layer

Observed only when the assemblies have been dropped several times after the first electrical failure has been detected

Component Side IMC Layer

PWB Side Failure Modes

Cracks propagate between (Cu,Ni)₆Sn₅ and Ni(P) layers

Cracks propagate mostly through Cu₆Sn₅ layer
PWB Side Failure Modes: 
Ni(P)|Au Joints

Ni(P)|Solder Reaction Zone
Effect Of The Solder Alloy

Cracks propagate along the interface between the IMC and the bulk solder!

Cracks propagate through the intermetallic layer!

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• Both statistical and failure analysis revealed that the most significant factor affecting the drop test reliability was the reaction layers formed on the component side

• Statistically significant differences were found only between the different under bump metallizations

• Interconnection with electroless Ni(V)|Cu under bump metallizations are superior to those with Ni(P)|Au metallization

• Phosphorous in the electroless Ni layer may have detrimental effect on the reliability of lead-free interconnections when tested under mechanical shock loading conditions

• Primary failure mode under fast deformation rates differs from that typically observed in thermally cycled interconnections due to the increased flow stress at drop tests

References ... 1 of 2

References ... 2 of 2