National Semiconductor
The Sight & Sound of Information

# Drop Testing of Components in Portable Applications

*L. Nguyen*
*National Semiconductor Corp.*
*Santa Clara, CA 95052*



## Acknowledgments


- **Fellowship**: Fulbright Scholarship Program
  Nokia Foundation
- **NSFN**: R. Nystroem, Mika Boos, and Matti Selaenne
- **NSSC**: S. Patil, G. Coppinger, M. Yegnashankaran, K. Aggarwal
- **HUT**: Prof. J. Kivilahti and research group


National Semiconductor
The Sight & Sound of Information

Otaniemi
Technology Park

Nokia R&D

National Semiconductor
The Sight & Sound of Information

3

# NSC Interaction with HUT

- **Reliability of CSPs in Drop Test (*ending CY05*)**
- **Effects of Microstructure and Underfill on High Frequency Signal Propagation in Pb-Free Solder Interconnections (*ending CY 06*)**
- **Impact Of Miniaturization on Manufacturing and Reliability of Electronics (IMR) (*ongoing*) - Joint funding with National Technology Agency (Tekes), Nokia, Aspocomp, Ecoteq, Atotech, MAS, and National Semiconductor**
- **Students:**
  - **Dragos Burlacu, PhD candidate, to be graduated Summer 2006**
  - **Mikko Alajoki, Laboratory of Electronics Production Technology at HUT, graduated Fall 2004**
  - **Tommi Heinonen, Laboratory of Electronics Production Technology at HUT, to be graduated in autumn 2005**
  - **Pekka Marjamaki, PhD candidate – drop test modeling**
  - **Toni Mattila, PhD candidate – intermetallics**
  - **Pirjo Kontio, Research Engineer**

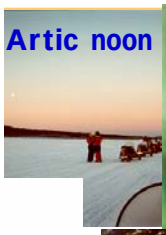
National Semiconductor
The Sight & Sound of Information

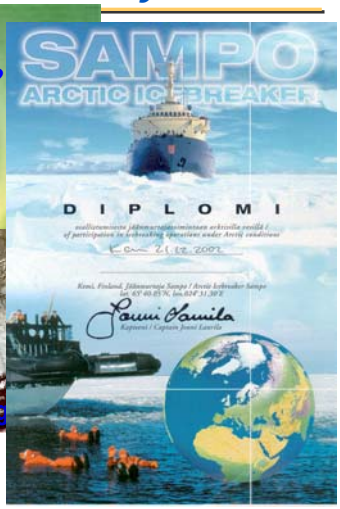
4

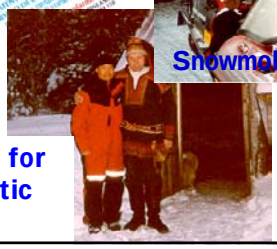
2

# All Work and No Play Makes for a Dull Stay

Reindeer driver license Rovaniemi







Lappish ceremony for crossing the Arctic Circle

Ice breaker cruise, icicle time Kemi, Gulf of Bothnia

5

# Extreme Thermal Shock!!!

Ice breaker view, Gulf of Bothnia, Jan. 02

Jump into Gulf of Bothnia for a swim in artic gear; wind chill factor ~ -40°F

National Semiconductor
The Sight & Sound of Information

6

2

## Outline

- **Motivation and Objectives**
- **Materials and Methods**
- **Results**
  - **Statistical Analysis**
  - **Failure Analysis**
- **Conclusions**

National Semiconductor
The Sight & Sound of Information

7

## Drop Testing

- **Orienting an object w/r to an assumed gravitational field and allowing it to drop from a specified height onto a flat, rigid surface**
- **Significant test in several industries:**
  - **Nuclear industry, where the integrity of containers carrying radioactive waste must be insured during accident scenarios**
  - **Other applications where products are "dropped" while being used – handheld devices such as cell phones, computer mice, laptop computers, calculators, electronic instruments, etc.**
- **In each case, manufacturers want to develop a reputation for building rugged products, where they can be dropped and will still function properly**

National Semiconductor
The Sight & Sound of Information

8

## Background

- Portable electronic products are more likely to be severely damaged by the mechanical shocks produced by dropping the equipment than by thermomechanical stresses generated during typical use of the products
- The first papers presented results on the reliability of electronic products under fast mechanical loading
  - Drop impact produces excessive bending and vibration [1-4]
- Board level drop tests to evaluate the reliability of surface mount electronic components under mechanical shock loading
  - The failure is strongly dependent on the design of the test board and material used [5-11]
- Development of standardized tests (e.g. JEDEC: JESD22-B111 in 2003 [12])
  - To evaluate and compare drop reliability of different SMD components, metallization, solders etc. in an accelerated test environment [13-16]

National Semiconductor
The Sight & Sound of Information

9

## Objectives

- Evaluate the drop test performance of lead-free wafer level chip scale packages (WL-CSP)
- Establish sound and well–understood relations between:
  - The reliability results (statistical analysis)
  - The observed failure modes (cross-sectional samples)
  - The associated metallurgies of solder interconnections (board side and component side metallizations, solder bump and solder alloy)

National Semiconductor
The Sight & Sound of Information

10

2

## Outline

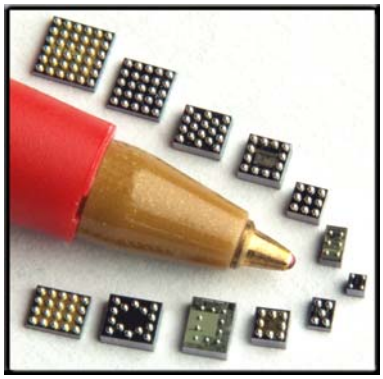
- Motivation and Objectives
- Materials and Methods
- Results
  - Statistical Analysis
  - Failure Analysis
- Conclusions

National Semiconductor
The Sight & Sound of Information

11

## WL-CSP: Micro SMD

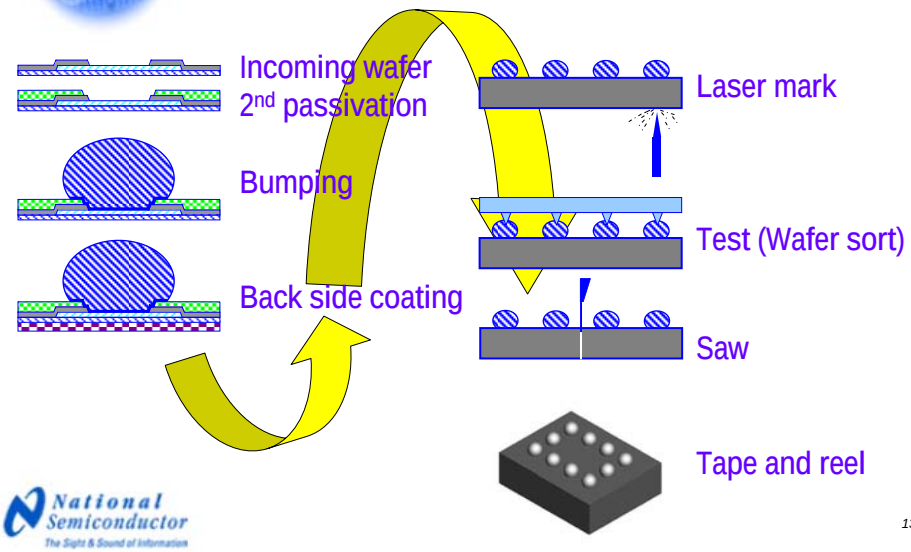
- "The die is the package"
- Smallest footprint per I/O count
- High I/O density
- Best in class electrical performance
- Easy board assembly
- Level 1 moisture sensitivity performance
- No need for underfill material
- Interconnect layout at 0.5 mm pitch
- No interposer between the silicon IC and the printed circuit board
- Offered in 0.17mm and 0.3mm ball size (Sn/Pb and Sn/Ag/Cu)
- Epoxy backcoating provides conventional black marking surfaces
- *Analog and Wireless products*



National Semiconductor
The Sight & Sound of Information

12

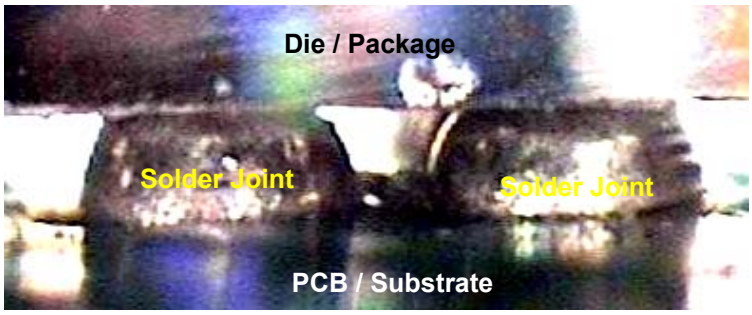
# Process Flow




National Semiconductor
The Sight & Sound of Information

13

# Side View of Assembled Package



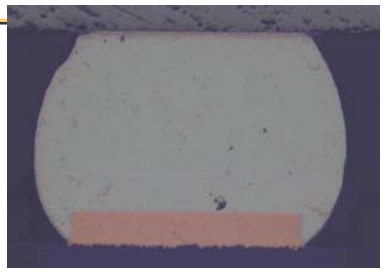

0.3 mm balls, 280 μm top pad opening; 300 μm board pad opening
Ersascope image of collapsed bumps

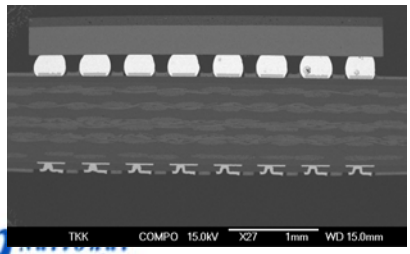
National Semiconductor
The Sight & Sound of Information

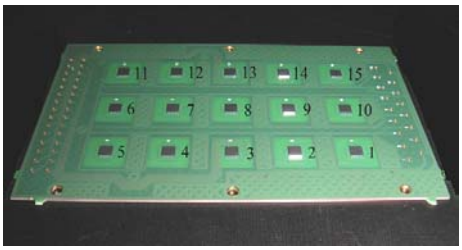
14

# Materials

- Micro SMD 64-bump
  - 0.5 mm pitch and 0.3 mm diameter
  - 8x8 area array
  - No underfill
- Printed wiring boards
  - 1+6+1 stack up (JEDEC standard)
  - Double sided; one side used at a time
  - Micro-vias on one side only
- Solder alloys
  - Sn4Ag0.5Cu
  - Sn37Pb





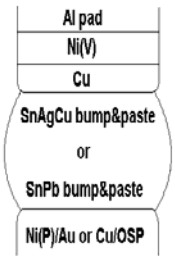



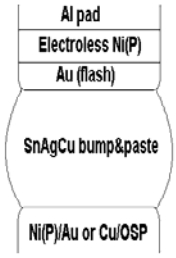

National Semiconductor
The Sight & Sound of Information

15

# Experimental Design

- Four variables each having two levels
  - Under bump metallization
    - (Al)Ni(V)|Cu
    - Electroless Ni(P)|Au
  - Solder bump alloy and solder paste
    - Near eutectic SnAgCu
    - Eutectic SnPb
  - PWB protective coating
    - Cu|OSP
    - Electroless Ni(P)|Au
    - Immersion Ag
  - Pad structure
    - Microvia-in-pad
    - No microvia-in-pad



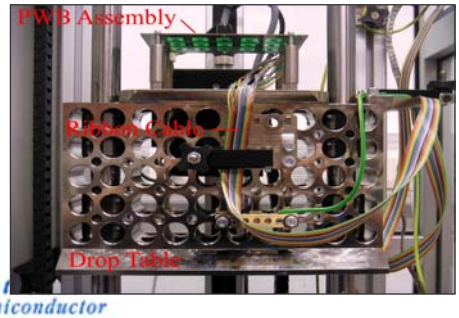

- 6 to 9 fully furnished boards per variable
- Statistical testing with the ANOVA

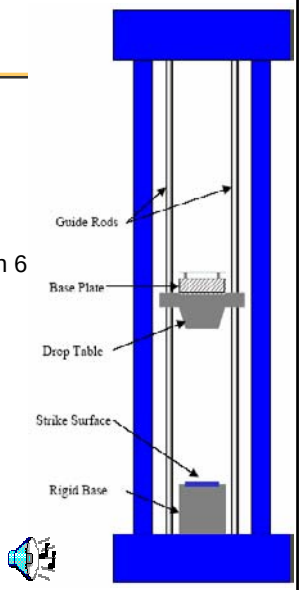
National Semiconductor
The Sight & Sound of Information

16

# Drop Test SetUp

- **According to the JESD22-B111 standard (JEDEC: *Board Level Drop Test Method of Components for Handheld Electronic Products*)**
- **Peak deceleration of 1,500 g for 0.5 ms (half-sine pulse)**
  - Drop height: 84 cm / 33 in
  - Failure criterion: 1 kΩ for 200 nanoseconds, 4 times in 6 consecutive drops



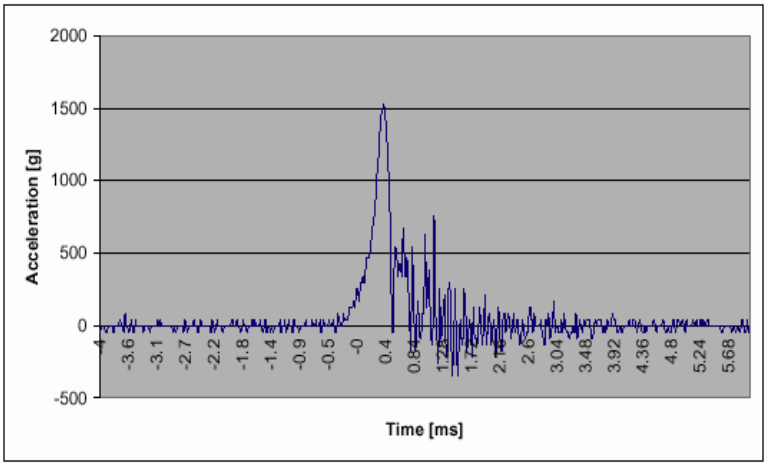




National Semiconductor
The Sight & Sound of Information

17

# Deceleration Profile

***Measured deceleration history during the 84 cm / 33" drop***




National Semiconductor
The Sight & Sound of Information

18

2

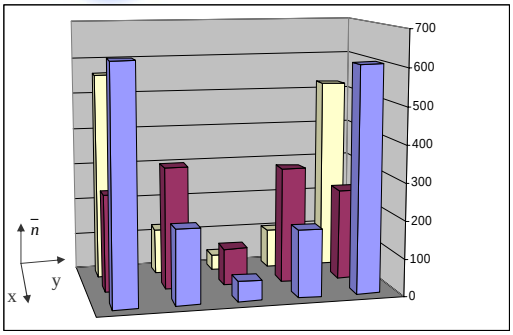
# Outline

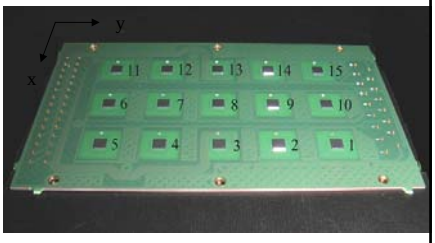
- Motivation and Objectives
- Materials and Methods
- Results
  - Statistical Analysis
  - Failure Analysis
- Conclusions

National Semiconductor
The Sight & Sound of Information

19

# Average Drops To Failure



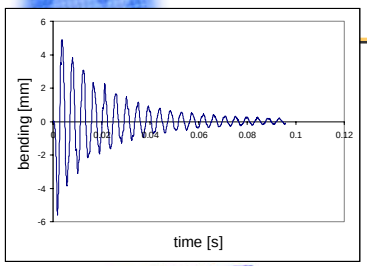




*Average number of drops to failure at different locations of the board*

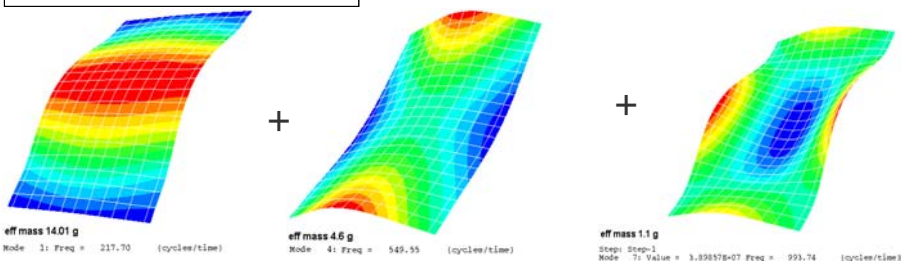
National Semiconductor
The Sight & Sound of Information

20

## Board Behavior After The Drop Impact




- **Board starts to vibrate after the impact**
- **Bending is a sum of the board's natural modes i.e. eigenmodes**
- **The leftmost eigenmode has strongest effect on the bending, while other modes have clearly smaller effect**

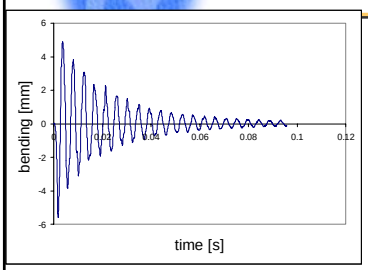


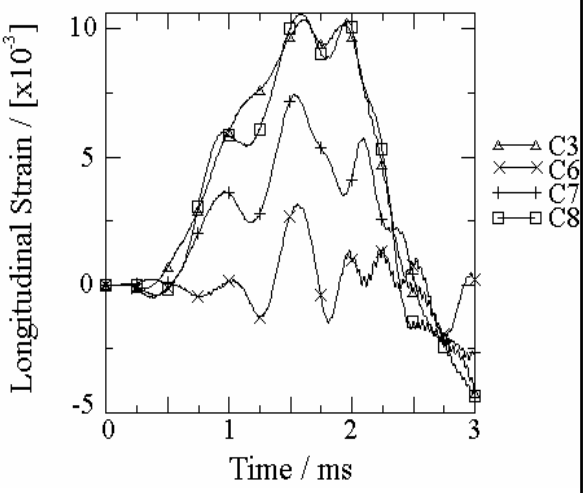

***The eigenmodes represent vertical displacements of test boards***

National Semiconductor
The Sight & Sound of Information

21

## Strains On The Board



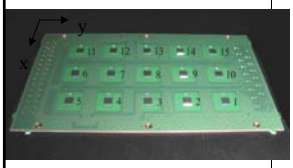


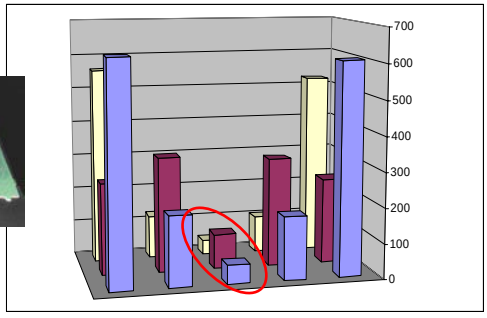

National Semiconductor
The Sight & Sound of Information

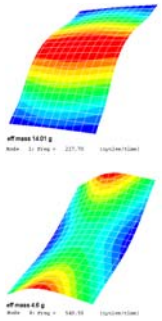
22

# Average Drops To Failure

***Average number of drops to failure at different location of the board***



- **The three components in the middle of the board are the first ones to fail**
  **→ Average drops-to-failure was calculated based on these three components**

National Semiconductor
The Sight & Sound of Information

23

# Conclusions Based On The Statistical Analysis

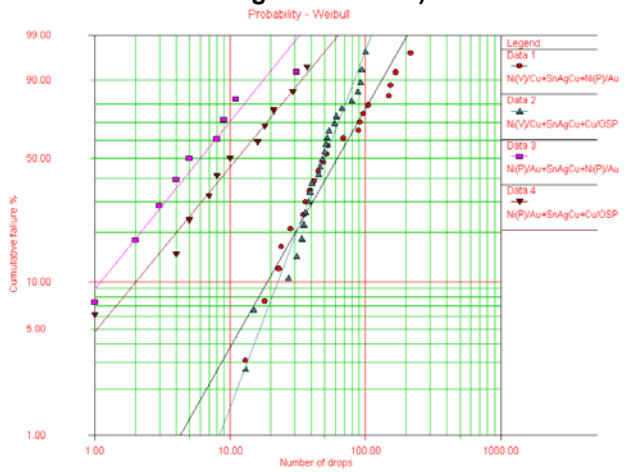
- **Statistically significant difference was found only between the component side metallizations:**
  - **Components with the *(Al)Ni(V)|Cu* UBM are more reliable than those with the electroless Ni(P)|Au UBM**
  - **No statistically significant differences between the PWB protective coatings**
  - **No statistically significant differences between the soldering pad structure**
- **No statistically significant difference was found between the PWB finishes with the (Al)Ni(V)|Cu components. However, with the electroless Ni(P)|Au components the assemblies with the *Cu|OSP* board finishes are more reliable than the assemblies with the electroless Ni(P)|Au board finish.**
- **The most reliable material combination:**
  - ***(Al)Ni(V)|Cu* component metallization, *SnPb* solder bump, *Sn37Pb* solder paste, *Cu|OSP* PWB finish and *no microvia*-in-pad board structure**

National Semiconductor
The Sight & Sound of Information

24

# Microvia-in-Pad

**Weibull plots for the lead-free microvia-in-pad assemblies (Legend: component metallization + solder bump material + printed wiring board finish)**

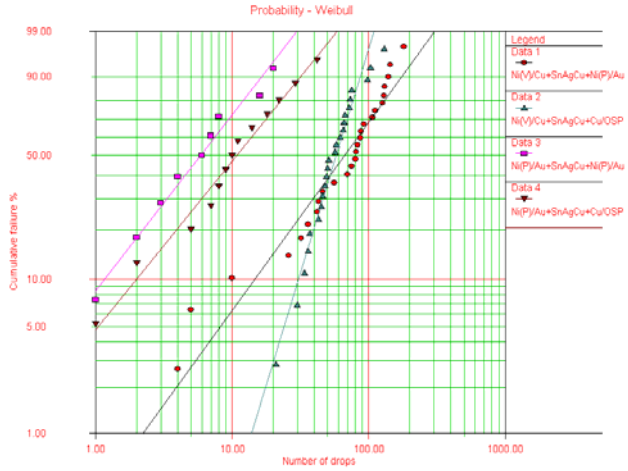



National Semiconduc
The Sight & Sound of Infor

25

# No Microvia-in-Pad

**Weibull plots for the lead-free no microvia-in-pad assemblies (Legend: component metallization + solder bump material + printed wiring board finish)**

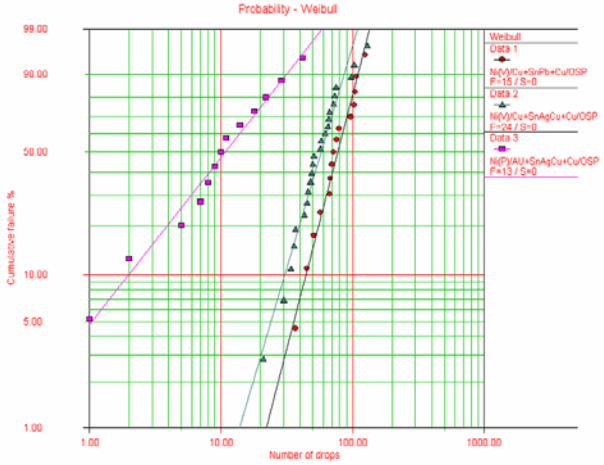



National Semiconduc
The Sight & Sound of Infor

26

# UBM Comparison

**Weibull plots for the no microvia-in-pad assemblies (Legend: component metallization + solder bump material + printed wiring board finish)**




National Semiconductor
The Sight & Sound of Information

27

# Weibull Parameters

| Component metallization | Bump alloy | Solder paste | PWB surface finish | Pad structure | η | β |
|---|---|---|---|---|---|---|
| (Al)Ni(V)\|Cu | SnAgCu | Sn3.8Ag0.7Cu | Electroless Ni(P)\|Au | Microvia-in-pad | 78 | 1.6 |
| (Al)Ni(V)\|Cu | SnAgCu | Sn3.8Ag0.7Cu | Electroless Ni(P)\|Au | No Microvia-in-pad | 89 | 1.2 |
| (Al)Ni(V)\|Cu | SnAgCu | Sn3.8Ag0.7Cu | Cu\|OSP | Microvia-in-pad | 58 | 2.4 |
| (Al)Ni(V)\|Cu | SnAgCu | Sn3.8Ag0.7Cu | Cu\|OSP | No Microvia-in-pad | 66 | 3.0 |
| (Al)Ni(V)\|Cu | SnPb | SnPb eut. | Electroless Ni(P)\|Au | Microvia-in-pad | 54 | 3.6 |
| (Al)Ni(V)\|Cu | SnPb | SnPb eut. | Electroless Ni(P)\|Au | No Microvia-in-pad | 41 | 3.3 |
| (Al)Ni(V)\|Cu | SnPb | SnPb eut. | Cu\|OSP | Microvia-in-pad | 47 | 3.3 |
| (Al)Ni(V)\|Cu | SnPb | SnPb eut. | Cu\|OSP | No Microvia-in-pad | 86 | 3.4 |
| Electroless Ni(P)\|Au | SnAgCu | Sn3.8Ag0.7Cu | Electroless Ni(P)\|Au | Microvia-in-pad | 8 | 1.1 |
| Electroless Ni(P)\|Au | SnAgCu | Sn3.8Ag0.7Cu | Electroless Ni(P)\|Au | No Microvia-in-pad | 8 | 1.1 |
| Electroless Ni(P)\|Au | SnAgCu | Sn3.8Ag0.7Cu | Cu\|OSP | Microvia-in-pad | 16 | 1.1 |
| Electroless Ni(P)\|Au | SnAgCu | Sn3.8Ag0.7Cu | Cu\|OSP | No Microvia-in-pad | 15 | 1.1 |

National Semiconductor
The Sight & Sound of Information

28

2

## Outline

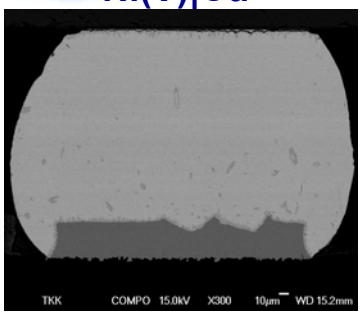
- Motivation and Objectives
- Materials and Methods
- Results
  - Statistical Analysis
  - Failure Analysis
- Conclusions

National Semiconductor
The Sight & Sound of Information

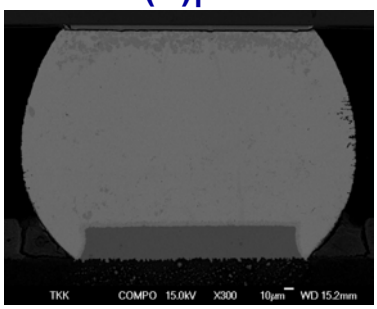
29

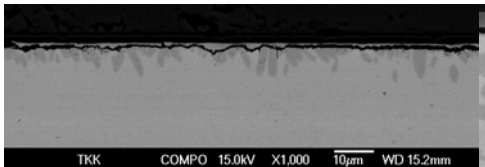
## Failure Modes After Drop Testing

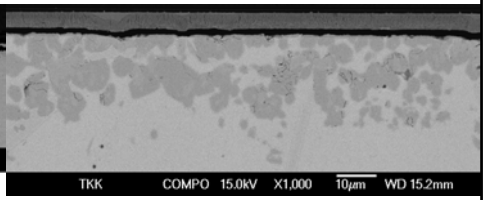
**Ni(V)|Cu**




**Ni(P)|Au**

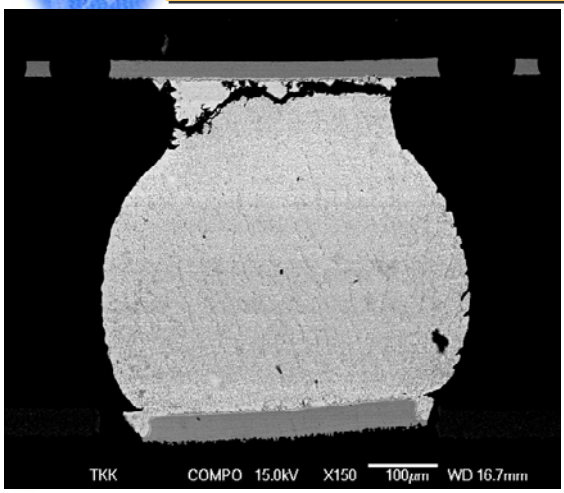


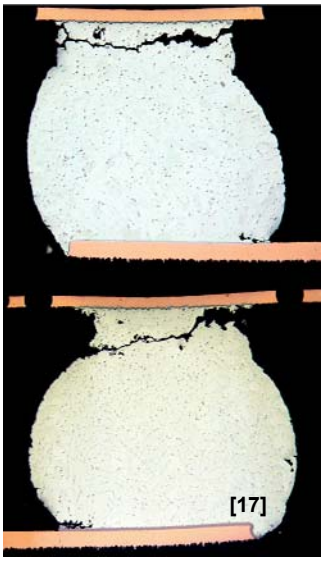




Semiconductor
The Sight & Sound of Information

# Failure Modes After Thermal Cycling



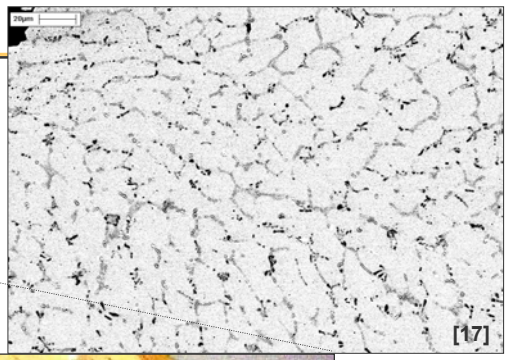



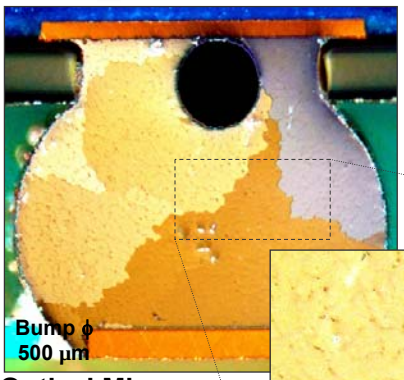

National Semiconductor
The Sight & Sound of Information

Bump ϕ
500 μm

31

# Microstructures After Reflow




Optical Microscopy: Polarized Light Images

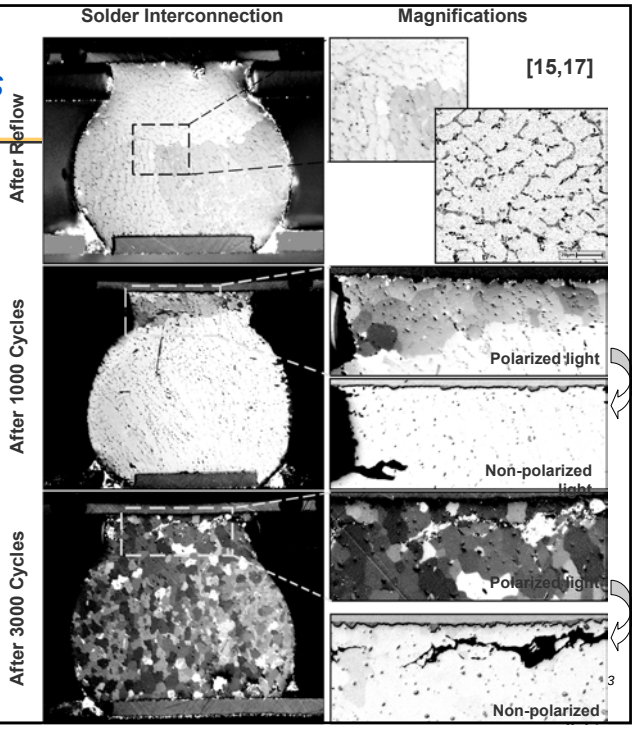
SEM Image

National Semiconductor
The Sight & Sound of Information

32

## Evolution of the Microstructures During Thermal Cycling

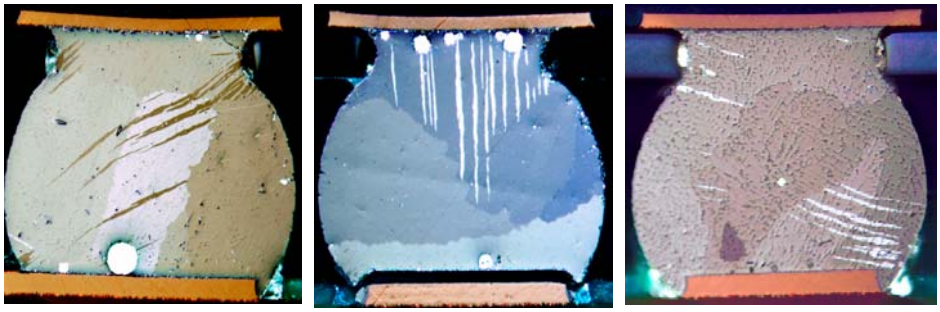
- Gradual expansion of recrystallization
- Cracks nucleate and grow along the grain boundaries especially between the recrystallized and the non-recrystallized part of the interconnections




National Semiconductor
The Sight & Sound of Information

3

## Microstructures After Failure In Drop Testing



- No recrystallization
- Deformation twins

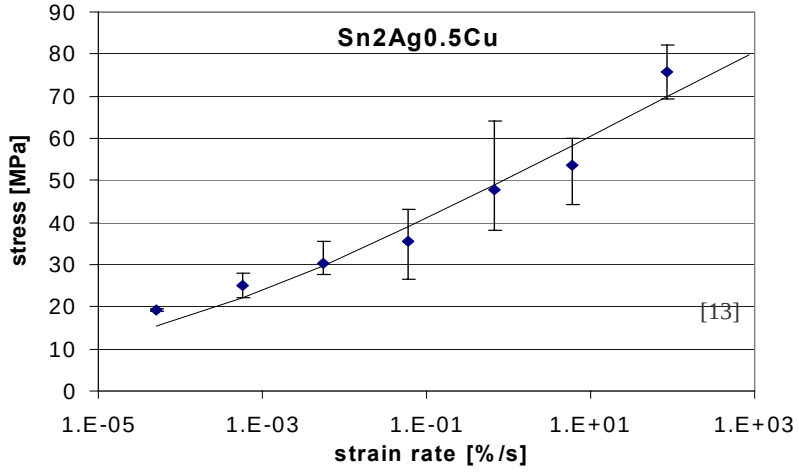
Bump ϕ 500 μm

[13-15]

National Semiconductor
The Sight & Sound of Information

34

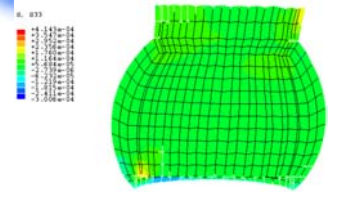
# Strain-Rate Sensitivity



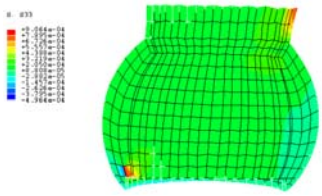

National Semiconductor
The Sight & Sound of Information

35

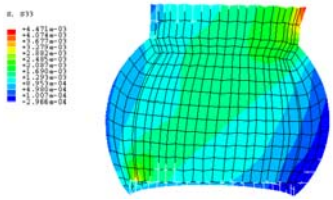
# Effect Of Deformation Rate On Stresses



rate 0.1 % / s



rate 10 % / s



rate 1000 % / s

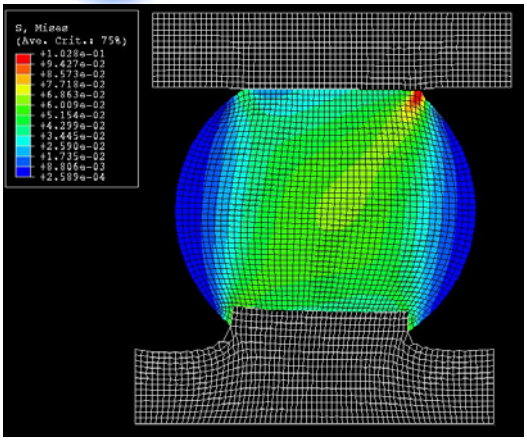
[14-16]

**The stresses increase with increased deformation rate due to reduced plastic deformation**

National Semiconductor
The Sight & Sound of Information

36

# FEM: Stresses In The Interconnections




- **Stresses are larger on the component side than on the PWB side**
- **Thus, cracks tend to nucleate and propagate on the component side of the interconnections**

National Semiconductor
The Sight & Sound of Information

37

2

# Outline

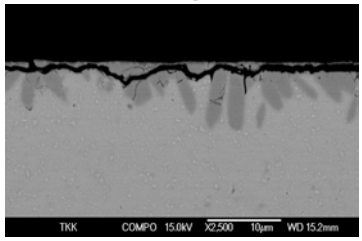
- **Motivation and Objectives**
- **Materials and Methods**
- **Results**
  - **Statistical Analysis**
  - **Failure Analysis**
    - **Failure modes in drop tests vs. those in thermal cycling**
    - **Impact of under bump metallization**
    - **Impact of PWB protective coating**
    - **Impact of solder alloy**
- **Conclusions**

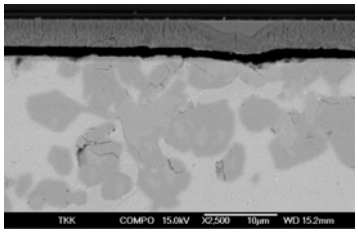
National Semiconductor
The Sight & Sound of Information

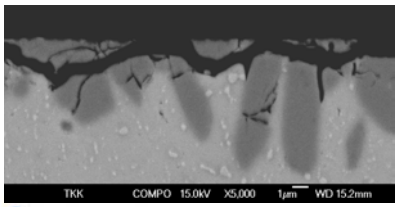
38

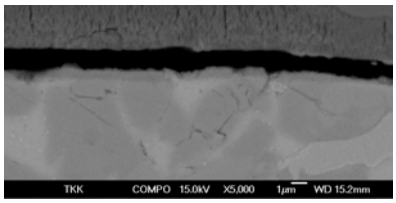
# Failure Modes On The Component Side

**Ni(V)|Cu** Ni(P)|Au



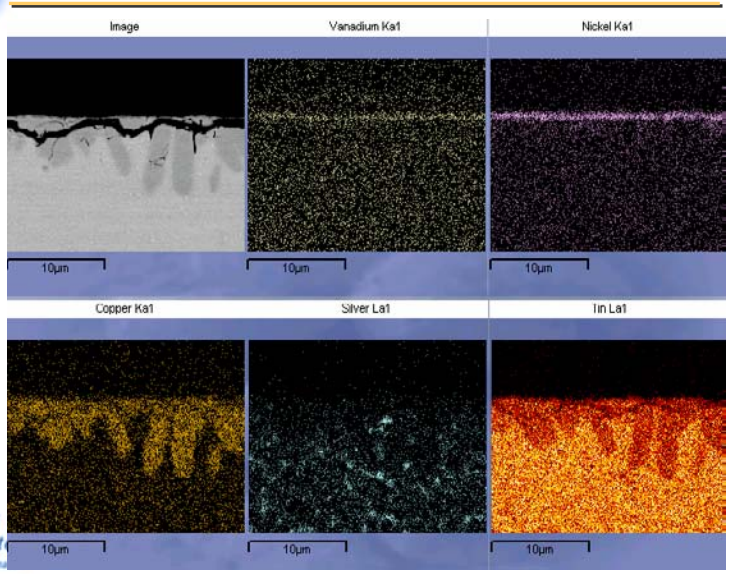




National Semiconductor
The Sight & Sound of Information

39

# Component Side IMC Layer

**Ni(V)|Cu**

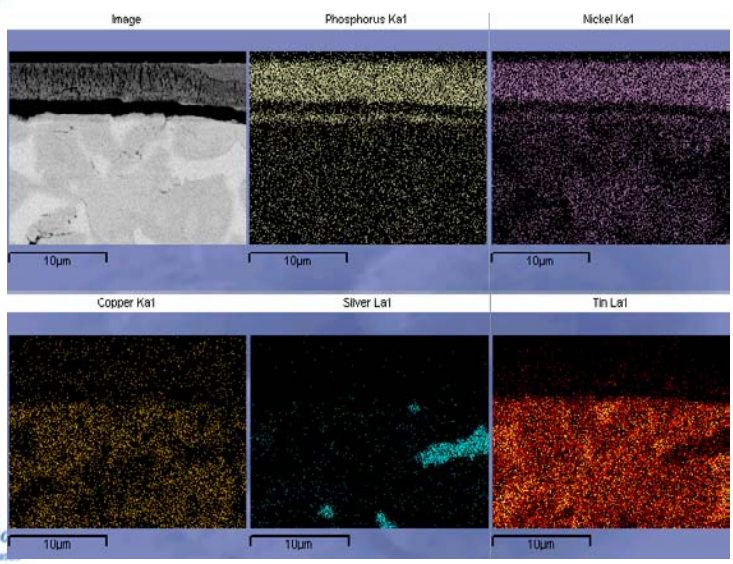



National Semiconductor
The Sight & Sound of Information

40

## Component Side IMC Layer

**Ni(P)|Au**



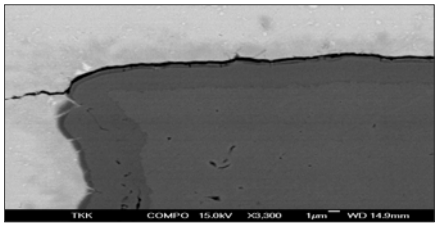

National Semiconductor
The Sight & Sound of Information

41

## PWB Side Failure Modes

**Observed only when the assemblies have been dropped several times after the first electrical failure has been detected**

**Ni(P)|Au**




***Cracks propagate between $(Cu,Ni)_6Sn_5$ and Ni(P) layers***

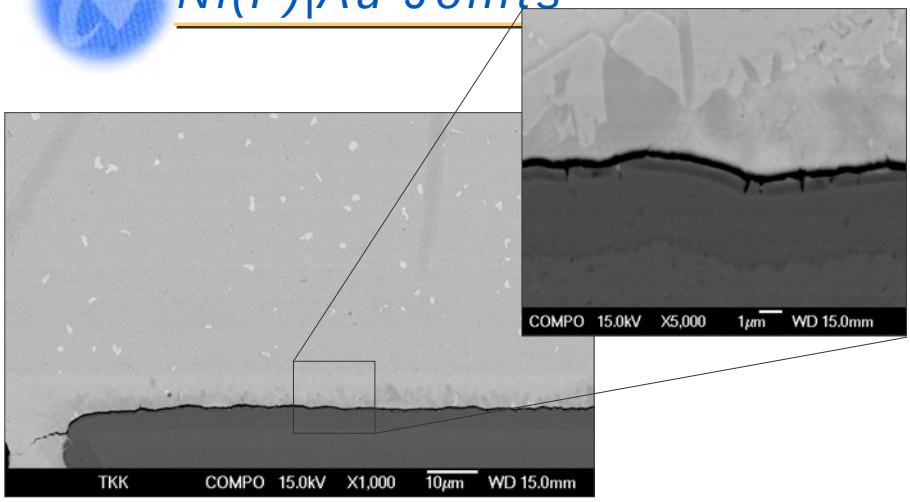
**Cu|OSP**

***Cracks propagate mostly through $Cu_6Sn_5$ layer***

National Semiconductor
The Sight & Sound of Information

42

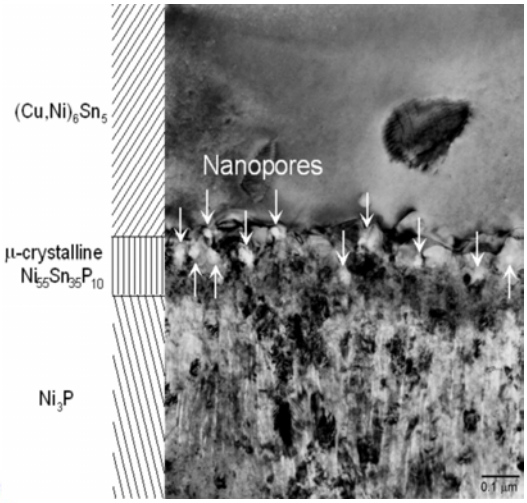
## PWB Side Failure Modes: Ni(P)|Au Joints




National Semiconductor
The Sight & Sound of Information

43

## Ni(P)|Solder Reaction Zone

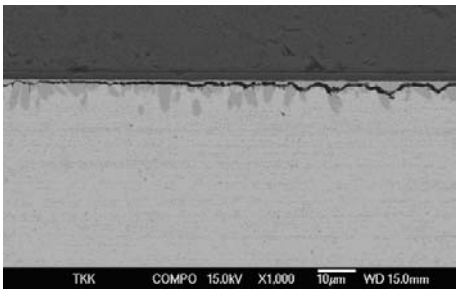



National Semiconductor
The Sight & Sound of Information

44

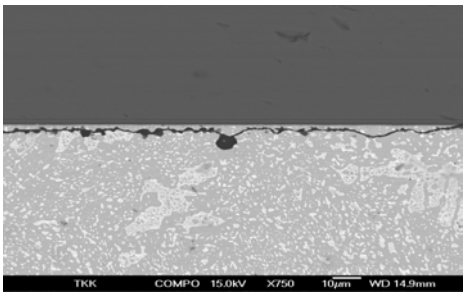
## Effect Of The Solder Alloy

(Al)Ni(V)|Cu and SnAgCu solder bump




*Cracks propagate through the intermetallic layer!*

(Al)Ni(V)|Cu + SnPb solder bump




*Cracks propagate along the interface between the IMC and the bulk solder!*

National Semiconductor
The Sight & Sound of Information

45

2

## Outline

- **Motivation and the Objectives**
- **Materials and Methods**
- **Results**
  - **Statistical Analysis**
  - **Failure Analysis**
- **Conclusions**

National Semiconductor
The Sight & Sound of Information

46

# Conclusions

- Both statistical and failure analysis revealed that the most significant factor affecting the drop test reliability was the reaction layers formed on the component side
- Statistically significant differences were found only between the different under bump metallizations
- Interconnection with electroless Ni(V)|Cu under bump metallizations are superior to those with Ni(P)|Au metallization
- Phosphorous in the electroless Ni layer may have detrimental effect on the reliability of lead-free interconnections when tested under mechanical shock loading conditions
- Primary failure mode under fast deformation rates differs from that typically observed in thermally cycled interconnections due to the increased flow stress at drop tests

National Semiconductor
The Sight & Sound of Information

47

# References ... 1 of 2


1. Low, K. H., Yang, A., Hoon, K. H., Zhang, X., Lim, J., and Lim, K. H., "Initial Study on the Drop-Impact Behavior of Mini Hi-Fi Audio Products," *Advances in Engineering Software*, Volume 32, Issue 9, Sep. 2001, pp. 683-693
2. Seah, S.K.W., Lim, C.T., Wong, E.H., Tan, V.B.C., and Shim, V.P.W., "Mechanical Response of PCBs in Portable Electronic Products During Drop Impact," *4th Electronics Packaging Technology Conference*, 10-12 Dec. 2002, pp. 120-125
3. Lim, C. T. and Low, Y. J., "Investigating the Drop Impact of Portable Electronic Products," *52nd Electronic Components and Technology Conference*, 28-31 May 2002, pp. 1270 -1274
4. Chwee-Teck Lim, Teo, Y.M., and Shim, V.P.W., "Numerical Simulation of the Drop Impact Response of a Portable Electronic Product," *IEEE Transactions on Components and Packaging Technologies* [see also Components, Packaging and Manufacturing Technology, Part A: Packaging Technologies, IEEE Transactions on], Volume: 25 Issue: 3, Sept. 2002, pp. 478-485
5. Wu, J., Song, G., Yeh, C.-P., and Wyatt, K., "Drop/Impact Simulation and Test Validation of Telecommunication Products," Thermal and Thermomechanical Phenomena in Electronic Systems, *ITHERM '98*. The Sixth Intersociety Conference on, 27-30 May 1998, pp. 330-336
6. Won, E. H., Kim, K. M., Lee, N., Seah, S., Hoe, C., and Wang, J., "Drop Impact Test – Mechanics & Physics of Failure," Thermal and Thermomechanical Phenomena in Electronic Systems, 1998. *ITHERM '98*. The Sixth Intersociety Conference on, 27-30 May 1998, pp. 330-336
7. Kujala, A., Reinikainen, T., and Ren, W., "Transition to Pb-free Manufacturing Using Land Grid Array Packaging Technology," *52nd Electronic Components and Technology Conference*, 28-31 May 2002, pp. 359-364
8. Mishiro, K., Ishikawa, S., Abe, M., Kumai, T, Higashiguchi, Y., and Tsebone, K., "Effect of The Drop Impact on BGA/CSP Package Reliability," *Microelectronics Reliability*, 42 (2002), pp. 77-82


National Semiconductor
The Sight & Sound of Information

48

# References ... 2 of 2


9. Arra, M., Xie, D., and Shangguan, D., "Performance of Lead-Free Solder Joints Under Dynamic Mechanical Loading," *The Proceedings of Electronic Components and Technology Conference*, 2002
10. Kujala, K. and Kulojärvi, M., "Package Miniaturization Options and Challenges for Baseband IC's," *Proceedings of IMAPS Nordic Annual Conference*, 21-24, 2003
11. Tee, T. Y., Ng, H. S., Lim, C. T., Pck, E., and Zhong, Z., "Board Level Drop Test and Simulation of TFBGA Packages for Telecommunication Applications," *Proceedings of Electronic Components and Technology Conference*, 2003
12. JESD22-B111. Board Level Drop Test Method of Components for Handheld Electronic Products. JEDEC Solid State Technology Association, 2003, pp. 16
13. T. T. Mattila and J.K. Kivilahti, "Failure Mechanisms of Lead-Free CSP Interconnections Under Fast Mechanical Loading," *Journal of Electronic Materials*, 34, 7, (2005), pp. 969-976
14. T. T. Mattila, P. Marjamäki, and J.K. Kivilahti, "Reliability of CSP Components Under Mechanical Shock Loading" (submitted 2005)
15. T. T. Mattila, T. Laurila, and J. K. Kivilahti, "Metallurgical Factors Behind The Reliability of High Density Lead-Free Interconnections," (Chapter in The Handbook of Lead-Free Soldering, to be published in 2005)
16. Marjamäki, P., Mattila, T., and Kivilahti, J.K., "Finite Element Analysis of Lead-free Drop Test Board," *The Proceedings of the 55th IEEE/EIA CPMT Electronic Component and Technology Conference*, May 31st - June 3rd, 2005, Lake Buena Vista, FL, pp. 462-466
17. T. T. Mattila, J.K. Kivilahti "Impact of Printed Wiring Board Coatings on the Reliability of Lead-Free Chip Scale Package Interconnections," *Journal of Materials Research*, 19, 11, (2004), pp. 3214-3223


National Semiconductor
The Sight & Sound of Information