3-D and Multi-Technology Packaging: Current Capabilities

Phil Marcoux

What is 3-D Packaging?

3-D Packaging is the explosion of new products using old and new packaging and interconnect technologies.
3-D Packaging

Acronyms Galore!

- SIP – System in Package
- SOC – System on Chip
- MCM – Multichip Module
- COB – Chip on Board
- POP – Package on Package

Hybrid – horizontal die

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More Acronyms
(Some of the lesser known)

- CWS – Chip with Sombrero
- CIC – Chip in Cave,
  – or Chip in Cul-de-Sac
- CIT – Chip in Tunnel
- COB – Chip Over Board
- PIP – Package In Package
- DIP – Dice in Package
- POSIP – Package on SIP
- DOPE – Dice On Package Encapsulated

And the all too common:
- IBP – Impossible to Build Package

MCP – Multi-component Package (A generic one we prefer)
3-D SIPs/MCMs/Hybrids/MCPs
What do they have in Common?

- Multiple Components
- Epoxy Fiberglass, Ceramic, Polyimide, Silicon, or Metal substrates
- Soldered SMT components
- Flip Chip ICs
- Wire bonded ICs
- Tape Automated Bonded (TAB) ICs
- Encapsulation
- Look and feel of a common IC package

Less Common

- Wafer Thinning
- Stacked die or stacked packages
- Nested parts
- Multiple substrates in one package
- Insulated wirebonds
- Hermetic parts within non-hermetic packages.
Reasons for Using SIPS

Who’s Using SIPS

Application Breakdown for Stacked Packages, 2005
Benefits of Multi-Chip Packaging

Source: White Electronic Design

- Reduces customer time-to-market
- Reduces design complexity
- Increases operating speeds
- Extends product life

MCP versus Discrete Approach

Combines PowerPC™ + L2 Cache in one package

60% Space Savings

MCP Examples

6. The Smart Power modules from Fairchild Semiconductor employ the SIP concept. As a result, a 15-A module (left) can be converted to a 20-A unit (right) by turning the polygon-shaped ceramic substrate into a rectangular version, leading to lower costs.
MCP Examples

Physical Design

Typical RF SiP Design Flow

Biggest Disruptor is “Creeping Engineering”!
Design Tips

- Bill of Materials
  - The BOM and substrate can be responsible for 60 to 90% of the product cost and 99.99% of the assembly headaches, so we need to choose them wisely.
  - Completeness of the circuit schematic is probably the most important factor affecting design and manufacturing cost and time.
  - Component metal finishes must be compatible with the selected attach process, e.g. mixing leaded with no-lead.
  - Substrates must be designed, panelized, tooled and routed to match the assembly equipment and fixtures.
  - Components must be kitted to match the assembly equipment.

Assuring Optimum Yield – Substrates

- High Tg material
  - (>200 C for lead solder, >240 for No-lead)

- Bondable gold on pads for wire bonds

- Less gold on solder pads
  - (Keep the gold volume < 4% in the solder)

- Provide the substrates to the assembler in approved strips.
Using Thinned Die

- Thinning must be done while die are in wafer form.
  - Depending on how thin you need – Stress Removal to remove sub-surface damage is recommended.

Using Bumped Die

- Best done while in wafer form.
  - However, Stud Bumping is proving to be very viable, especially for prototyping and small volumes.

Au “tolerant” solder, Conductive Epoxy, or Thermosonic Bond
Use RDL Layers

- In case you weren’t aware gold isn’t free.
- Stacked die use a lot of gold.
- RDL layer is usually an Ti/W/Ni/Au layer over the finished IC.
- The RDL layer Redistributes the bonding pads to ease assembly.

This 4 die stack uses 3500 mm of gold wire costing ~$0.60 - $1.00

Use RDL Layers

- Adds ~ $0.10 to $ 0.50 per die
- Enables shorter wires and “waterfall” bond capability
- RDL Sequence:
  - Sputter Barrier metal over passivation (usually Ti/W)
  - Apply liftoff mask layer and pattern
  - Plate on Ni and Au
  - Remove liftoff layer and etch field metal
What Capabilities Should you look for if you plan to outsource your 3-D MCP?

- **Co-Design** (DFM and Quality start with getting the manufacturer involved before the design is completed (“Co-design”).

- Strong Supplier Relationships.

- SMT and flip chip processes.

- Thermosonic conventional and reverse bonding.

- RDL Layer processing.

- DAF (Die Attach Film) die attach.

- Dam and Fill encapsulation.

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Assuring Optimum Yield - **KGD**

- KGD or Known Good Die has long been discussed as the essential ingredient to yield and lower cost.

- CORWIL agrees and has found from experience that 100% die visual inspection and buying die or wafers from reputable sources can assure KGD.

- We encourage using BIST and JTAG for complex die.

- When absolutely needed have the assembler package your critical die in a “minimalist” package, such as a QFN for electrical testing and burn-in prior to MCP assembly.

- Having quality manufacturing practices is a must.
Assuring Optimum Yield – Wire Bond

• Proper wire bond pads:
  – “Bondable gold” (Note 1) vs. solderable gold
    – Bondable Au may require electrolytic Au and plating bars, but >25 microinches of electroless Au over 100 to 150 microinches of electroless Ni seems to bond well.
    – Adequate bond pad – Nominal and low power traces
  • For Au (thermosonic ball):
    – 18µ wire – min. pad FLAT width = 40µ; min pitch = 55µ
    – 25µ wire – min. pad FLAT width = 48µ; min pitch = 60µ
    – 33µ wire – min. pad FLAT width = 65µ; min pitch = 80µ
    – Length = 4X the wire diameter
  • For Al (ultrasonic wedge) –
    – Width = 50µ
    – Length = 75µ

Note 1: A misnomer since the purpose of the gold is to prevent oxidation of the Ni so it’s capable of bonding with the gold wire.

Assuring Optimum Yield – Wire Bond

• Example of an IBP*

• Poorly designed die result in messy, difficult bond-outs.

IBP = Impossible to Build Package
Assuring Optimum Yield – Wire Bond

• Avoid excessive die overhang
  – Excess overhang can lead to microcracking in the overhanging die.
  – Amount of allowable overhang depends on the capabilities (specifically downbond force) of your assembler's bonder.

Source: KnS

Possible Excess Overhang
Possible Crack Site

Assuring Optimum Yield – Wire Bond

• Proper wire bond pads:
  – Adequate bond pad – thick power traces
    • For either Au or Al – there must be a FLAT area equal to the area requested for the low power bond pads (prior slide).
  – Thin dielectrics on Substrate
    • May require trace keepout
  – Low-k dielectrics on Die
    • NOTIFY Your Assembler!

<table>
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<th>Bond Type</th>
<th>Bonding Mechanism</th>
<th>Wire</th>
<th>Temp.</th>
<th>Ultrasound</th>
<th>Pressure</th>
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<tr>
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<td>Au</td>
<td>Elevated (~150°C)</td>
<td>Yes</td>
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Source: Myleck Components Corp.
Assuring Optimum Yield - Soldering

- Proper flip chip pads and SMT lands:
  - Pad and land area should match manufacturer recommendations.
  - Solderable gold needs to be thin (< 4% vol. to avoid embrittlement)
    - We prefer a min. of 3 to 5 microinches of immersion AU over 100 to 150 microinches of electroless Ni, commonly called “ENiC”.
  - Adequate land hold down
    - Tiny SMT components can overheat when mixed with large mass parts. Land hold downs minimize pad lift.
  - Thin dielectrics
    - May require special reflow control to avoid delamination.

Summary

3-D Packaging is in usage. Applications are using wafer thinning, WLP, SMT processes, flip chip, reverse bonding, stud bumping, and more. Benefits include shorter time-to-market, lower development costs, smaller size.

Launch yours today!