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Board Level Reliability of Wafer Level Chip Scale Packages With Copper Post Technology


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Analog Devices, Inc.



Presentation Outline

- ◆ **Introduction**
 - Background
 - Objective
- ◆ **Experimental Section**
 - Materials
 - Test Methodology
- ◆ **Results & Discussions**
 - Time Zero / Failures
 - Weibull Distributions
- ◆ **Conclusions**
- ◆ **Recommendation**


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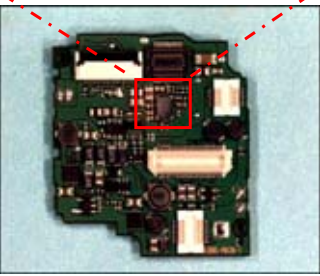
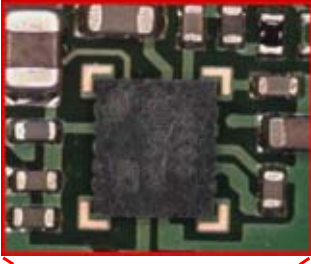
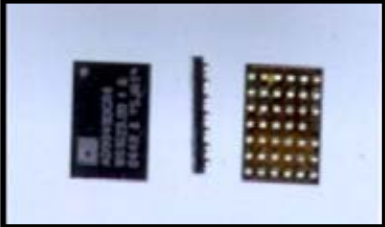
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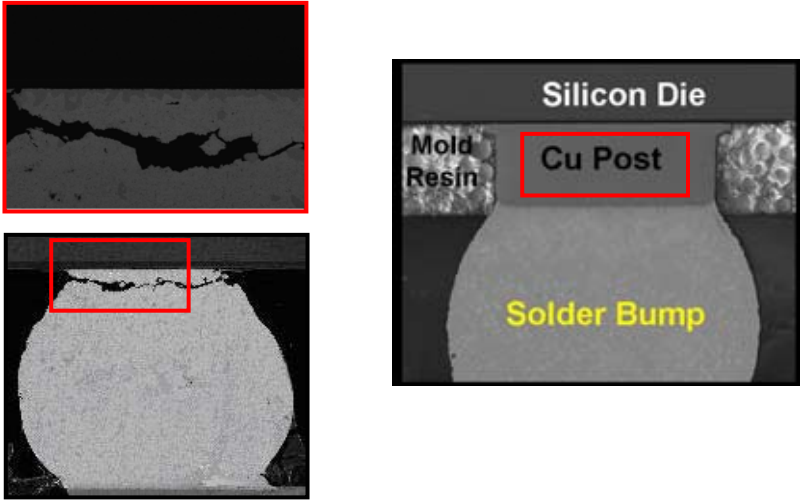
Background



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WLCSP Typical Failure at TC

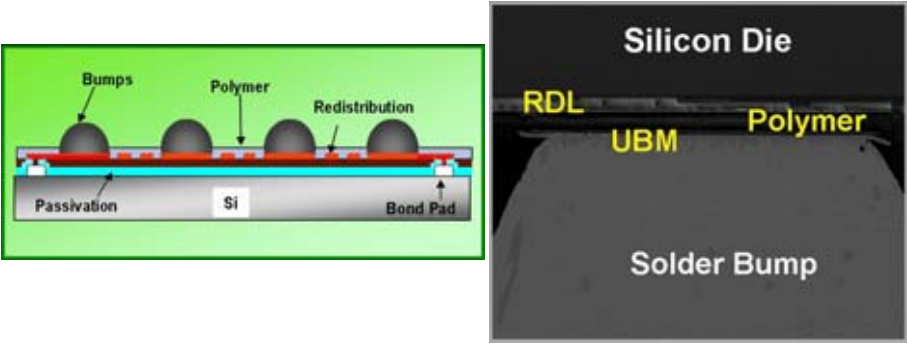


The slide displays two micrographs on the left and a cross-sectional diagram on the right. The top micrograph shows a dark, irregular crack across the top surface of a component. The bottom micrograph shows a similar crack, but with a red box highlighting a specific area. The cross-sectional diagram on the right shows a 'Silicon Die' at the top, with 'Mold Resin' on either side. Below the die is a 'Cu Post', which is highlighted with a red box. At the bottom of the diagram is a 'Solder Bump'.

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WLCSP Structures - Typical

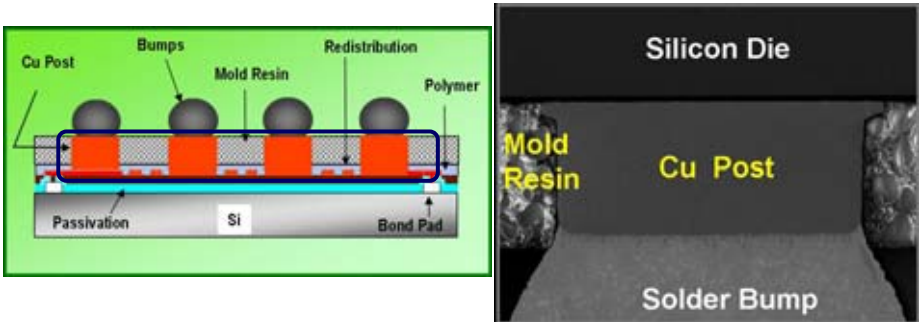


The slide features a schematic diagram on the left and a cross-sectional diagram on the right. The schematic shows a cross-section of a silicon die with 'Passivation' on top. Below the passivation is a 'Si' layer. On the surface, there are 'Bumps', a 'Polymer' layer, and 'Redistribution' lines. A 'Bond Pad' is also indicated. The cross-sectional diagram on the right shows a 'Silicon Die' at the top, with 'RDL' (Redistribution Layer) and 'UBM' (Under Bump Metal) layers. A 'Polymer' layer is also shown. At the bottom is a 'Solder Bump'.


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WLCSP Structures - Copper Post

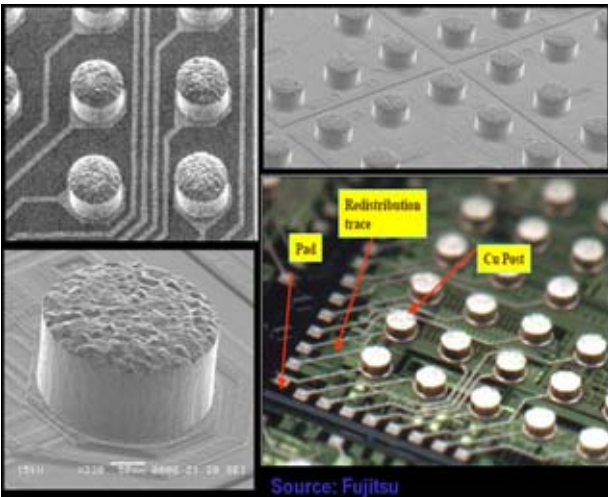


The diagram on the left shows a cross-section of a WLCSP structure. It features a silicon die on top, with a passivation layer below it. A layer of copper (Cu) is deposited on the die, forming copper posts (Cu Post) and a redistribution layer. Mold resin is applied over the copper, and a polymer layer is added on top. Solder bumps are attached to the copper posts. The silicon die is labeled 'Si', and the bond pad is labeled 'Bond Pad'. The diagram on the right is a scanning electron microscope (SEM) image showing the structure from a different perspective, with labels for 'Silicon Die', 'Mold Resin', 'Cu Post', and 'Solder Bump'.




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Copper Post Technology



The image shows three SEM images and a photograph of a printed circuit board (PCB) with copper posts. The top-left SEM image shows a close-up of a copper post. The top-right SEM image shows a grid of copper posts. The bottom-left SEM image shows a cross-section of a copper post. The bottom-right photograph shows a PCB with copper posts and redistribution traces. Labels in the photograph include 'Redistribution trace', 'Pad', and 'Cu Post'. The source is cited as 'Source: Fujitsu'.



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Objectives

Evaluate the thermal cycle performance of a standard WLCSP and the effect of the adding Copper post.

- Effect of Underfill , Underfill Material
- Passivation Polymer Material
- RDL Material , Width


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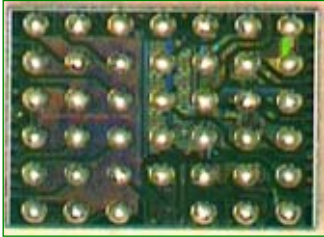
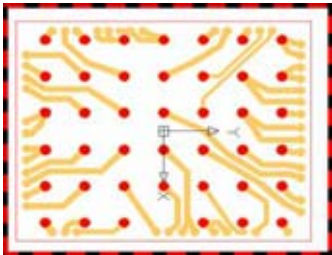
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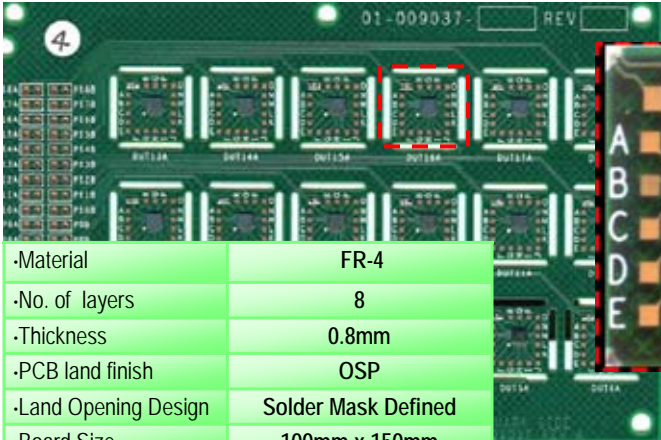
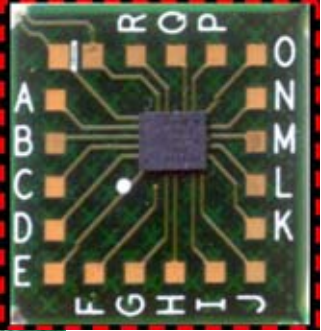
Daisy Chain Die


Die Dimensions	
I/O	41
Ball Array	6x7
Bump Comp	SnAgCu (3.0/0.5)
Die Size	2.67 x 3.32mm
Bump Dia	0.25 +/- 0.045
Bump Pitch	0.450
Bump Ht	0.207 +/- 0.025
Pkg Height	0.563

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PCB Properties & Layout

·Material	FR-4
·No. of layers	8
·Thickness	0.8mm
·PCB land finish	OSP
·Land Opening Design	Solder Mask Defined
·Board Size	100mm x 150mm
·No of DUT	18-Top/Bottom Side

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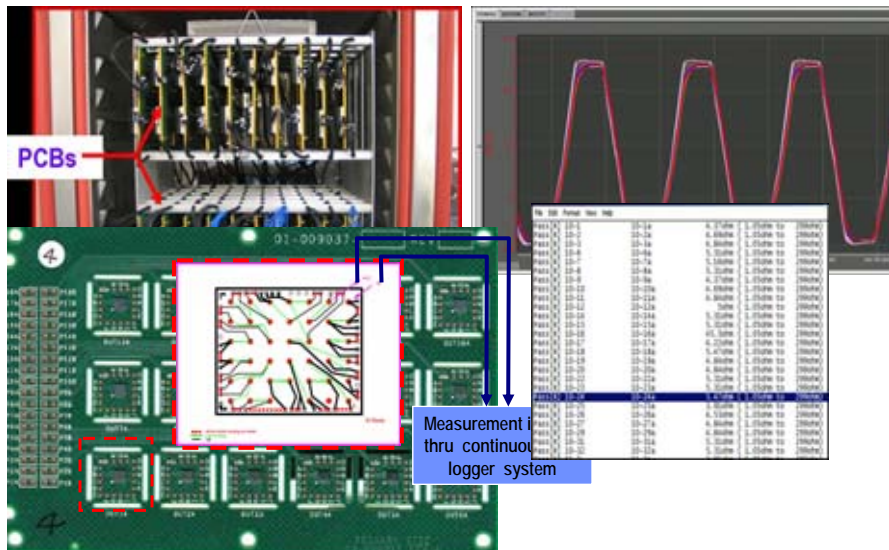
Experimental Matrix

Leg	Bump Process / RDL /Polymer	Cu Post	Under fill	No of Units /
1	Redistributed by Bump Fab – Cu 70um PI	Yes	NO	64
2	Redistributed by Bump Fab –Cu 70um PI	Yes	Mat A	64
3	Redistributed by Bump Fab – Cu 20um PI	Yes	Mat A	64
4	Redistributed by Wafer Fab – Al 70um SiO2	Yes	NO	64
5	Redistributed by Wafer Fab – Al 70um SiO2	Yes	Mat A	64
6	Redistributed by Wafer Fab – Al 70um SiO2	Yes	Mat B	64
7	Redistributed by Bump Fab- Al 70um 5;5 PI	No	NO	64
8	Redistributed by Bump Fab- Al 70um 10;5 PI	No	Mat A	62
9	Redistributed by Bump Fab- Al 70um 5;5 PI	No	Mat A	62
10	Redistributed by Bump Fab- Al 70um BCB	No	NO	64
11	Redistributed by Bump Fab- Al 70um BCB	No	Mat A	64

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Test Methodology



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ANALOG DEVICES

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Base Line Solder Joint- Cu Post

Leg	Bump Process / RDL / Polymer	Cu Post	Under fill	Solder Joint t=0
1	Redistributed by Bump Fab – Cu 70um PI	Yes	NO	
2	Redistributed by Bump Fab –Cu 70um PI	Yes	Mat A	
3	Redistributed by Bump Fab – Cu 20um PI	Yes	Mat A	
4	Redistributed by Wafer Fab – Al 70um SiO2	Yes	NO	
5	Redistributed by Wafer Fab – Al 70um SiO2	Yes	Mat A	
6	Redistributed by Wafer Fab – Al 70um SiO2	Yes	Mat B	

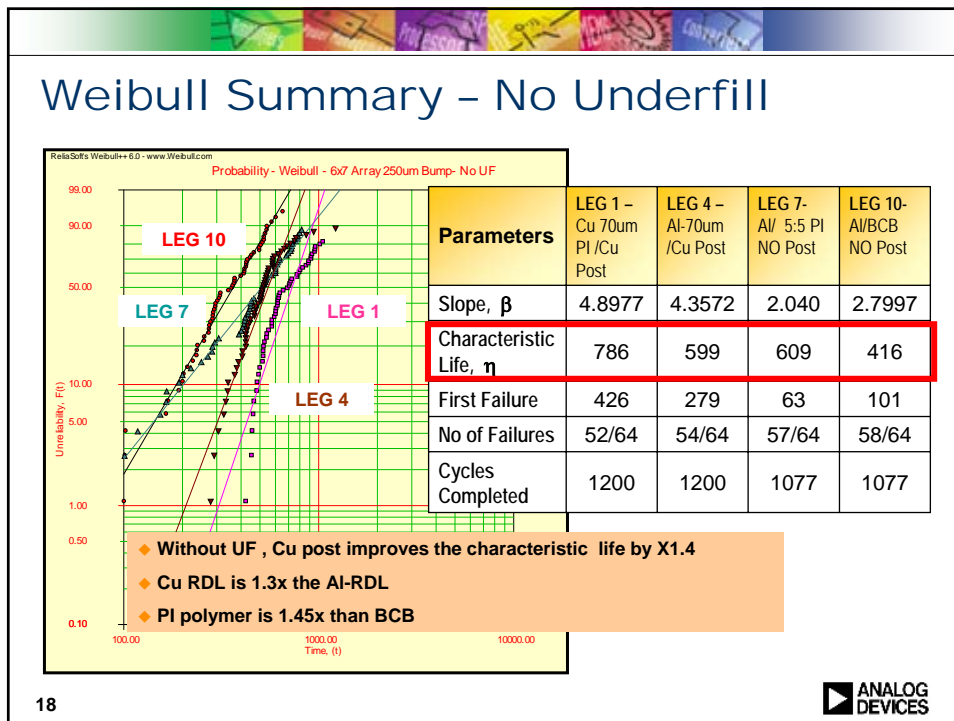
ANALOG DEVICES

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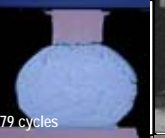
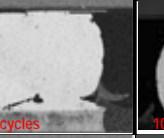
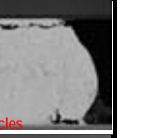
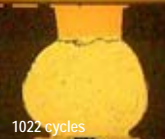

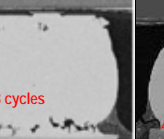
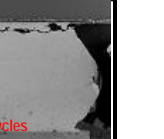
Base Line Solder Joint- NO Cu Post

Leg	Bump Process / RDL /Polymer	Cu Post	Under fill	Solder Joint t=0
7	Redistributed by Bump Fab- Al 70um 5;5 PI	No	NO	
8	Redistributed by Bump Fab- Al 70um 10;5 PI	No	Mat A	
9	Redistributed by Bump Fab- Al 70um 5;5 PI	No	Mat A	
10	Redistributed by Bump Fab- Al 70um BCB	No	NO	
11	Redistributed by Bump Fab- Al 70um BCB	No	Mat A	


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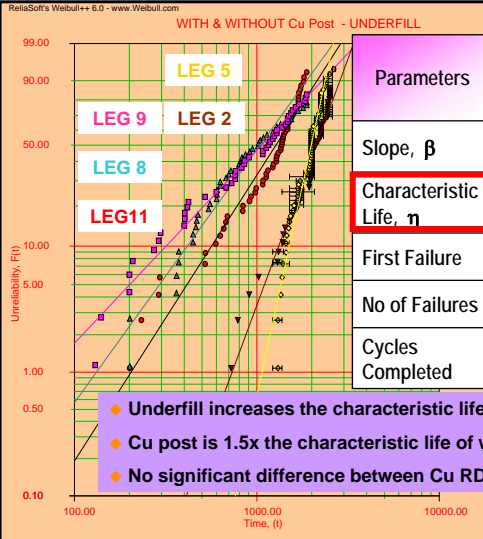
Failures – No Underfill

	LEG 1 –Cu 70um PI /Cu Post	LEG 4 – Al-70um /Cu Post	LEG 7- Al/ 5:5 PI NO Post	LEG 10- Al/BCB NO Post
Early	 420 cycles	 279 cycles	 154 cycles	 102 cycles
Later	 1022 cycles	 1220 cycles	 818 cycles	 448 cycles

◆ LEG 7 which uses PI dielectrics showed different failure mode, i.e. cracks appear on the substrate side


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Weibull Summary – WITH Underfill



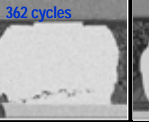
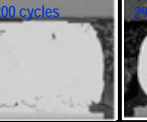
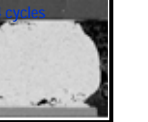


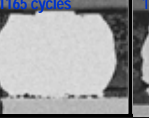
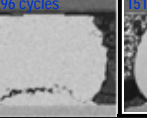
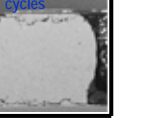


Parameters	LEG 2- Cu 70um PI /Cu Post	LEG 5 – Al-70um /Cu Post	LEG 8- Al/ 10:5 PI NO Post	LEG 9 Al/ 5:5 PI NO Post	LEG 11- Al/BCB NO Post
Slope, β	3.9914	6.8229	2.0493	1.5657	2.3172
Characteristic Life, η	2317	2096	1247	1339	1490
First Failure	723	1220	201	130	201
No of Failures	54/64	58/64	45/62	45/62	55/64
Cycles Completed	2702	2702	1900	1900	1900


- ◆ Underfill increases the characteristic life by 3x of the No UF.
- ◆ Cu post is 1.5x the characteristic life of without Cu post.
- ◆ No significant difference between Cu RDL and Al-RDL

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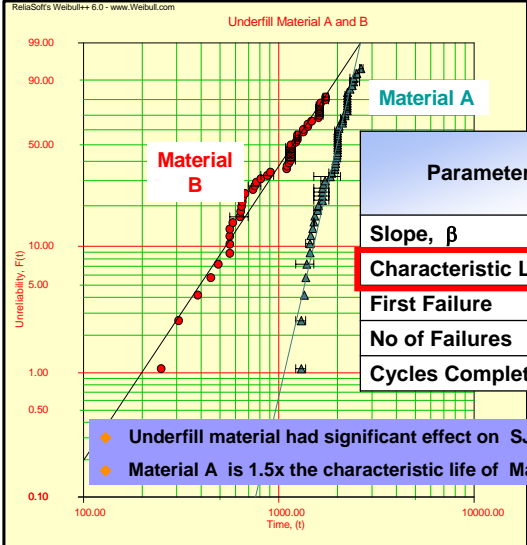
Failures – With Underfill

	LEG 2–Cu 70um PI /Cu Post	LEG 5 – Al-70um /Cu Post	LEG 8- Al/ 10:5 PI NO Post	LEG 9- Al/ 5:5 PI NO Post	LEG 11- Al/BCB NO Post
Early	 723 cycles	 1220 cycles	 362 cycles	 200 cycles	 400 cycles
Later	 2591 cycles	 2702 cycles	 1165 cycles	 1294 cycles	 1511 cycles

◆ **With Underfill, failures have shifted to solder – substrate interface.**


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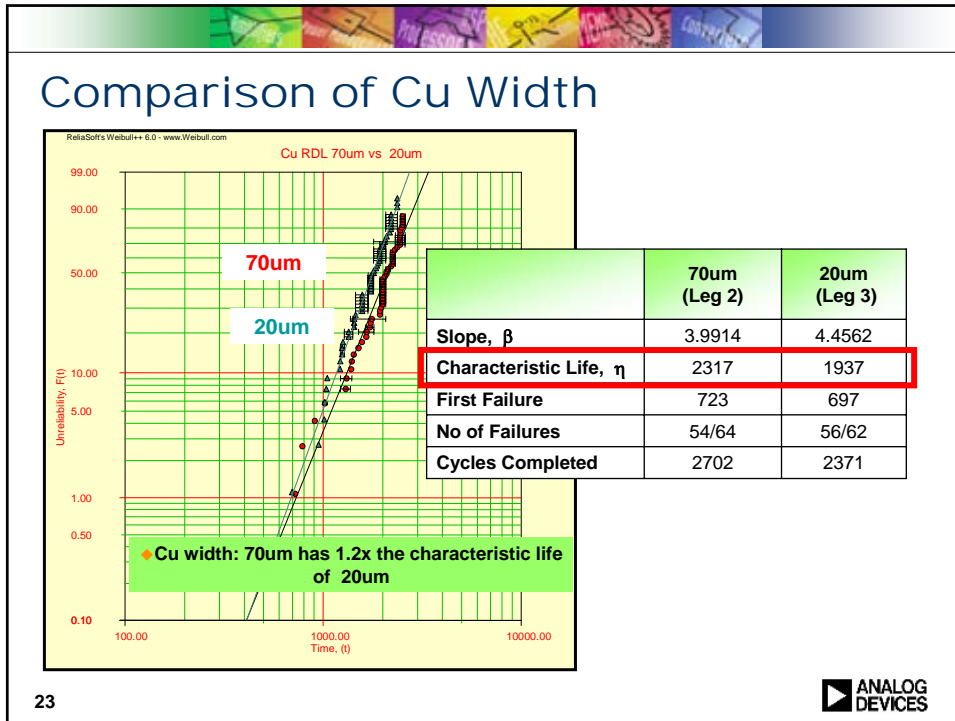
Comparison of Underfill



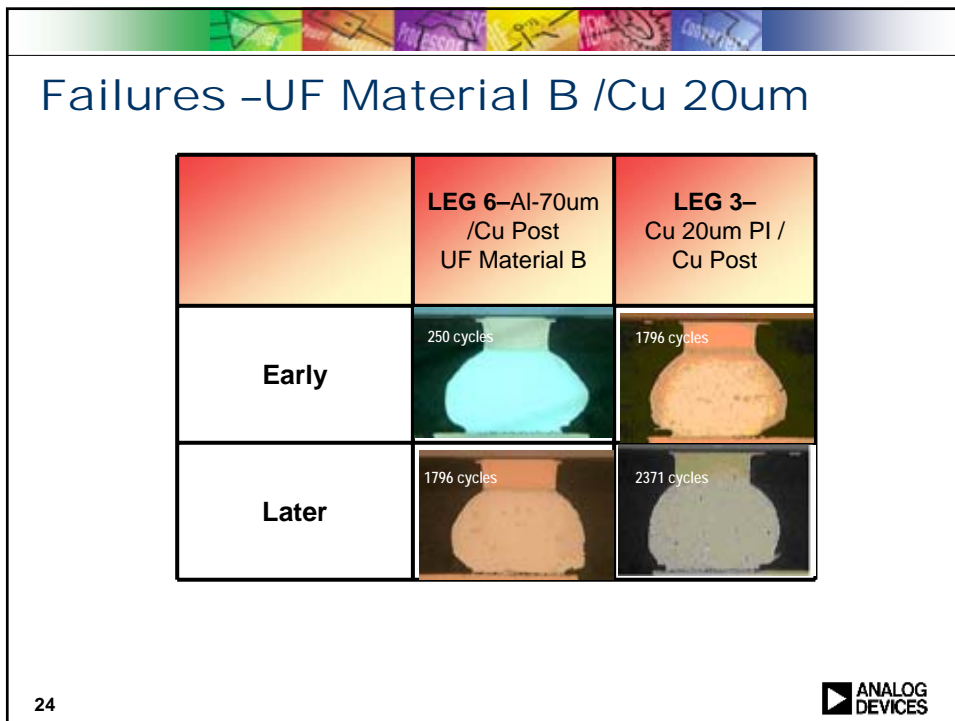
Parameters	Material A (Leg 5)	Material B (Leg 6)
Slope, β	6.8229	2.3737
Characteristic Life, η	2096	1378
First Failure	1220	250
No of Failures	58/64	50/64
Cycles Completed	2702	1933

- ◆ Underfill material had significant effect on SJR
- ◆ Material A is 1.5x the characteristic life of Material B.


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Conclusions

- ◆ **Copper Post Structures improved the WLCSP characteristic life by at least 1.4 times.**
- ◆ **Underfill significantly increases the solder joint life by >3x.**
 - **Ideally, the underfill material will force the failure site from die side to substrate side.**
- ◆ **Passivation polymers can influence the solder joint reliability of WLCSP**
 - **Can also shift the location of the failure from die to substrate side even without underfill.**

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Recommendation

- ◆ **Copper post technology is a good option for WLCSP applications**
 - greater level of solder joint reliability
 - good solder electro-migration resistance
 - higher current densities.

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