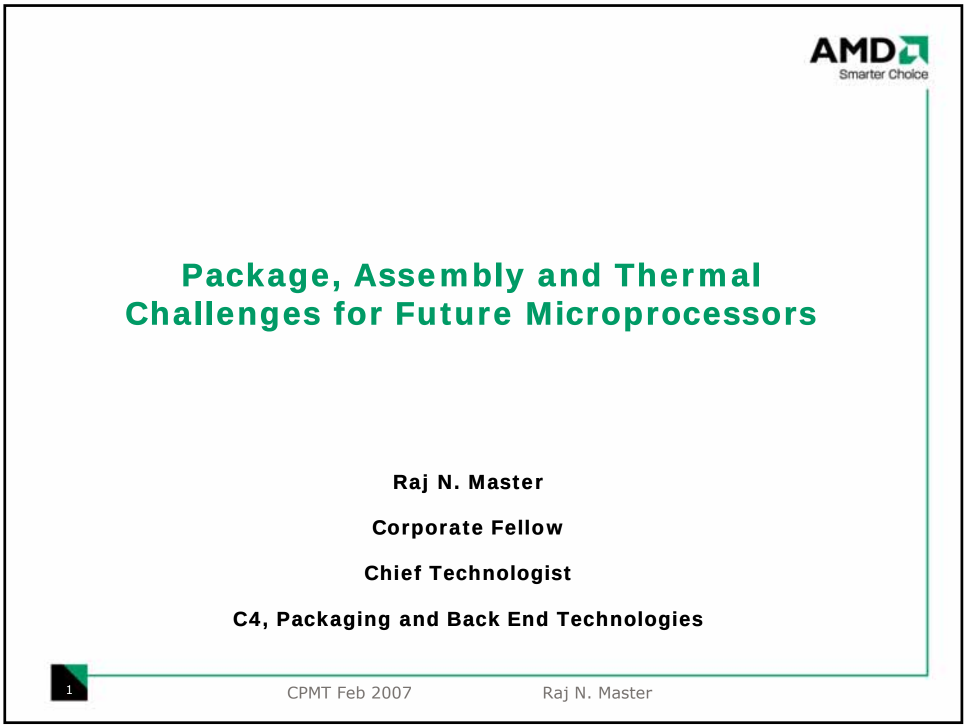


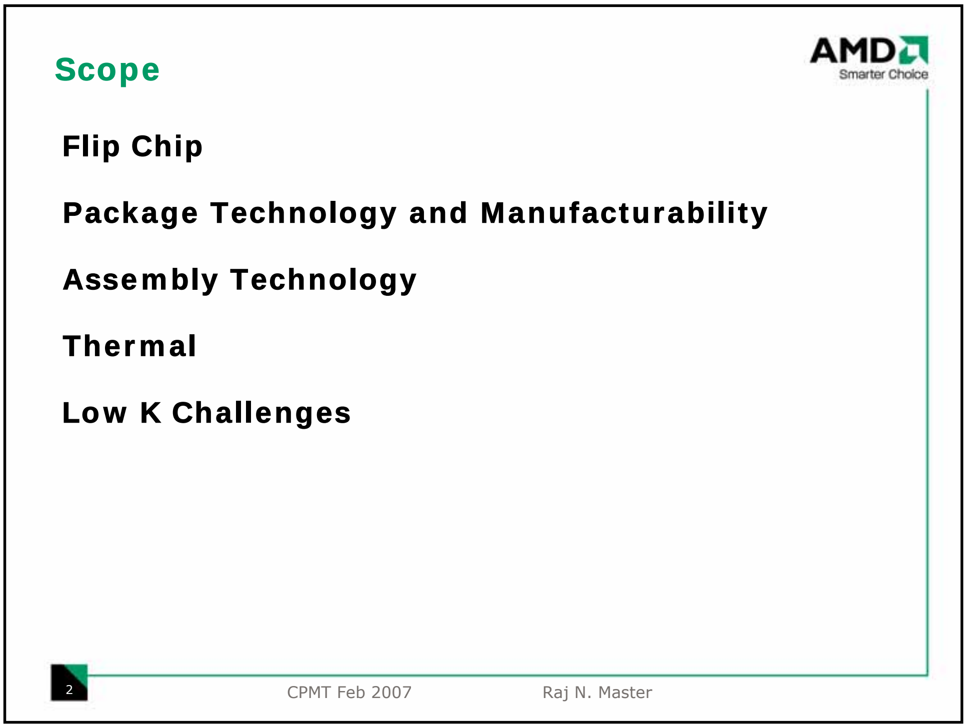
Package, Assembly and Thermal Challenges for Future Microprocessors

Raj N. Master

Corporate Fellow

Chief Technologist

C4, Packaging and Back End Technologies



Scope

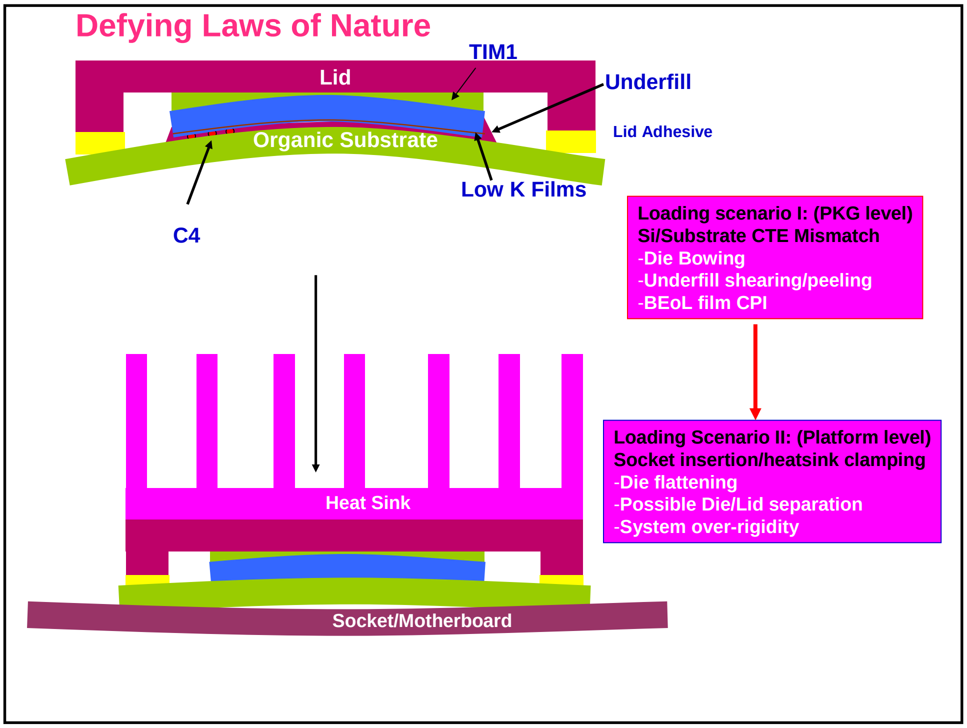
Flip Chip

Package Technology and Manufacturability

Assembly Technology

Thermal

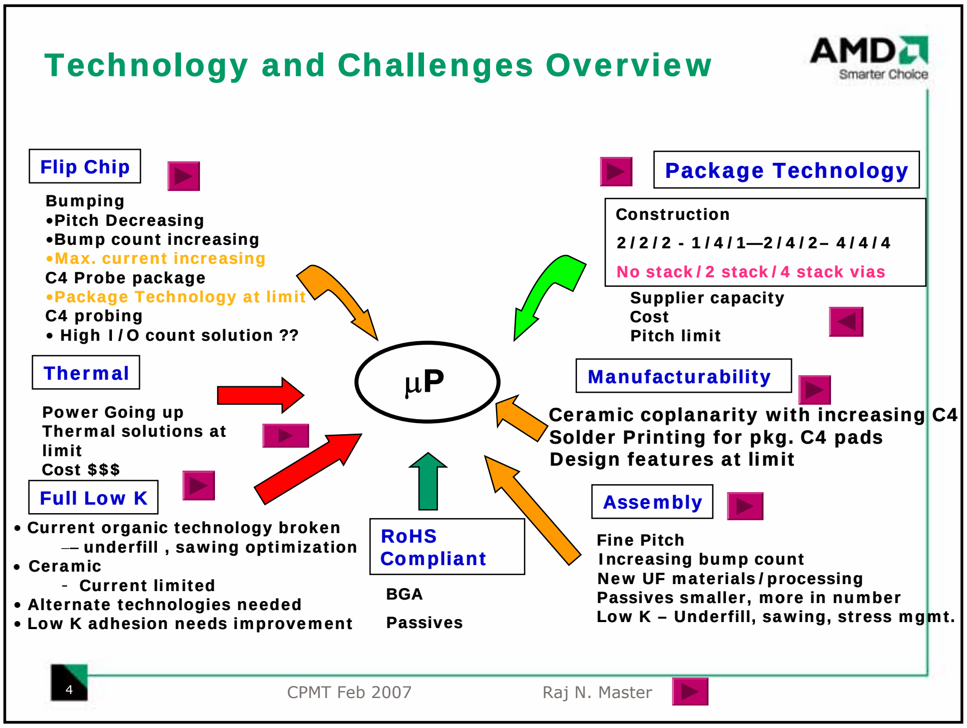
Low K Challenges



Defying Laws of Nature

Loading scenario I: (PKG level)
Si/Substrate CTE Mismatch
-Die Bowing
-Underfill shearing/peeling
-BEoL film CPI

Loading Scenario II: (Platform level)
Socket insertion/heatsink clamping
-Die flattening
-Possible Die/Lid separation
-System over-rigidity



Technology and Challenges Overview

AMD Smarter Choice

Flip Chip

Bumping
- Pitch Decreasing
- Bump count increasing
- Max. current increasing

C4 Probe package
- Package Technology at limit

C4 probing
- High I/O count solution ??

Thermal

Power Going up
Thermal solutions at limit
Cost $$$

Full Low K

- Current organic technology broken
  - — underfill , sawing optimization
- Ceramic
  - Current limited
- Alternate technologies needed
- Low K adhesion needs improvement

RoHS Compliant

BGA

Passives

Package Technology

Construction
2/2/2 - 1/4/1—2/4/2– 4/4/4
No stack/2 stack/4 stack vias

Supplier capacity
Cost
Pitch limit

Manufacturability

Ceramic coplanarity with increasing C4
Solder Printing for pkg. C4 pads
Design features at limit

Assembly

Fine Pitch
Increasing bump count
New UF materials/processing
Passives smaller, more in number
Low K – Underfill, sawing, stress mgmt.

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Flip Chip Challenges

Pitch Decreasing from 350 μ ---→ 150 μ --→ ??

No. of bumps increasing ---→ 5 – 10 K per die

- **Bumping Choice**
  - **Electroplating --- Uniformity, extendibility, low defect rate**
  - **Screen printing --- Limited by Solder paste, stencil printing, voids**
- **Current Carrying capability**
  - **Current Density increasing -→ limit pitch decrease**
    - **Bump and die at UBM via opening**
- **Joule Heating significant**
- **Choice of Solder**
  - **Eutectic Solder not suitable for EM**
  - **High Lead solders should be used**

Alternate bumping / interconnection technologies required

- **Bump less**
- **Pillar bumping**
- **Compliant springs, Nano links**

Bump Geometry

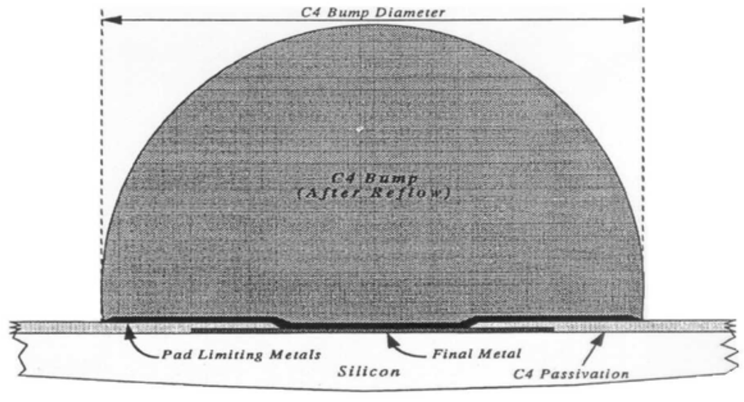
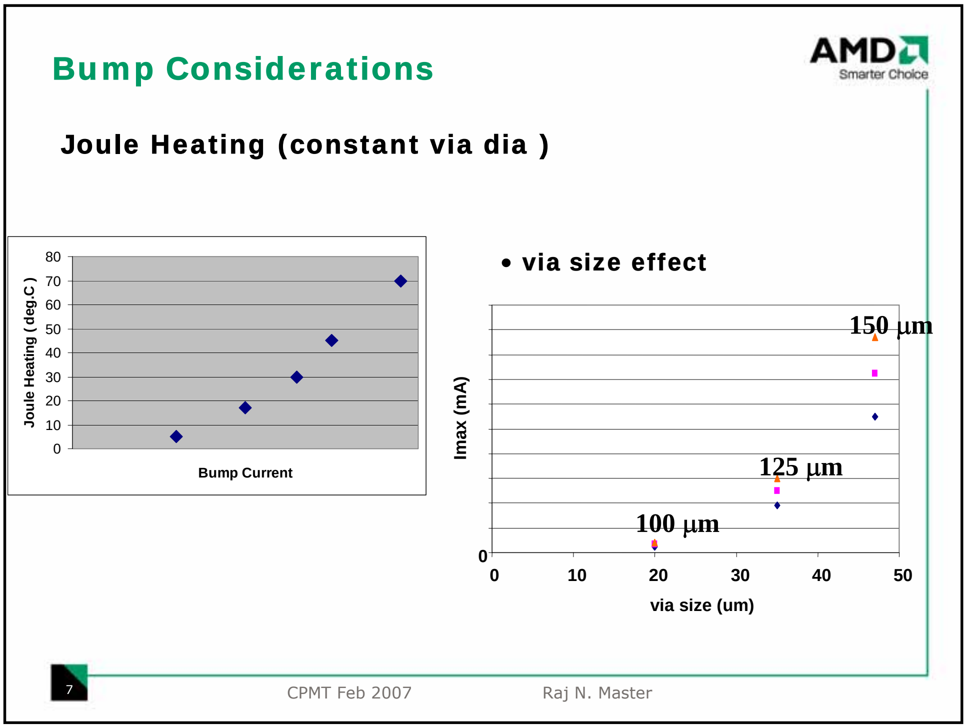


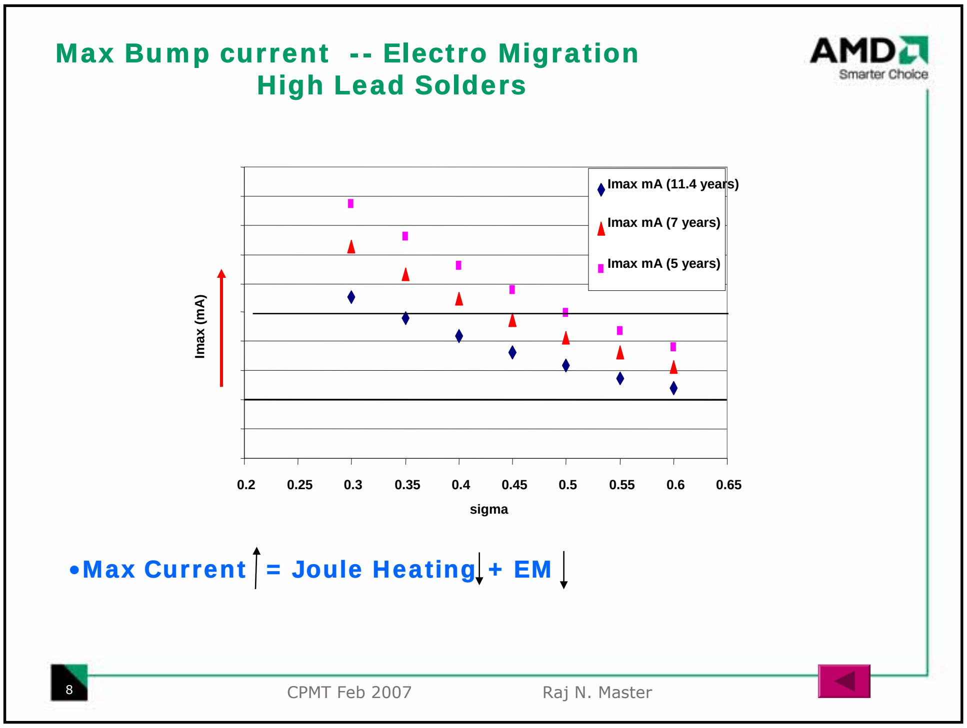
Figure 11 - A C4 Bump After Reflow



Bump Considerations

Joule Heating (constant via dia)

- **via size effect**



Max Bump current -- Electro Migration High Lead Solders

•Max Current ↑ = Joule Heating ↓ + EM ↓

Package Choice Criterion

Electrical Performance

Cost

Consistent supply of packages

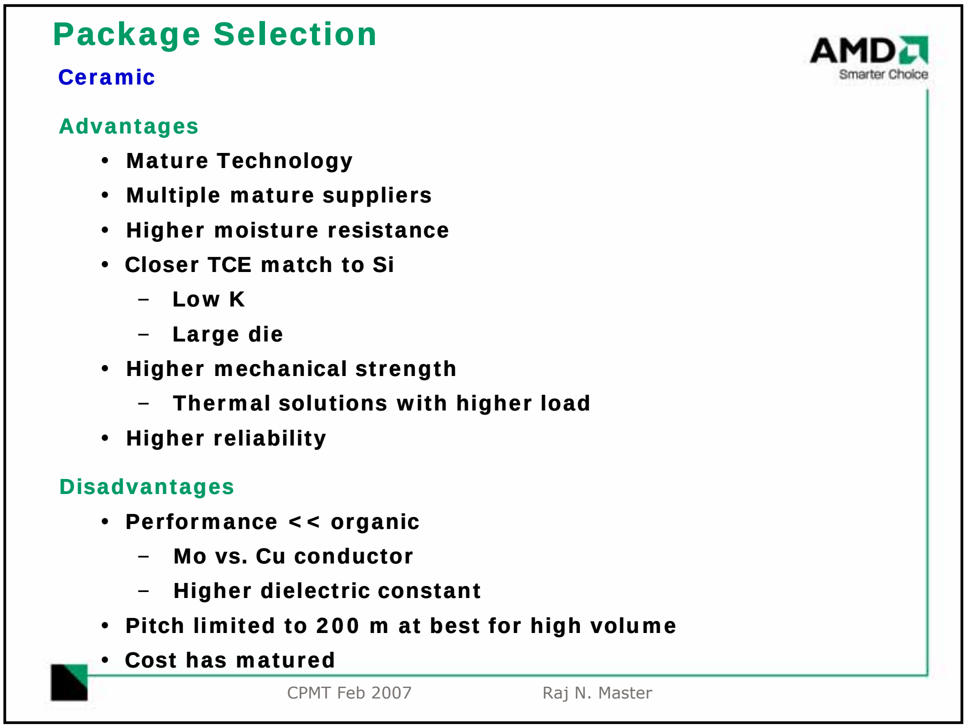
Reliability

Packaging Choices

Reliability
- **Board Level**
- **C4**

Board Level
- **Organic ----- CTE = 18**
- **Solder Columns for ceramic**
- **High TCE Ceramic ---- CTE = 12 (Single Source)**

C4
- **Organic**



Package Selection

Ceramic

Advantages

- Mature Technology
- Multiple mature suppliers
- Higher moisture resistance
- Closer TCE match to Si
  - Low K
  - Large die
- Higher mechanical strength
  - Thermal solutions with higher load
- Higher reliability

Disadvantages

- Performance << organic
  - Mo vs. Cu conductor
  - Higher dielectric constant
- Pitch limited to 200 m at best for high volume
- Cost has matured

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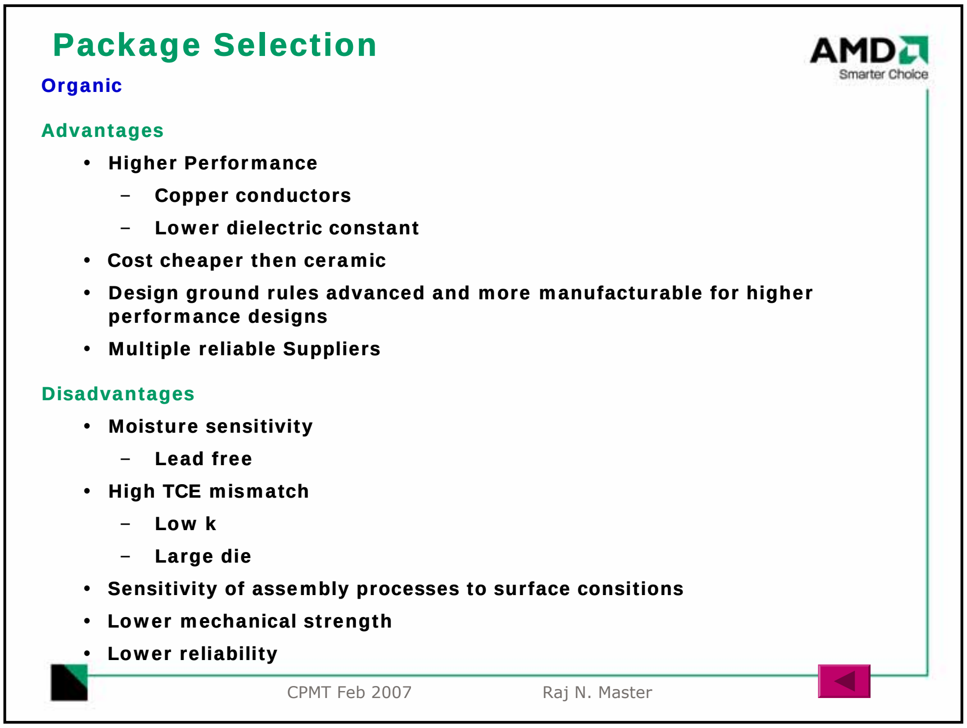

Package Selection

Organic

Advantages

- Higher Performance
  - Copper conductors
  - Lower dielectric constant
- Cost cheaper then ceramic
- Design ground rules advanced and more manufacturable for higher performance designs
- Multiple reliable Suppliers

Disadvantages

- Moisture sensitivity
  - Lead free
- High TCE mismatch
  - Low k
  - Large die
- Sensitivity of assembly processes to surface consitions
- Lower mechanical strength
- Lower reliability

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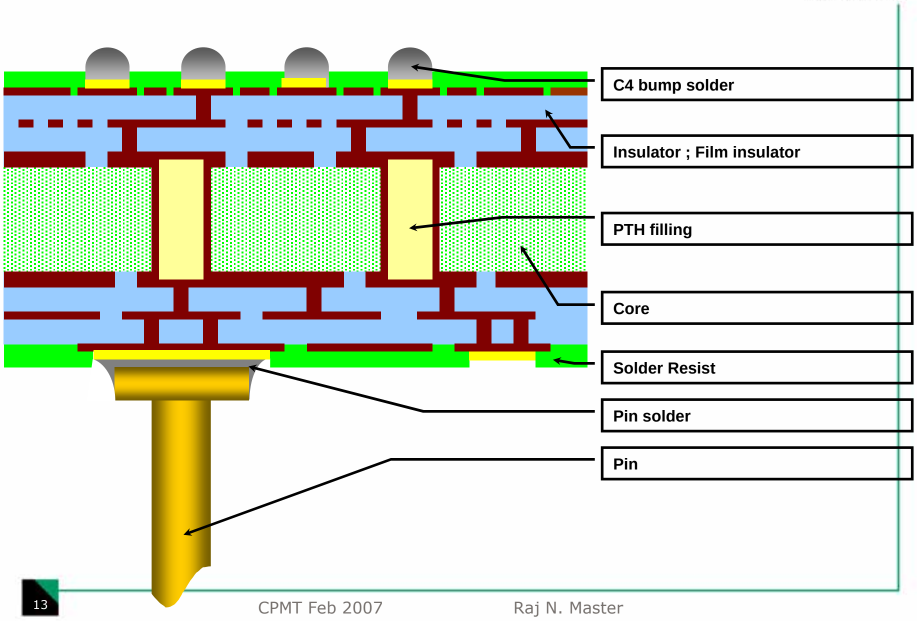
Organic Structure



C4 bump solder

Insulator ; Film insulator

PTH filling

Core

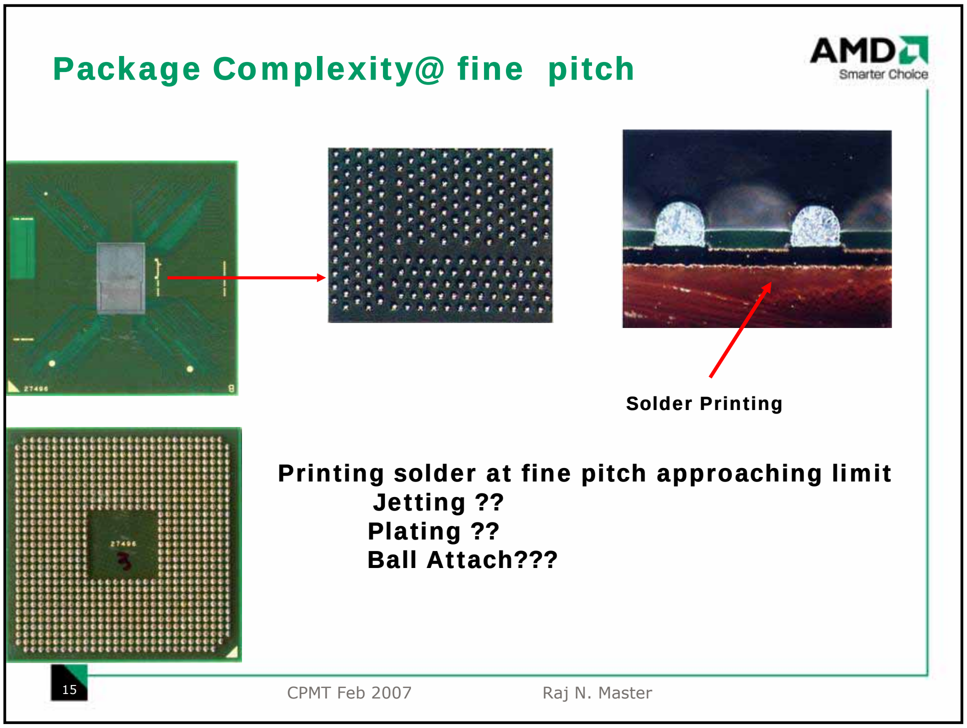
Solder Resist

Pin solder

Pin

Package Challenges

- **Increased functionality and larger die**
  - **Finer Pitch**
    - **Ceramic ……. 200 µ**
    - **Organic ……. 180 – 150 µ**
  - **Larger body sizes to route**
    - **Ceramic ….. Finer features not manufacturable**
    - **Organic …… Finer features possible requires material and process changes**
- **Need for increased decoupling capacitance**
  - **Higher cost …. Larger body size**
  - **Embedded capacitance breakthrough needed**
- **Suppliers have different material sets**



Package Complexity@ fine pitch

Solder Printing

Printing solder at fine pitch approaching limit
- Jetting ??
- Plating ??
- Ball Attach???

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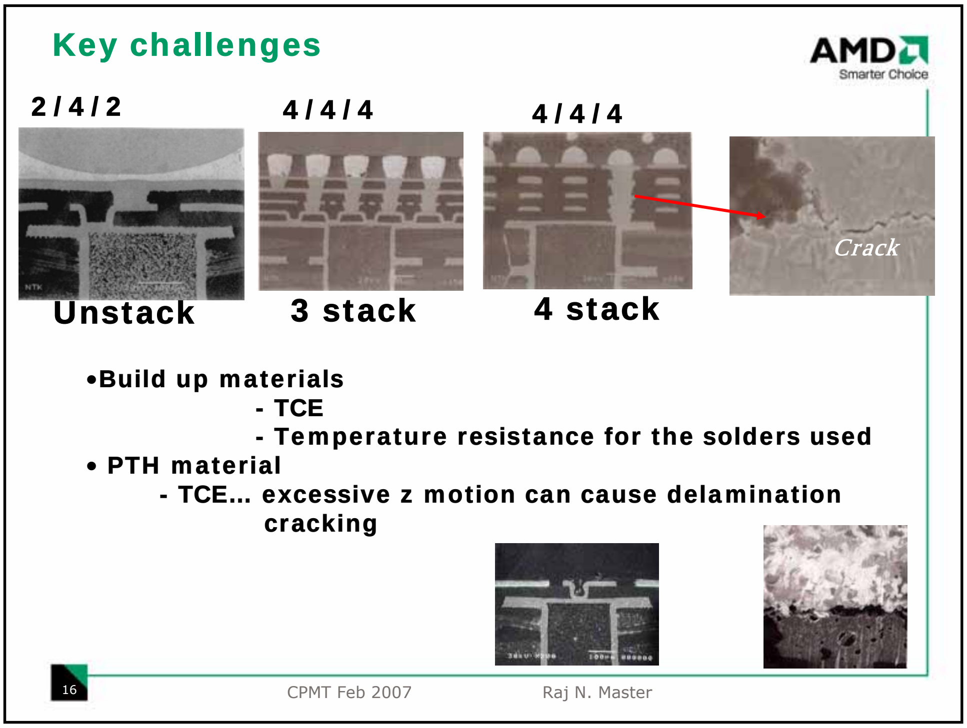

Key challenges

Unstack 3 stack 4 stack

- Build up materials
  - TCE
  - Temperature resistance for the solders used
- PTH material
  - TCE… excessive z motion can cause delamination cracking

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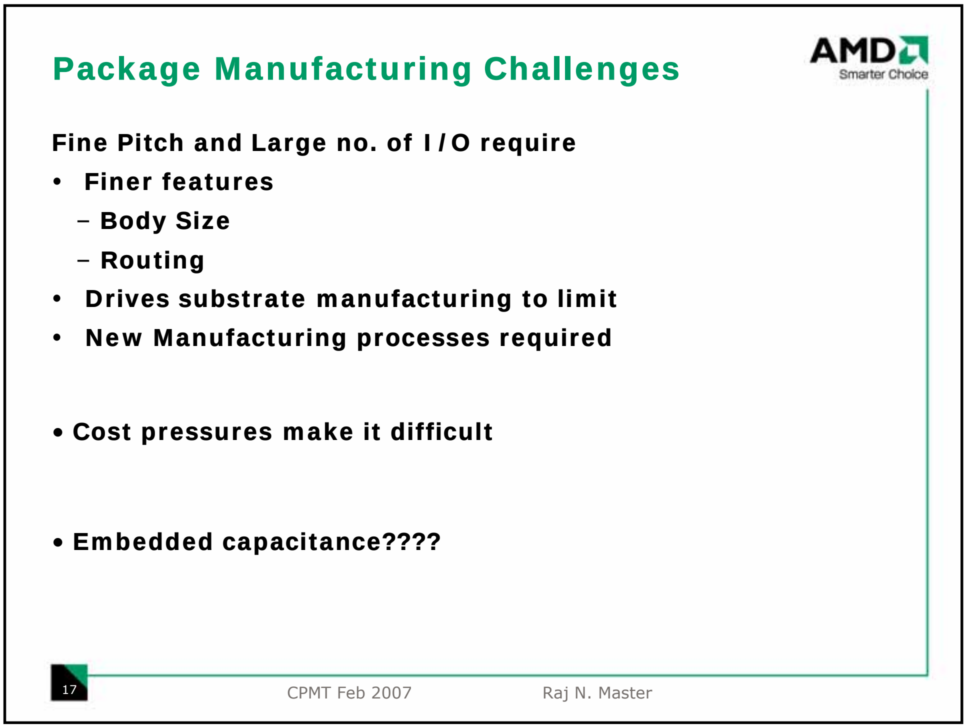


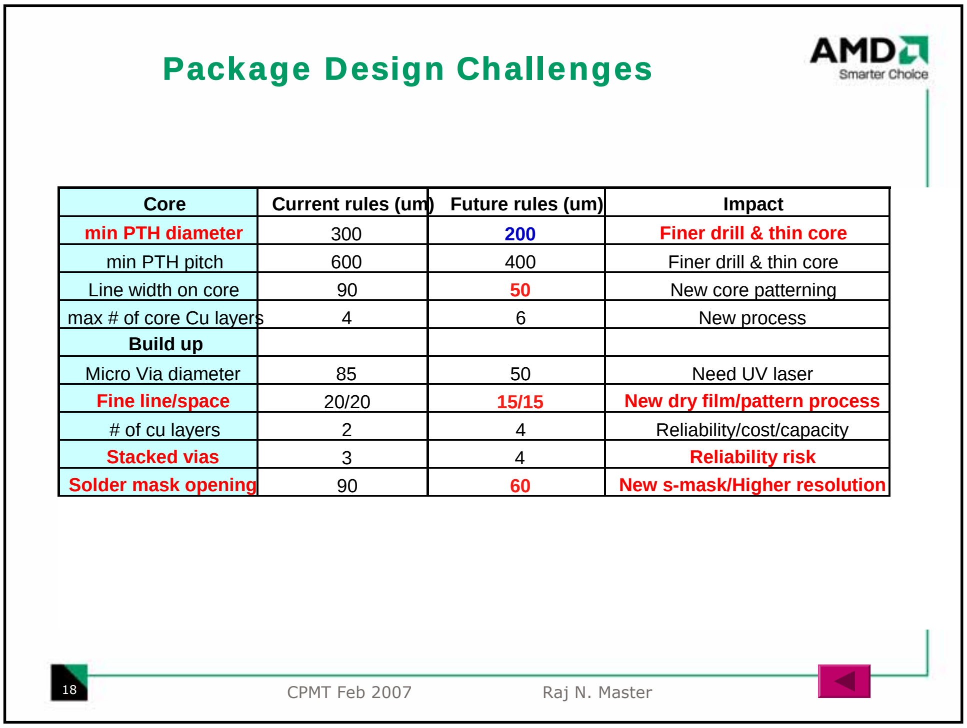
Package Manufacturing Challenges

Fine Pitch and Large no. of I / O require

- **Finer features**
  - **Body Size**
  - **Routing**
- **Drives substrate manufacturing to limit**
- **New Manufacturing processes required**

- **Cost pressures make it difficult**

- **Embedded capacitance????**



Package Design Challenges

Core	Current rules (um)	Future rules (um)	Impact
min PTH diameter	300	**200**	**Finer drill & thin core**
min PTH pitch	600	400	Finer drill & thin core
Line width on core	90	**50**	New core patterning
max # of core Cu layers	4	6	New process
Build up			
Micro Via diameter	85	50	Need UV laser
Fine line/space	20/20	**15/15**	**New dry film/pattern process**
# of cu layers	2	4	Reliability/cost/capacity
Stacked vias	3	4	**Reliability risk**
Solder mask opening	90	**60**	**New s-mask/Higher resolution**

Assembly

Chip Placement

Finer pitch drives higher accuracy

- **Slows down UPH**

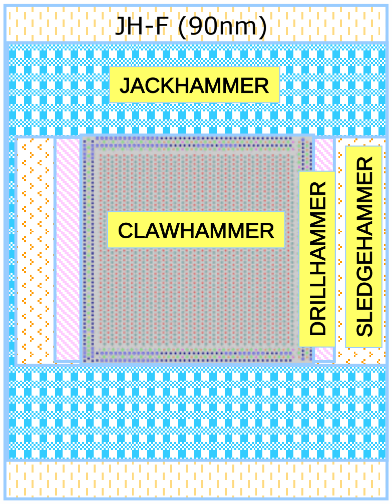
Large die and finer pitch

- **Stringent bump and package co planarity**

New fluxes required

- **Low residue for larger area**
- **Compatibility with under fills**
- **Oxide removal**

Die footprints…… Die and Bump counts getting larger



CH 7.98 x 8.71	2821
DH 9.71 x 8.59	3490
SH 12.89 x 8.75	4676
JH 13.1 x 15.5	8876
JH 13.1 x 17.5	10000

What will they think next!!!!!!!

Assembly

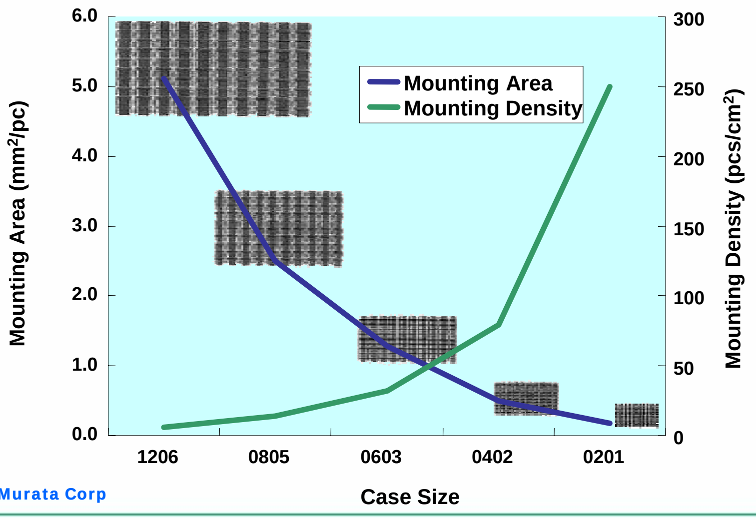
UF materials

- Finer particle size for lower standoff as pitch decreases
  - Solids loading decreases due to high surface area
  - Effects physical and mechanical properties
- Optimized physical / mechanical properties
  - Large die
  - Low K

UF processes

- Finer P.S.D. slows down the conventional UF dispense
- Sensitivity to Solder mask surfaces increases
- New approaches for high volume manufacturing??
  - Novel dispensing methods
    - Jetting
    - Multiple needles (5 -10 simultaneously)
  - No Flow UF ??
  - Wafer applied UF ??
- Defects become more critical

Passives Roadmap



Courtsey: Murata Corp

Assembly

Passives attachment

- **Numbers are increasing**

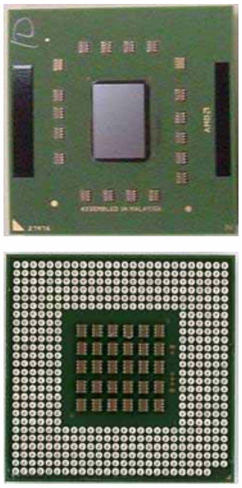
Evolution

- **SMT**
- **Multi terminal LLA, IDC**
- **Resistors**
- **Smaller sizes**

Processes and defects

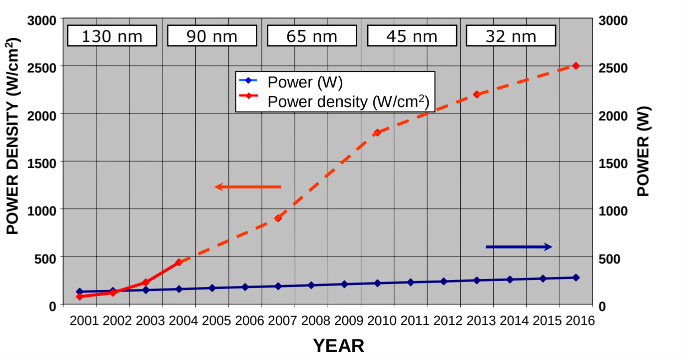
- **Dispensing at limit…. Shorting,tombstoning;unbalanced fillets**
- **Printing**
- **???**

Embedded Package capacitance required



Thermal Issues

The 2002 ITRS says power increases gradually and die size remains constant at ~300 mm²: But that's not the whole story…



… because the power dissipating area (core) continues to shrink!
(and as # of transistors increases, so does total switching current required!)

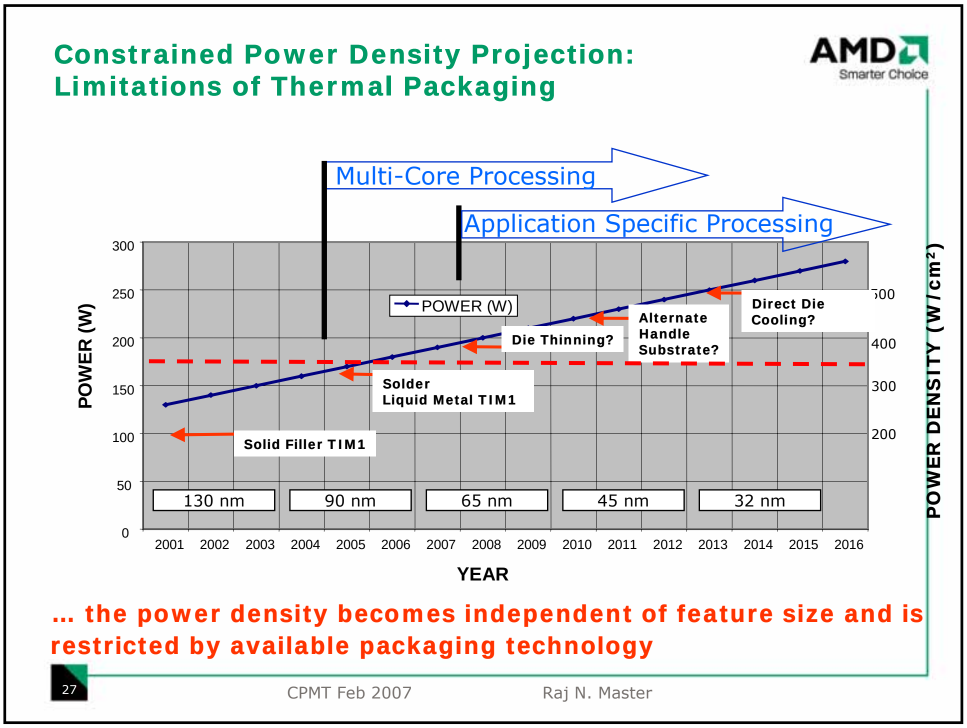
Thermal Interface Materials

- **Traditional Curable Grease / PCM with Solid Fillers**
  - Ease of Application
  - Understood Reliability
  - Low Cost
  - Thermal Resistance does not Meet Future Requirements
- **Solder**
  - Low Thermal Resistance
  - Best Thermal Resistance Uniformity
  - Concerns with Temperature and Power Cycling Reliability
  - Surface Preparation and Added Manufacturing Steps
- **Liquid Metal Hybrids**
  - Low Thermal Resistance
  - Needs Containment
  - Poor Understanding of Reliability
- **Materials Under Research**
  - Carbon Nanotubes
  - Graphite Derivatives

Thermal Issues: Solutions

Power density cannot continue to increase at this rate, but in the near-term we need to address up to 500 W/cm^2 (Hotspot cooling)!

- Very thin die to reduce thermal resistance through the Si
- New thermal interface materials (TIMs)
  - High thermal conductivity metallic fillers
  - Phase change filler materials with high heat of transformation
  - Low contact resistance (wetting on difficult surfaces)
  - High elasticity to account for mechanical stress
- Refined surfaces at thermal interfaces
  - Polished to reduce asperities and contact resistance
  - Reactive to improve wettability of TIMs
- New heat spreader materials
  - Maybe diamond finally has a chance
- New cooling technologies
  - Heat sinks and fans losing efficiency (increasing volume/watt removed)
  - Liquid cooling with miniaturized pumping systems
  - Need to bring cooling technology directly to the die



Constrained Power Density Projection: Limitations of Thermal Packaging

… the power density becomes independent of feature size and is restricted by available packaging technology

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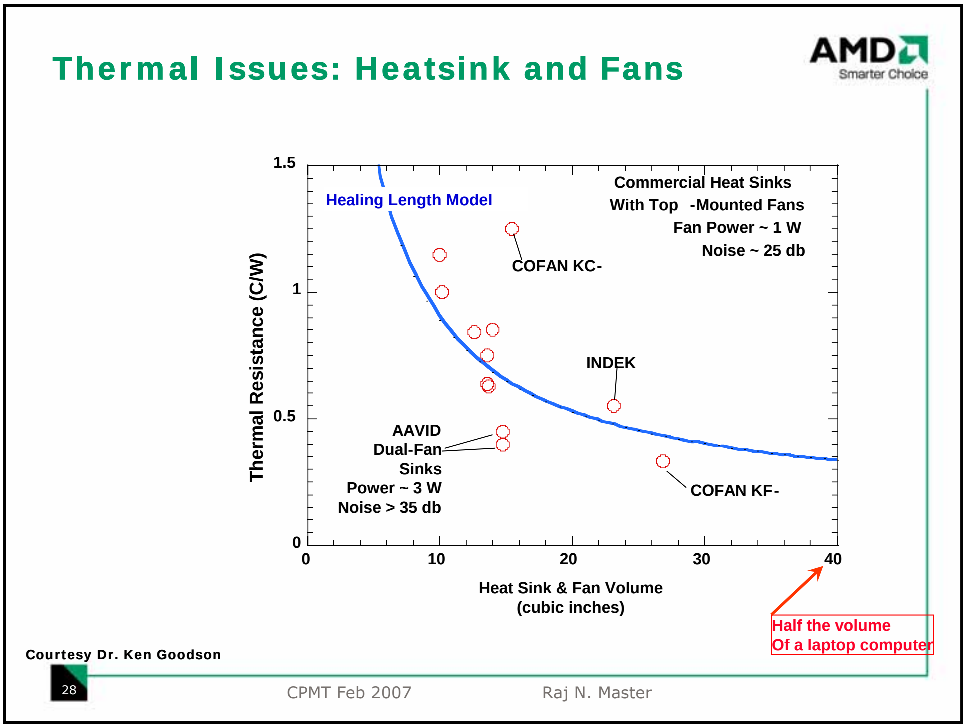

Thermal Issues: Heatsink and Fans

Courtesy Dr. Ken Goodson

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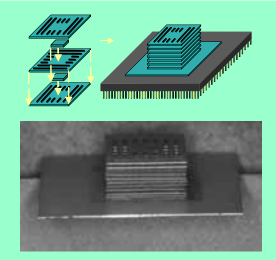
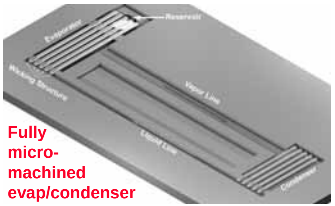
Thermal Issues: Direct die cooling (liquid)

AMD Smarter Choice

Micromachined Capillary Evaporator Designs

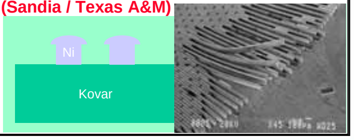


Multilayer micromachined evaporator increases capillary pressure (U. Maryland)



Fully micro-machined evap/condenser (UC Berkeley)

Single-layer optimized wicking structure (Sandia / Texas A&M)



Courtesy Dr. Ken Goodson

Low-K Overview

AMD Smarter Choice

Ceramic

Package

Alumina (Std)

- Better CTE match for full Low K
  - Reliability data supports
- Fine pitch problem
- Performance marginal

- Glass – Ceramic (LTCC) / Cu
  - Not ready for high volume
  - Cost= 1.5-2X current

Organic

Package Organic

- Current organic technology broken for full Low K
  - Die adhesion improvement Key
- Low CTE package required
  - No successful approaches
- Cost=1.5-2X current package

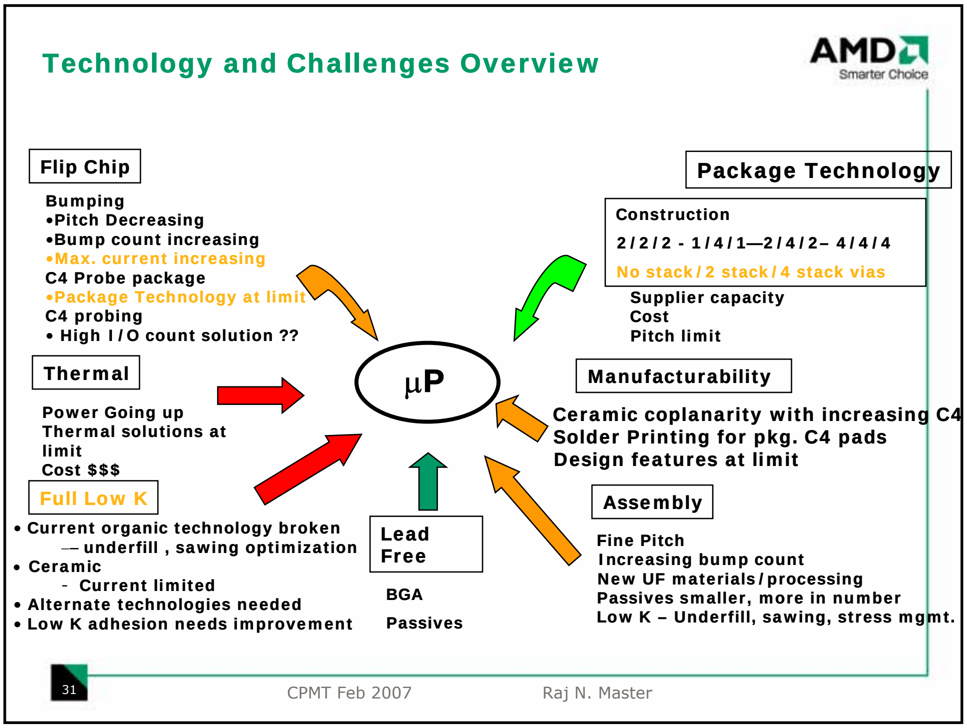
Low K

Assembly

- Current state-of-the-art 150μ
- Laser saw possible

Assembly

- Laser saw needed
- Full low K drives material and process solutions
  - stress management



Technology and Challenges Overview

AMD
Smarter Choice

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Thermal solutions at limit
Cost $$$

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  - — underfill , sawing optimization
- Ceramic
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- Alternate technologies needed
- Low K adhesion needs improvement

μP

Lead Free

BGA

Passives

Package Technology

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2/2/2 - 1/4/1—2/4/2– 4/4/4
No stack/2 stack/4 stack vias

Supplier capacity
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Manufacturability

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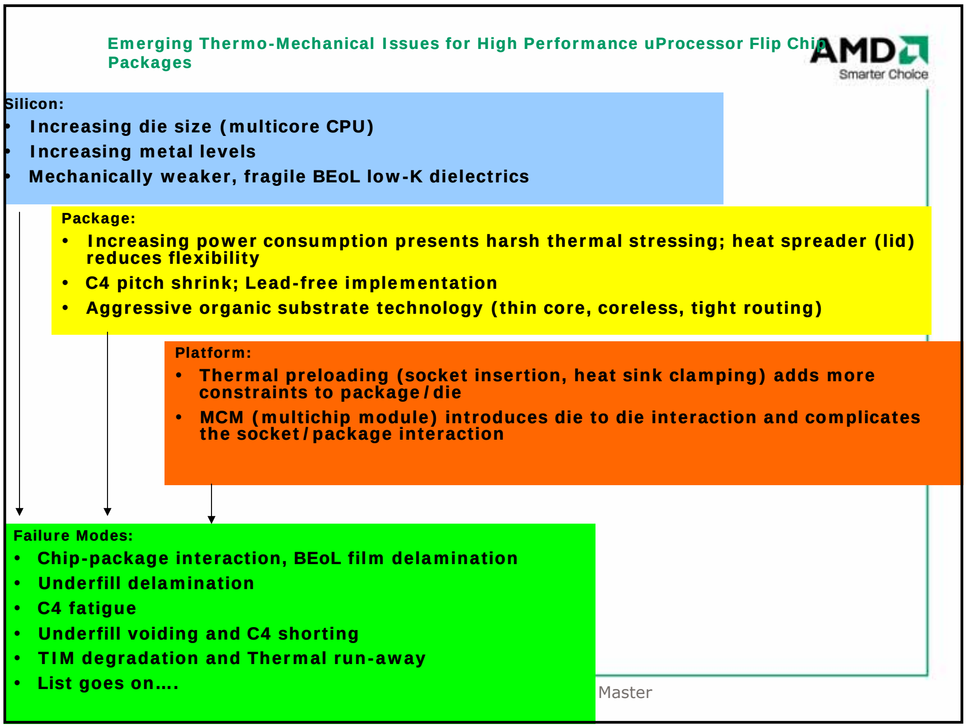


Emerging Thermo-Mechanical Issues for High Performance uProcessor Flip Chip Packages

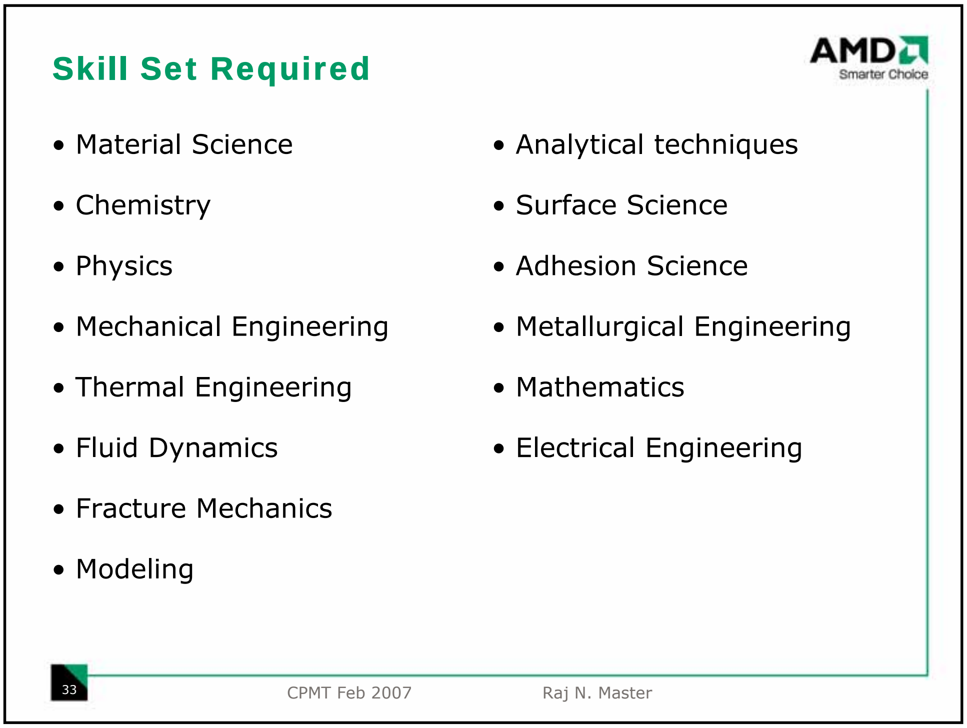
AMD
Smarter Choice

Silicon:
- Increasing die size (multicore CPU)
- Increasing metal levels
- Mechanically weaker, fragile BEoL low-K dielectrics

Package:
- Increasing power consumption presents harsh thermal stressing; heat spreader (lid) reduces flexibility
- C4 pitch shrink; Lead-free implementation
- Aggressive organic substrate technology (thin core, coreless, tight routing)

Platform:
- Thermal preloading (socket insertion, heat sink clamping) adds more constraints to package/die
- MCM (multichip module) introduces die to die interaction and complicates the socket/package interaction

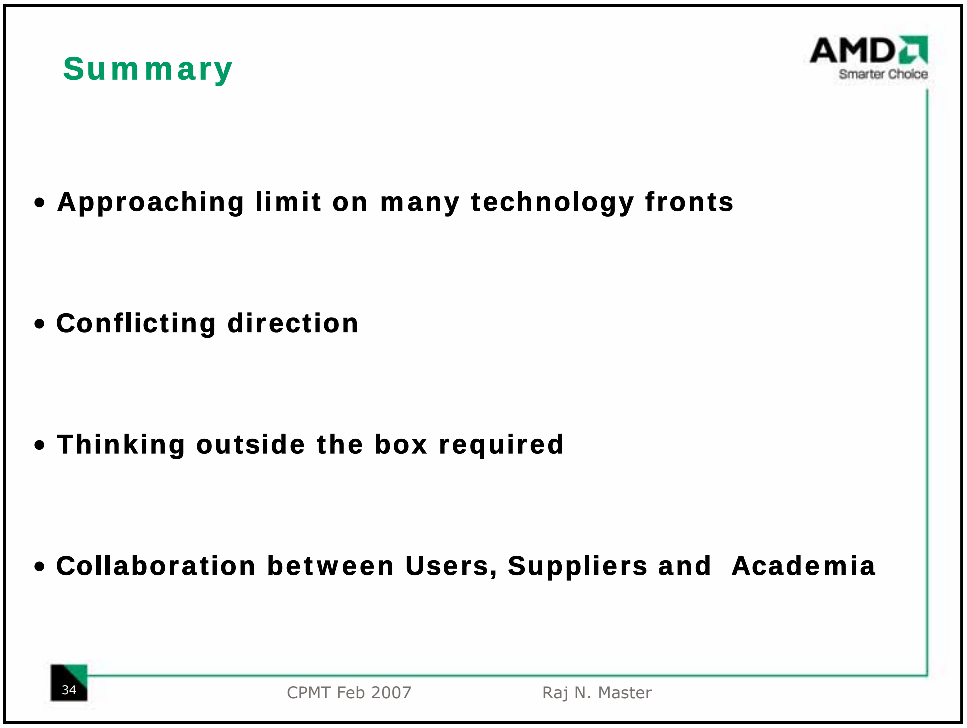
Failure Modes:
- Chip-package interaction, BEoL film delamination
- Underfill delamination
- C4 fatigue
- Underfill voiding and C4 shorting
- TIM degradation and Thermal run-away
- List goes on….



Skill Set Required

- Material Science
- Chemistry
- Physics
- Mechanical Engineering
- Thermal Engineering
- Fluid Dynamics
- Fracture Mechanics
- Modeling

- Analytical techniques
- Surface Science
- Adhesion Science
- Metallurgical Engineering
- Mathematics
- Electrical Engineering



Summary

- **Approaching limit on many technology fronts**
- **Conflicting direction**
- **Thinking outside the box required**
- **Collaboration between Users, Suppliers and Academia**