3D IC Development and Key Role of Supply Chain Collaboration

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Agenda

- Background and Motivation

- Stacked Silicon Interconnect Technology

- Supply Chain Collaboration
Background and Motivation
Background: FPGA

§ Building Blocks
- Configurable Logic Block (CLB)
  - Configuration memory
  - Programmable switches
  - Interconnect drivers
- Hard IP (DSP, EMAC, etc.)
- Block RAM
- Configurable IOs
- High-speed transceivers

Programmable SoC of logic, memory, and analog circuits
Customers Are Asking for More

• More than 2X today’s logic capacity…

• Many more high-speed serial transceivers…

• Many more processing elements…

• Much more internal memory to store data…
Challenge 1: Availability and Capability

Largest FPGAs only viable later in the life cycle
Challenge 2: Power and Bandwidth

Traditional mitigation techniques are no longer adequate

Chip-to-Chip via
Standard I/Os and SerDes

More total gates, sooner, but…

Resources Not Scaling
1. Not enough I/Os
2. I/O latencies too high
3. Wasted I/O power

Innovation Needed
Introducing Stacked Silicon Interconnect Technology
High Bandwidth, Low Latency, Low Power

Large Monolithic FPGA

Xilinx Innovation

✓ Massive number of low latency, die-to-die connections
✓ Earlier in time
✓ No wasted I/O power
✓ Over five years of R&D

Delivers the Best of Both Worlds: High and Usable Capacity
Delivers Resource-Rich FPGAs

Largest Device with Transceivers

- 2M logic density enabled one generation ahead!

Xilinx

Nearest Competitor

90nm  65nm  40nm  28nm

3.5x

1.9x
For the Most Demanding FPGA Applications

- Next Gen Wired Communications
- Next Gen Wireless Communications
- High Performance Computing
- Medical Imaging
- Aerospace & Defense
- Industry’s Highest System Performance and Capacity
Summary

- **SSIT Addresses IO Bottleneck**
  - 100X better BW/W over traditional IOs/SerDes

- **Can offer Next Generation Density Now**

- **SSIT Platform Enables**
  - Optimal Partitioning
    - Digital and analog blocks
    - IP/IC reuse
  - Heterogeneous Integration
    - Digital, mixed signal, & optical
    - FPGA & memory
Stacked Silicon Interconnect Technology

- Technology Overview
- Supply Chain Collaboration
- Summary
Xilinx FPGA Architectural Innovations
At the Heart of the Technology

ASMBL Optimized FPGA slice

FPGA Slices Side-by-Side

Silicon Interposer:
>10K routing connections between slices
~1ns latency
Harnesses Proven Technology in a Unique Way

**Microbumps**
- Access to power / ground / IOs
- Access to logic regions

**Through-silicon Vias (TSV)**
- Only bridge power / ground / IOs to C4 bumps
- Coarse pitch, low density aids manufacturability
- Etch process (not laser drilled)

**Passive Silicon Interposer (65nm Generation)**
- 4 conventional metal layers connect micro bumps & TSVs
- No transistors means low risk and no TSV induced performance degradation

**Side-by-Side Die Layout**
- Minimal heat flux issues
- Minimal design tool flow impact

**New!**
- 28nm FPGA Slice
- Passive Silicon Interposer
- Through-Silicon Vias
- C4 Bumps
- Microbumps
- BGA Balls
- Package Substrate
Virtex-7 SSIT uses 28 nm FPGA and 65 nm Interposer

- Low risk approach to integrate TSV & u-bump
  - Passive silicon interposer with 65nm interconnects & coarse-pitch TSV
- High density micro-bump for 10K-30K chip-to-chip connections
- Better FPGA low-k stress management with silicon interposer

28nm Test Vehicle + 65 nm Interposer

<table>
<thead>
<tr>
<th>Technology</th>
<th>Specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M4</td>
<td>2um pitch 4 4X layers</td>
</tr>
<tr>
<td>TSV</td>
<td>&gt;10 um diameter &amp; 210um pitch</td>
</tr>
<tr>
<td>Micro-bump</td>
<td>45um pitch</td>
</tr>
<tr>
<td>C4</td>
<td>210um pitch</td>
</tr>
<tr>
<td>Package</td>
<td>4-2-4 Layer, 1.0 mm BGA pitch</td>
</tr>
</tbody>
</table>

Courtesy of Xilinx, TSMC, Amkor
Correlation between Measurement and Simulation

Through transmission structure using two TSVs

**Insertion Loss S21 [dB]**

Dotted Red Trace – Measurement
Solid Blue Trace - Simulation

**Return Loss S11 [dB]**
Eyes After TSV Optimization

w/o Interposer

10Gbps

13Gbps
# Reliability Validation Status

<table>
<thead>
<tr>
<th>Reliability Tests</th>
<th>Focus Areas</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Level L4 Precon and TCB</td>
<td>TSV and C4</td>
<td>Passed 1000 TCB</td>
</tr>
<tr>
<td>Wafer Level TCB</td>
<td>TSV&amp; Interposer Interconnects</td>
<td>Passed 1000 TCB</td>
</tr>
<tr>
<td>Electro-migration</td>
<td>Micro-bump Joint</td>
<td>Passed 0.1% CDF for 10 years</td>
</tr>
<tr>
<td>High Temperature Storage</td>
<td>Micro-bump Joint</td>
<td>Passed 1000 hours</td>
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<tr>
<td>Package Level L4 Precon and TCB – 1st Leg</td>
<td>Micro-bump Joint, TSV, C4 Interconnects</td>
<td>Passed L4 and 500 TCB (CSAM)</td>
</tr>
<tr>
<td>Package Level L4 Precon and TCB – 2nd Leg</td>
<td>Micro-bump Joint, TSV, C4 Interconnects</td>
<td>In progress</td>
</tr>
<tr>
<td>Package Technology Qualification - L4 Precon, TCB, THB, HTOL, HTS</td>
<td>Micro-bump Joint, TSV, C4, Silicon, Package</td>
<td>In planning</td>
</tr>
</tbody>
</table>
Underfill

Initial Underfill

MRT L5/250

HAST 48 Hours

HAST 264 Hours

No Delamination, Post HAST: 110C, 85% RH, 264 Hours

Courtesy of Xilinx, TSMC, Amkor
Establishing a Supply Chain Flow

**Considerations**
- Product and Cost Requirements
- Scalable Business Model
- Design Rules (Foundry vs. OSAT)
- Heterogeneous Die integration
Benefits from Collaboration with Other Technology Leaders

- Leading fabless & fablite companies
- Equipment manufacturers
- Fabs and OSAT
- Industry consortia

- Requirements alignment
- Industry standards setting
- Best practice sharing
Xilinx has a Robust Supply Chain

Leading foundry and OSAT partners

FPGA, Interposer, & Package Design

28nm FPGA & Interposer

Package Substrate

μBump, Die separation CoC attach, & Assembly

Final Test of Packaged Part
TSMC Discusses Stacked Silicon Interconnect

Dr. Shang-Yi Chiang
Senior Vice President, R&D, TSMC
System Migration Trend

Traditional → Silicon Interposer → 3D

- Analog
- RF
- Passive
- Logic
- Memory
Xilinx Is Well on the Way to Volume Production

<table>
<thead>
<tr>
<th>Test Vehicle</th>
<th>CY09</th>
<th>CY10</th>
<th>CY11</th>
<th>CY12</th>
</tr>
</thead>
<tbody>
<tr>
<td>TV1 (90nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>TV2 (40nm)</td>
<td></td>
<td></td>
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<tr>
<td>TV3 (28nm)</td>
<td></td>
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</tr>
<tr>
<td>Device (28nm)</td>
<td>ISE 13.1 Beta</td>
<td>TO</td>
<td>ES</td>
<td>Prod</td>
</tr>
</tbody>
</table>

Today

Module Development
Process Integration
Reliability Assessment
Supply Chain Validation
Design Enablement
Design Validation
Process Qualification
EA Design Tools
Initial Sampling
Xilinx leads industry with **Stacked Silicon Interconnect** technology delivering breakthrough capacity, bandwidth and power efficiency

**Stacked Silicon Interconnect Technology**
- 2X FPGA capacity advantage at each process node
- Core part of Virtex-7 family
- Supported by standard design flows