A Comparison of Low Cost Interposer Technologies

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NVIDIA Products and Interposer Drivers

NVIDIA Products
- Application processor for mobile phones and tablet PCs (Tegra)
- Gaming GPU for laptop and desktop PCs (GeForce)
- High-end digital content creation for workstation (Tesla/Quadro/Volta)

Interposer Drivers
- Higher electrical performance
- Smaller form factor
Low Cost Interposer Approaches

Si Interposer

Organic Interposer

Glass Interposer

Source: Yole/Global Foundries 2012

Source: SEMCO

Source: Corning (2013 IMAPS)
Si Interposer Process Cost Analysis

- Via etching and filling (69%) processes are major cost factor
- TSV formation is the most expensive cost for interposer fabrication
- Thinner interposer reduces process cost

Cost Distribution of TSV Processes

- Via Etching: 24%
- Via Isolation: 25%
- Via filling: 4%
- Temporary bonding: 3%
- Thinning: 44%

Source: IME
Assembly Flows for Thinner Interposer

**Chip to Chip**
- **Process Thin I/P or Die**
  - Chip/Wafer Damage
- **Top Die Attach**
  - uBump Joining Defects
- **Underfill & Cure**
- **Finish Assembly**

**Chip to Sub**
- **Attach I/P & UF on Sub**
  - C4 Bump Joining Defects
- **Top Die Attach**
  - uBump Joining Defects
- **Underfill & Cure**
- **Finish Assembly**

**Chip to Wafer**
- **I/P Wafer with full thickness**
- **Top Die Attach**
- **Mold & Top Die Exposure**
- **C4 Bump & Singulation**
Thin Si Interposer Summary

Advantages
- Reduce interposer process cost
- No warpage concern during top die attach (C2W)
- Tighter design rule
- Better electrical performance

Challenges
- uBump joint reliability
- Higher interposer thickness variation
- New investment for C2W process equipment (OSATs)
Organic Interposer

- Use low CTE and high modulus organic materials
- Mechanically symmetric structure
- Offer finer design rule than conventional substrate
- Apply Si fab equipment for manufacturing

(Source: SEMCO (2012 MEPTEC))
Si vs. Organic Interposer

<table>
<thead>
<tr>
<th>Si Interposer</th>
<th>Organic Interposer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Wafer</strong></td>
<td>Core Substrate Type</td>
</tr>
<tr>
<td>Silicon (3ppm/K) 100µm</td>
<td>Core Material (CTE) Core Thickness</td>
</tr>
<tr>
<td>1µm</td>
<td>Line Width</td>
</tr>
<tr>
<td>Asymmetry (n+1)</td>
<td>Structure (Top+Bottom)</td>
</tr>
<tr>
<td>Dry Etch</td>
<td>Core Through Hole</td>
</tr>
<tr>
<td>PECVD + PVD+Cu Plating (Semiconductor Process)</td>
<td>Through Hole Filling</td>
</tr>
<tr>
<td>Wafer Thinning</td>
<td>Total Thickness Control</td>
</tr>
<tr>
<td>801ea/m² (12 inch)</td>
<td>Net Die (25 x 25mm²)</td>
</tr>
</tbody>
</table>

Source: SEMCO (2012 MEPTEC)
Organic Interposer Assembly Flow

**Chip to Strip**
- Top D/A & Mold on IP Strip
- Plate C4 Bumps & IP on PKG Sub

**I/P to PKG Substrate**
- I/P on PKG Sub → UF
- Die Attach & UF

- Similar to C2W process flow
- Die attach and mold process
- Thermal compression bonding for D/A

- C2S process flow
- Die attach and mold process
- Mass reflow for D/A
Organic Interposer Summary

Advantages
- Use low cost process and materials
- Process rectangular panel format
- Utilize existing supply chain
- Extended to interposer embedded substrate
- Potentially lower cost

Challenges
- Looser design rule than Si interposer
- Innovation needed to create robust tight L/S
- Manufacturing and reliability challenges
- Limited suppliers
Glass Interposer

- Formed by fusion process
- Applicable for roll to roll process with Cu via filling process
- Material properties can be tailored (CTE: 3~9 ppm/C)
- Via formation processes: Laser or Wet etch
- Similar assembly process steps to Si interposer
Glass Interposer Assembly Process

**Chip to Singulated I/P**
- Completed I/P → Top D/A & UF
- Attach I/P on PKG Sub

**Similar to C2C process flow**
- Attach top die on singulated I/P
- Require T/C bonding for thin I/P

**Chip to Wafer**
- Via & RDL → Top D/A & UF on I/P Wafer
- Wafer Thinning & C4 → Attach to PKG Sub

**Similar to C2W process flow**
- Mass reflow for die attach
- Challenge for **glass wafer thinning**
Glass Interposer Summary

Advantages
- Use low cost material
- Process rectangular panel format
- Potentially applicable for roll to roll process
- Material properties can be tailored

Challenges
- Supply chain
- Looser design rule than Si interposer
- Cost effective via formation
- Warpage control for large panel
# Low Cost Interposer Comparison

<table>
<thead>
<tr>
<th></th>
<th>Thin Si Interposer</th>
<th>Organic Interposer</th>
<th>Glass Interposer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process Format</strong></td>
<td>Wafer</td>
<td>Panel</td>
<td>Panel</td>
</tr>
<tr>
<td><strong>Design Rule</strong></td>
<td>Very Tight</td>
<td>Loose</td>
<td>L/S: Under development</td>
</tr>
<tr>
<td>(L/S &amp; Via Diameter)</td>
<td></td>
<td></td>
<td>Via: Loose</td>
</tr>
<tr>
<td><strong>Assembly Process</strong></td>
<td>C2W</td>
<td>C2SI</td>
<td>C2GI</td>
</tr>
<tr>
<td><strong>Supply Chain</strong></td>
<td>Si Fab or</td>
<td>Substrate → OSAT</td>
<td>Not defined yet</td>
</tr>
<tr>
<td></td>
<td>Si Fab → OSAT</td>
<td></td>
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</tr>
</tbody>
</table>
Summary

- Current interposer cost is too high
- The cost should be reduced to enable for high volume production
- We need innovation from the industry (Foundries, OSATs, Material/Equipment Suppliers) to implement 2.5D for HVP