Survey and Review of 2.5/3D IC Packaging Technologies
Part 1 - Overview

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AGENDA

Part 1
Introduction
Why Complement “2D Silicon Designs” with … … 2.5D and/or 3D-IC Packaging Technology
Designs Completed // in Progress and Future
Business Considerations
Summary and Q & A

Part 2
Deep Dive into Topics of Interest
Herb Reiter’s Background

**BUSINESS DEVELOPMENT:**
- 12+ years
  - IC Design Tools
  - Semiconductor IP
  - SOI Technology
  - FinFET Metrology
  - PoP & SIP Packaging
  - Since 2008: 2.5/3D-ICs

**PRODUCT MARKETING:**
- ASIC 18 years
- VLSI Technology 1989 - 1997
- ALLIANCE MGMT and MARKETING: CMOS ASICs and ASSPs

**EDA2ASIC Consulting Since 2002**

“House-Keeping”

Keep the meeting interactive & relevant for YOU

Flip Chart to capture “Q’s” – and discuss “A’s” later

Soft-copies of the slides will be made available

Web-pointers on slides lead to further details

Appendix: 3D books, conferences, R&D partners

Part 2 will be a deep dive into topics of interest
Two New Packaging Alternatives

Side-by-side dice on an Interposer, also called “2.5D-IC”
Vertically stacked dice, called “3D-IC”

Source: YOLE  [http://www.i-micronews.com/lectureArticle.asp?id=8836]

Why Complement “2D Silicon Designs”...
... with 2.5D and/or 3D-IC Packaging Technology

[Images of 2D, 2.5D, and 3D designs]
Heterogeneous Integration

Many systems need non-digital functions to interact with the real world.

For Information Processing, 2.5D & 3D ICs combine both Digital only 2D SoCs.

Derived from: ITRS Roadmap

Silicon Cost per 100 Million Gates (1)

Cost per Gate Trend with Reduction in Feature Dimensions

Source: International Business Strategies, Inc.

http://www.eetimes.com/author.asp?section_id=36&doc_id=1321674&image_number=1
**Wafer Cost Increases Rapidly**

- The wafer price increase washes away the scaling benefit → little saving in XTor cost... need to lower CoC, simplify process, better yield... etc., to incentivize Fab customers to 20 and 14nm.

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**Shrinking Reaches Complexity Limit**

- "2D ICs" are hitting economic COMPLEXITY LIMIT !!!
- Partitioning into smaller dice increases # of gross dice per wafer and yield ➔ Both reduce total unit cost

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http://semiconductorexpert.blogspot.com/2012/03/nvidia-tsmc-20nm-essentially-worthless.html

http://www.newelectronics.co.uk/electronics-technology/the-economics-of-chip-manufacture-at-advanced-technologies/35562/
Chip Design Cost Trend


- Design cost ($M)
- Mask cost ($M)
- Embedded software ($M)
- Yield ramp-up cost ($M)

28nm = 2x 45nm cost

> $170 M

On-Chip Interconnect Delay Trend

Interconnect RC

BEOL RC dominant

~1000x

Transistor delay

Power Loss in Input/Output Buffers

Source: Page 38 of ChipScale Review Sept/Oct 2013, by Dr. Dev Gupta (see pointer above)

...2.5D and 3D-IC Technology
Packaging Evolution

-1980s

Mostek MK 38P70

2,500 μm pin spacing

1980s

2.5D IC

Die are face-down and side-by-side on interposer

Virtex 7000 Family

-1990s

PoP

-2000s

SIP

Vertically Stacked Die: 3D

Die interconnected with TSVs in Assembly

Hybrid Memory Cube / Wide I/O Stack

-2010s

Vertically Stacked Die: 3D

Die interconnected with TSVs in Assembly

Hybrid Memory Cube / Wide I/O Stack

2,500 μm pin spacing

2010s

Vertically Stacked Die: 3D

Die interconnected with TSVs in Assembly

Hybrid Memory Cube / Wide I/O Stack

- 25 μm spacing

Multi-Physics Design Challenge

<table>
<thead>
<tr>
<th>Materials</th>
<th>CTE (ppm/°C)</th>
<th>Young’s Modulus (GPa)</th>
<th>Poisson’s Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>2.8</td>
<td>131</td>
<td>0.28</td>
</tr>
<tr>
<td>Copper</td>
<td>17.0</td>
<td>117</td>
<td>0.35</td>
</tr>
</tbody>
</table>

Source: A. Wilde, P. Schneider, P. Ramm, DTC 2010


Electrical

Thermal

Mechanical

Electro-thermal interactions

Electromigration

Performance and Reliability

Thermo-mechanical stress
**End-Use Markets for 2.5/3D**

![Chart showing market shares of different end-use markets for 2.5/3D technology, with cellphones and servers having the highest market share.](http://www.icinsights.com/news/bulletins/Cellphones-Pass-PCs-As-Biggest-Systems-Market-And-IC-User/)

**Benefits of Higher Value Packaging**

<table>
<thead>
<tr>
<th>Market</th>
<th>Low Power Dissipation</th>
<th>High Bandwidth CPU &lt;-&gt; DRAM</th>
<th>Low Latency IC &lt;-&gt; IC</th>
<th>Heterogeneous Integration</th>
<th>Form-factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cellphones and esp. Smartphones</td>
<td>★★★ ★★★</td>
<td>★★★</td>
<td>★</td>
<td>★★★</td>
<td>★★★</td>
</tr>
<tr>
<td>Compute Servers, Network Routers</td>
<td>★★★ ★★★</td>
<td>★★★</td>
<td>★★★★★★★</td>
<td>★★★</td>
<td>★★★</td>
</tr>
<tr>
<td>Tablets and other Mobile Devices</td>
<td>★★★ ★★★</td>
<td>★★★</td>
<td>★★★★★★★</td>
<td>★★★</td>
<td>★★★</td>
</tr>
<tr>
<td>Standard PCs and Workstations</td>
<td>★★★ ★★★</td>
<td>★★★</td>
<td>★★★★★★★</td>
<td>★★★</td>
<td>★★★</td>
</tr>
<tr>
<td>Automotive Applications</td>
<td>★★★ ★★★</td>
<td>★★★</td>
<td>★★★★★★★</td>
<td>★★★</td>
<td>★★★</td>
</tr>
</tbody>
</table>

Additional decision factors: Unit Cost, System Cost Savings, NRE, Time-to-profit, Risk,...

4/21/2014 — Extremely Valuable, Very Valuable, Valuable
### Comparison of 2.5D and 3D-ICs

<table>
<thead>
<tr>
<th>Criteria</th>
<th>2.5D</th>
<th>3D</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit Cost</td>
<td>Lower</td>
<td></td>
<td>Interposer adds to 2.5D cost</td>
</tr>
<tr>
<td>Development cost &amp; time</td>
<td>Lower</td>
<td></td>
<td>Fewer placement considerations</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>Higher</td>
<td></td>
<td>Many short, vertical connections</td>
</tr>
<tr>
<td>Latency</td>
<td>Lower</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Lower</td>
<td></td>
<td>Shorter connections → Lower RC loads</td>
</tr>
<tr>
<td>Form-Factor</td>
<td>Smaller</td>
<td></td>
<td>3D needs less board-space</td>
</tr>
<tr>
<td>Cooling Challenges</td>
<td>Fewer</td>
<td></td>
<td>Every die directly accessible</td>
</tr>
<tr>
<td>Design Flexibility</td>
<td>Greater</td>
<td></td>
<td>Interposer gives additional freedom</td>
</tr>
<tr>
<td>Testability</td>
<td>Easier</td>
<td></td>
<td>Every die easier accessible</td>
</tr>
<tr>
<td>Current Proto Capabilities</td>
<td>Better</td>
<td>*</td>
<td>∴ 3D memories are ready NOW</td>
</tr>
<tr>
<td>Current Production Capacity</td>
<td>Check</td>
<td>Check</td>
<td>Production supply chain emerging</td>
</tr>
<tr>
<td>Overall Risk, currently</td>
<td>Lower</td>
<td></td>
<td>2.5D needs fewer new capabilities</td>
</tr>
<tr>
<td>Need for standards</td>
<td>Lower</td>
<td></td>
<td>Vertical stacking: More coordination</td>
</tr>
</tbody>
</table>

* *: 3D memories are ready NOW

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### Best of Both Worlds

* SOURCE: YOLE Developpment, France

Geometries range from 10 to 800 um ....!
Basic 2.5D/3D Design Flow

Inputs
- Availability, technical- and cost estimates
- Constraints: Material, Wafer-fab, Assembly, Test

System Specification
- Plan System Architecture
- Path-Finding, Partitioning into ICs
- Floor Planning of Individual ICs
- Logical- & Physical Implementations
- Logical- & Physical Verifications
- Packages & PCB Development

Key Design Challenges
- Complexity
- Power Density / Heat
- PI and SI
- Noise, Coupling
- Testability
- Multi-physics effects

Release to Manufacturing

IC Design Steps
System Design Steps

Examples for Industry Status

A = 2.5D/3D Design Completed
B = 2.5D-IC Opportunity
C = Monolithic Integration
A: Xilinx Saves Significant Power

- Virtex 2000T – 2 million logic cells
- 4-layer metal Si interposer with TSV
- 4 FPGA sub die in package
- >10,000 inter-die connections
- In production since 2011

Power of these 4 FPGAs: 18 Watts
Versus 120 Watts if individually packaged

Modularity
- Much better yields versus one large die
- Speed- and power binning possible

Courtesy: Xilinx

A: Xilinx Integrates Digital and Analog in a 2.5D-IC

Virtex-7 H580T Heterogeneous FPGA announced May 30, 2012
Two FPGA slices and up to sixteen 28 Gbps and seventy-two 13.1 Gbps transceivers
Single-package solutions for addressing key Nx100G and 400G line card applications

**A: Xilinx Integrates an Entire System**

March 2014:


Source: Bill Swift Presentation at DesignCon, January 2013

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**A: Cisco Integrates Logic and Photonics**

Saves significant PCB space and cost with 2.5D-IC


Source: Bill Swift Presentation at DesignCon, January 2013
A: STEricsson Increases Bandwidth and saves significant power with 3D-IC

JEDEC (JC 42.6) released Q4, 2011 the Wide I/O 1 Standard. It offered TWICE the Bandwidth at the same Power Dissipation as LPDDR2.

Drivers of the Wide I/O 1 standard: Samsung, Elpida, Hynix, Micron, Qualcomm, TI, Intel, AMD, ST, Apple, Advantest,... BUT it was too costly for use in smartphones

Wide I/O 2 discussed in 2012/13, 3rd, lower cost version considered at JEDEC now.

A: Samsung Increases Performance and saves significant power with 3D-IC

• World’s 1st AP using Widcon & TSV

Samsung calls Wide I/O “Widcon”
B: 2.5D Opportunity

Lots of passives surround the PMU and consume board-space

Smart multi-sensor module with 9 degrees of freedom
The INEMO-M1 is the first 9-axis motion sensing system-on-board (SoB) of the iNEMO module family. Offered by STMicroelectronics.
Stacking of functions is performed in a wafer fab.

Monolithic Integration needs to be performed in a wafer fab.
Achieves significantly smaller geometries versus dice stacking in assembly.
Currently only in development and use for Memories.
C: Inductive and Capacitive Coupling

For inductive coupling also see: http://www.thruchip.com/index.htm

Source:
Vol 05, Article 02223; February 2014
http://iives.com

System Integration with 2.5D & 3D-ICs

Source: Rao Tummala, Georgia Institute of Technology, 3D Systems Packaging Research Center, Oct 2010
Business Considerations

2D SoC, 2.5D or 3D-IC

Decision Criteria & Risks

Business

Technical

System Cost Savings / ROI
NRE
Unit Cost

Power Dissipation
Battery Life

Size + Weight
Form factor

Integration of
Logic + Memory + Analog + MEMS, ...

Supply Chain


Market Value
Time to Profit
Internal Resources

4/21/2014
Crossing the Chasm

The Big Scary Chasm

Peak of inflated expectations

Plateau of productivity

Smaller Chasm

Trough of disillusionment

Source:
Jeffery Moore, 1991
http://www.amazon.com/Crossing-Chasm-Marketing-Disruptive/dp/0060517123

Top 10 3D-IC Patent Holders

Source: YOLE, May 2013
SUMMARY

- Major challenges IF we only follow Moore’s Law
  - Complexity limit, Latency, Bandwidth, Flexibility, Cost, Risk,...

- 2.5D/3D-ICs are gaining significant momentum
  - 450 and EUV are delayed...: <20nm ➔ high NRE, high wafer cost
  + Power Density, Testability, Supply Chain, Cost,... being addressed

- 2D Chips are the Building Blocks for 2.5D/3D-ICs
  + Die-level IP-reuse will help reducing NREs and time-to-profit

Thank You !!!

Q & A