Overview

- Two Main Issues in Assembly
- Something About Voids
- Industrial Standards
- Factor Analysis for Void Formation
  * Surface Finish
  * Voids from PCB Design
  * Voids from Component
  * Voids from Solder Paste
  * Voids from Process
- Voids in Bumping Process
- Conclusion
Two Main Issues in Assembly

1. HoP (Head-on-Pillow) and NWO (Non-Wetting Open)

2. Voids in solder joints (not only BGA)

Something about Voids

<table>
<thead>
<tr>
<th>Types of Voids</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Macrovoids</td>
<td>Voids were formed as volatile ingredients of the fluxes within the solder paste, usually found everywhere in solder joint.</td>
</tr>
<tr>
<td>Planar Microvoids</td>
<td>Voids generated by anomalies in surface finish application process, generally located in one plane and found at the solder-to-land interface.</td>
</tr>
<tr>
<td>Shrinkage Voids</td>
<td>Caused by the solidification of SAC solders, formed as linear cracks with rough edges from the surface of the solder joints.</td>
</tr>
<tr>
<td>Micro-via Voids</td>
<td>Caused by microvias in lands.</td>
</tr>
<tr>
<td>Pinhole Voids</td>
<td>Voids generated by excursions in the copper plating process at board supplier.</td>
</tr>
</tbody>
</table>
Something about Voids

Kirkendall Voids

During thermal aging (including temp. cycling), rapid diffusion of one material into another could cause crystal vacancies to form in the bulk material, that then leads to risks for reliability failures of solder joints.

- Kirkendall voids were formed in the Cu$_2$Sn because the Sn and Cu atoms diffused.
- During high temperature storage, two IMCs Cu$_6$Sn$_5$ and Cu$_3$Sn continued to grow and a certain amount of solder matrix was the different composition between the voids and neighbor IMCs.


Why don’t we like void?

- Poor Heat Transfer Rate
- Poor Current Carrying Capability
- Long-term Reliability Concern
- Squeezed Short
- Bump Height Uniformity
Inspection methods of Voids

Modern 2D/3D X-Ray inspection systems are powerful tools for finding defects in BGA, QFN and 3D packages.

<table>
<thead>
<tr>
<th></th>
<th>2D/3D X-ray</th>
<th>CT Scan</th>
<th>Cross Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>Best</td>
<td>Moderate</td>
<td>Worst</td>
</tr>
<tr>
<td>Preparation time</td>
<td>Best</td>
<td>Best</td>
<td>Worst</td>
</tr>
<tr>
<td>Analysis time</td>
<td>Best</td>
<td>Best</td>
<td>Worst</td>
</tr>
<tr>
<td>Automation</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Worst</td>
</tr>
<tr>
<td>Void Location</td>
<td>Moderate</td>
<td>Best</td>
<td>Best</td>
</tr>
<tr>
<td>Accuracy</td>
<td>Best</td>
<td>Moderate</td>
<td>Worst</td>
</tr>
<tr>
<td>Cost</td>
<td>Worst</td>
<td>Best</td>
<td>Moderate</td>
</tr>
</tbody>
</table>

Voiding Inspection Systems in SHENMAO Lab

SMT System
- Printer
- Reflow oven
- X-ray inspection

Wafer Bumping System
- Wafer printer
- Reflow oven

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### Industrial Standards for Voids

<table>
<thead>
<tr>
<th>Component</th>
<th>Criteria</th>
<th>Standard</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder Balls of BGA components (Pre-SMT)</td>
<td>&lt; 15%</td>
<td>JESD 217</td>
</tr>
<tr>
<td>Surface Mount Area Array (Post-SMT)</td>
<td>&lt; 25%</td>
<td>IPC-A-610</td>
</tr>
<tr>
<td>QFN, MOSFET, Components with Bottom Thermal Plane Terminations (Post-SMT)</td>
<td>No industrial standard but often target at &lt; 25%</td>
<td>-</td>
</tr>
</tbody>
</table>

### Occurrence Rate of Voids

![Occurrence Rate of Voids Chart](chart.png)
**Factor Analysis of Void Formation**

![Diagram showing factor analysis of void formation](image)

**Surface Finish**

**Test Conditions**

- **Surface treatment:**
  - OSP / ENIG / ImAg / ImSn
- **Printer:** Panasonic SP18P-L
- **Stencil thickness:** 0.12 mm
- **# of reflow zones:** 12
- **Atmosphere:** air
- **Heating profile:** RSS
- **Observation Apparatus:** MSX2000 X-ray detector
### Surface Finish

**Comparison of Different Surface Finish**

#### QFP

<table>
<thead>
<tr>
<th>Surface Finish</th>
<th>OSP</th>
<th>ENIG</th>
</tr>
</thead>
<tbody>
<tr>
<td>ImSn</td>
<td>2.92%</td>
<td>0.83%</td>
</tr>
<tr>
<td>ImAg</td>
<td>2.72%</td>
<td>1.20%</td>
</tr>
</tbody>
</table>

#### 0603 Chip

<table>
<thead>
<tr>
<th>Surface Finish</th>
<th>OSP</th>
<th>ENIG</th>
</tr>
</thead>
<tbody>
<tr>
<td>ImSn</td>
<td>5.58%</td>
<td>1.54%</td>
</tr>
<tr>
<td>ImAg</td>
<td>5.16%</td>
<td>3.37%</td>
</tr>
</tbody>
</table>
**Surface Finish**

**Comparison of Different Surface Finish**

<table>
<thead>
<tr>
<th>Surface Finish</th>
<th>OSP</th>
<th>ENIG</th>
</tr>
</thead>
<tbody>
<tr>
<td>BGA 0.5 mm</td>
<td>6.38%</td>
<td>0.83%</td>
</tr>
<tr>
<td>ImSn</td>
<td>5.44%</td>
<td></td>
</tr>
<tr>
<td>ImAg</td>
<td>4.17%</td>
<td></td>
</tr>
</tbody>
</table>

**Mechanism of Voids from ImAg**

- Large amount of caves between ImAg surface and Cu pad
- Poor boundary
- De-wetting point
- Driving force of solder
- Organic outgasing from flux
- Outgasing from H2O, O2 or chemicals residue

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Key Factors of Voids from ImSn

- Discoloration
- Low tin thickness
- Ionic / organic contamination

*Oxidation on ImSn surface
*Transform to IMC layer → Dewetting
*De-wetting

Cracks from Planar Voids

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Voids from PCB Design

Via Hole

- Poor filling from stencil printing
- Risk of residue from electroplating

Typical Microvia Void

Voids from Component

Contaminations

Traces of flying pin test

A very large void in center of the BGA ball

“Balloon effect” to form large void
Two voiding types can be found in MOS, LGA, or any component with larger soldering area.

1. Gas
   - The outer area of the paste will melt first and then block the inner gas to escape.

2. Non-wetting
   - The minimal soldering with the component is caused by non-wetting.

Combination of 2 effects:
**Voids from Component**

**Stencil Design**

Take QFN for example

- **Ground Pad:**
  - Four-grid
  - Nine-grid
  - Minus 20% Area

<table>
<thead>
<tr>
<th>Large void size</th>
<th>Small void size</th>
<th>Minimized void size</th>
</tr>
</thead>
</table>

**Good:** "Window paning" creates vents that results in smaller voids.

**Bad:** Vent channels resulted in additional "open" areas that reduced solder joint continuity. However, it can't eliminate voids completely due to the surface finish wetting issues.

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**Voids from Solder Paste**

Solder paste plays an important role in contribution of void.

- High volume of flux → High volume of gas generated
- Large surface area from solder powder → Rapid chemical reaction in reflow

Water soluble solder pastes tend to cause larger void than no-clean ones.

- Different chemical compound in flux
- Moisture absorption

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Reflow Simulator

- Customized Reflow Profile
- Customized Atmosphere (Air/N₂)
- Monitors what is happening during reflow.
- Displays two images at the same time by connecting two sets of CCD cameras.
- Measures the warp caused by thermal stress

BGA-1

BGA-2

Camera 1 (top view)

Camera 2 (side view)

Reflow chamber

Bumping

Voids from Solder Paste

Mechanism of Void Formation in Reflow

Flux cleans oxide (gas 1) and activator (gas 2) and solvent (gas 3) to generate void.

Gas may be trapped because of the surface tension of flux and solder.

MO + RC(OH)₂ → (RCOO)M + H₂O\(_(g)\)

Flux cleans oxide (gas 1)

RC(OH)₂ + R'OH → R'C(OR)₂ + H₂O\(_(g)\)

Activator (gas 2)
Voids from Solder Paste

**Powder Size Effect**

- **Type 5 (15-25μm)**
  - Smaller Surface Area
  - Less Flux Reaction
  - Less Gas Generation
  - Ave. 0.19%
  - Max. 1.20%

- **Type 7 (2-12μm)**
  - Larger Surface Area
  - More Flux Reaction
  - More Gas Generation
  - Ave. 9.64%
  - Max. 13.20%

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Voids from Solder Paste

**Powder Oxidation Effect**

<table>
<thead>
<tr>
<th>Sample</th>
<th>Oxygen content</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>334 ppm</td>
</tr>
<tr>
<td>B</td>
<td>507 ppm</td>
</tr>
</tbody>
</table>

\[
\text{SnO}_2 + RCOOH \rightarrow (RCOO)_y Sn + H_2O(g)
\]

According to the reaction, the more oxidation on the surface, the more H$_2$O gas formation, resulting in higher voiding.

- Ave. 0.92%
- Max. 2.70%
- Ave. 1.86%
- Max. 4.90%

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**Voids from Process**

**Profile Consideration**

<table>
<thead>
<tr>
<th>Profile</th>
<th>Void in BGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTS</td>
<td>6.03%</td>
</tr>
<tr>
<td>RSS</td>
<td>2.52%</td>
</tr>
</tbody>
</table>

*Void Growth*  
RSS < RTS

*Flux outgases on heating.

*Long soaking helps to reduce voids  
→ by Increasing outgassing before solder melts.

RSS profile is more suitable for larger components because a longer soaking time can achieve thermal uniformity. It also provides longer time for gas to escape.

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**Atmosphere**

*Void Growth*  
N$_2$ < Air

N$_2$ prevents powder from oxidation.

→ Reduces gas formation from flux reaction during reflow

In N$_2$ atmosphere, flux becomes more fluid (lower surface tension) so that the gas can escape easily.
**Voids from Process**

**Vacuum Reflow**
- Gas evacuates from molten solder easily
- Cycle time is 30-60 sec or longer (in-line reflow oven)
- Costs much more than conventional reflow oven
- Minor risk of splash of flux and solder ball
- Minor risk of small sized component shift

**Fluxless Reflow (in Formic Acid Atmosphere)**
- No Flux = No Gas Generation
- Cycle time
- Limited cleaning and reduction ability
- Solder balls need to be fixed in (ball attach / bumping / pre-solder) process

**Voids in Bumping Process**

**Bumping Process**
- Opening definition
- Paste deposition
- 1st reflow & Dry film removal
- Flux dispensing
- 2nd reflow
- Flux clean solvent
- Flux spray

**Flip Chip**
- Flip Chip Tacky Flux
- Substrate Bumping
- Wafer Bumping

**Substrate**
- BGA Flux
- SMT Solder Paste

**PCB**

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Voids in Bumping Process

Voids are big challenges for bumping process

Problem from Production Process
- Reflow condition

Bad printing condition
- Excess (high) melting temperature and melting time

Excess (high) speed heating in secondary heating zone
- Thick printing

Problem from Wafer/Substrate
- Shape design of dry film
- Poor wetting and oxidation on pad
- Plating liquid residue

Moisture

Voids in Bumping Process

Solder Paste Design

<table>
<thead>
<tr>
<th>Flux</th>
<th>Conventional</th>
<th>New Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rosin</td>
<td>20–50%</td>
<td>R1</td>
</tr>
<tr>
<td>Activator</td>
<td>0–10%</td>
<td>A1+A2</td>
</tr>
<tr>
<td>Halide</td>
<td>0–5%</td>
<td>H1</td>
</tr>
<tr>
<td>Thixotropic</td>
<td>0–10%</td>
<td>T1</td>
</tr>
<tr>
<td>Solvent</td>
<td>10–25%</td>
<td>S1+S2</td>
</tr>
</tbody>
</table>

In-house testing results (piece wafer)

<table>
<thead>
<tr>
<th></th>
<th>Ave.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>3.04%</td>
<td>7.40%</td>
</tr>
<tr>
<td>New Formula</td>
<td>1.03%</td>
<td>3.90%</td>
</tr>
</tbody>
</table>

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**Voids in Bumping Process**

**Solder Paste Design**

<table>
<thead>
<tr>
<th>Wafer Type</th>
<th>Dummy</th>
<th>Dummy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Paste</td>
<td>Conventional</td>
<td>New Formula</td>
</tr>
<tr>
<td>Dry Film Opening (μm)</td>
<td>150</td>
<td>150</td>
</tr>
</tbody>
</table>

**In-Line Testing Results (Full Wafer)**

<table>
<thead>
<tr>
<th>FV bump void (%)</th>
<th>Sample Size</th>
<th>7500</th>
<th>7500</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt; 30</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>26-30</td>
<td>8</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>21-25</td>
<td>31</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>16-20</td>
<td>56</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>11-15</td>
<td>113</td>
<td>9</td>
<td></td>
</tr>
<tr>
<td>Amount Void</td>
<td>209</td>
<td>39</td>
<td></td>
</tr>
<tr>
<td>Void Rate (%)</td>
<td>2.78</td>
<td>0.52</td>
<td></td>
</tr>
<tr>
<td>Max Void Size</td>
<td>31%</td>
<td>30%</td>
<td></td>
</tr>
</tbody>
</table>

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**Voids in Bumping Process**

**Solder Paste Design**

**New Formula**

Shear strength of solder bump increased because of low voiding from new solder paste formula.

Shear strengths dropped after multiple reflow.

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Conclusion

Design
1. Select a suitable surface finish.
2. Choose right solder powder size.
3. Avoid microvia.
4. Design stencil aperture properly for large ground pad.

Process
1. Control the quality of incoming component and PCB. Low cost is not always the best!
2. Discuss with solder paste manufacturer for best reflow profile. Or try different soldering paste.
3. Use Nitrogen reflow or Vacuum reflow if possible.

Thank you!