

**IEEE SHORT COURSE****(Organized by IEEE Rel/CPMT/ED Singapore Chapter)****“Electrostatic Discharge (ESD) Protection in BiCMOS/CMOS Technology: Overview, Testing, Modeling, Design, and RF Optimization”**

by

**Prof Juin J. Liou, *University of Central Florida, USA*****Date: 26 July 2007 (Thursday)****Time: 9:00am to 5:00pm****Venue: Hotel Rendezvous, 9 Bras Basah Road, Singapore 189559****Fee: (includes one lunch, two tea breaks and course notes)**

Full-time Students: S\$150 (documentation required)

IEEE Members: S\$300

Others: S\$350

**REGISTRATION DEADLINE: 18 July 2007****Enquiries: Mrs Jasmine Leong, Tel: 6743 2523, Email: [ipfa@pacific.net.sg](mailto:ipfa@pacific.net.sg)****OVERVIEW:**

Electrostatic discharge (ESD) is a process in which a finite amount of charge is transferred from one object (i.e., human body) to the other (i.e., microchip). This process can result in a very high current passing through the microchip within a very short period of time, and more than 35% of chip damages can be attributed to such an event. As such, designing robust on-chip ESD structures to protect microchips against ESD stress is a high priority in the semiconductor industry. In fact, many semiconductor companies worldwide are having difficulties in meeting the increasingly stringent ESD protection requirements for various electronics applications.

This short course gives a comprehensive coverage on various issues pertinent to ESD mechanism and protection, including ESD fundamentals, testing, modeling, design, and optimization in BiCMOS and CMOS technologies.

**OUTLINE:**

1. Overview of ESD (charge generation, damaging mechanisms, ESD standards, ESD protection schemes)
2. Issues of ESD testing and measurements (testing equipment, transmission line pulsing (TLP) technique)
3. ESD protection modeling (model development of MOSFET and SCR for ESD applications)
4. ESD protection design (example of practical ESD designs on data communication transceiver, gas sensor system-on-chip, and low-voltage IC)
5. ESD optimization for RF functionality integrity (optimization of ESD protection structure to minimize parasitic capacitance for RF applications)

**WHO WILL BENEFIT FROM THE COURSE:**

1. Managers and engineers working at companies involving in the design, fabrication, and characterization of analog, digital, mixed-mode, RF, MEMS, memory, and flat panel display.
2. Faculty and students specialized in the fields of semiconductor device, integrated circuit and electronics system in general.

**ABOUT THE INSTRUCTOR:**

*Juin J. Liou* received the B.S. (honors), M.S., and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1982, 1983, and 1987, respectively. In 1987, he joined the Department of Electrical and Computer Engineering at the University of Central Florida, Orlando, Florida where he is now a Professor. His current research interests are nanoelectronics computer-aided design, RF device modeling and simulation, and semiconductor manufacturing and reliability.

Dr. Liou has filed 3 patents, and has published 6 textbooks (another in progress), more than 210 journal papers (including 13 invited articles), and more than 160 papers (including 58 keynote or invited papers) in international and national conference proceedings. He has been awarded more than \$7.0 million of research grants from federal agencies (i.e., NSF, DARPA, Navy, Air Force, NIST), state government, and industry (i.e., Semiconductor Research Corp., Intel Corp., Intersil Corp., Lucent Technologies, Alcatel Space, Conexant Systems, Texas Instruments, Lockheed Martin, Analog Devices, Fairchild Semiconductor), and has held consulting positions with research laboratories and companies in the United States, Japan, Taiwan, and Singapore. In addition, Dr. Liou serves as a technical reviewer for various journals and publishers, chair or member of the technical program committee for several international conferences, external examiner for several universities, and regional editor (in USA, Canada and South America) for the *Microelectronics Reliability* Journal.

Dr. Liou received ten different awards on excellence in teaching and research from the University of Central Florida (UCF) and six different awards from the IEEE Electron Device Society (EDS). Among them, he was awarded the UCF Distinguished Researcher Award three times (1992, 1998, 2002), UCF Research Incentive Award two times (2000, 2005), and IEEE Joseph M. Biedenbach Outstanding Educator Award in 2004 for his exemplary teaching, research, and international collaboration. His other honors include Fellow of the IEE, Trustee Chair Professor of UCF, Cao Guang-Biao Endowed Professor of Zhejiang University, China, Consultant Professor of Huazhong University of Science and Technology, Wuhan, China, Courtesy Professor of Shanghai Jiao Tong University, Shanghai, China, IEEE EDS Distinguished Lecturer, and National Science Council Distinguished Lecturer.

Dr. Liou served as the IEEE EDS Vice-President for Regions/Chapters, IEEE EDS Treasurer, IEEE EDS Finance Committee Chair, Elected Member of IEEE EDS Administrative Committee, and Member of IEEE EDS Educational Activities Committee.