

IEEE TECHNICAL TALK

Organized by IEEE Rel/CPMT/ED Singapore Chapter and
co-hosted by Silicon Technology Group, Microelectronics Centre, NTU

“Electrostatic Discharge (ESD) In the Nano-electronic Era”

Speaker : **Dr Steven H. Voldman, IEEE Fellow**
IBM, USA

Date : **23 February 2007, Friday**

Time : **4:00pm**

Venue : Nanyang Technological University, School of EEE
Block S2.2, Executive Seminar Room (S2.2-B2-53)

Map: http://www.street-directory.com/ntu/campus.cgi?no=School+of+Electrical+and+Electronic+Engineering+%28EEE%2C+Block+S2.2%29&map_search=nanyang&search.x=19&search.y=5

Admission : Free

ABSTRACT

Electrostatic Discharge (ESD) phenomenon today is a reliability concern in semiconductor components, systems from cell phones, laptops, to automotive products. A key question today in the semiconductor industry is whether electrostatic discharge (ESD) sensitivity will be a roadblock to the introduction, manufacturability or implementation of today's technology, and of future nano-structures? A first question - Is this an issue in the future, or are we already in the ESD roadblock condition today? To start this dialogue, we must ask where we are today in the present technology, and what is the technical trend that we are experiencing in the electrostatic sensitivity.

In this talk, we will discuss the direction of semiconductor technology from digital, analog and radio frequency (RF) applications. We will first discuss CMOS technology and the ESD Technology Roadmap highlighting the trend in the semiconductor industry; this will be followed by a discussion on the trend in CMOS, Silicon on Insulator (SOI), strained Silicon, to FINFET devices. For RF technology, ESD trends and advances in RF CMOS, BiCMOS Silicon Germanium, Silicon Germanium Carbon, Gallium Arsenide, and RF MEMs will be reviewed. The presentation will also include the magnetic recording industry's transition from MR heads, to tunneling MR (TMR) heads and the ESD implications. Electrostatic discharge issues associated with photomasks, and reticles in the mask product process will also be highlighted. Off-chip protection concepts such as polymer voltage suppression (PVS) devices will also be discussed.

ABOUT THE SPEAKER

Dr. Steven H. Voldman is an IEEE Fellow for "Contributions in ESD protection in CMOS, Silicon On Insulator (SOI) and Silicon Germanium (SiGe) Technology." He received his B.S. Eng. Science from University of Buffalo (1979); a M.S. EE (1981) and Electrical Engineer Degree (1982) from Massachusetts Institute of Technology (MIT); and a MS Eng. Physics (1986) and Ph.D EE (1991) from University of Vermont under IBM's Resident Study Fellow program.

In IBM, since 1982, Dr. Voldman worked on many semiconductor reliability areas from MOSFET design, hot electron, soft error rate (SER), and MOSFET gate-induced drain leakage (GIDL). Dr. Voldman was responsible for CMOS latchup since 1984, and ESD since 1991. He has been a member of IBM's Bipolar SRAM development, CMOS DRAM, CMOS logic, and SOI technologies. He is presently in IBM's BiCMOS Silicon Germanium, RF CMOS, RF SOI, power and image processing technology teams.

Dr. Voldman served as the SEMATECH ESD Working Group Chairman (1995-2000) for the US semiconductor industry. He has served as the ESD Symposium General Chairman, and presently serving on the ESD Association Board of Directors, ESDA Education Committee, ESD Technology Roadmap Committee, ESD Standards Chairman for Transmission Line Pulse (TLP) testing and Very-Fast TLP (VF-TLP) testing, and all other ESD/latchup device standards committees.

Dr. Voldman initiated the "ESD on Campus" program to bring ESD lectures and tutorials to faculty and students internationally. The ESD lecture program has visited universities in United States, China, Singapore, Taiwan, and Malaysia. The ESD on Campus lecture program has provided visits and technical lectures at Jiao Tung University (Shanghai), Fudan University (Shanghai), Zhejiang University (Hangzhou, China), National University of Singapore (NUS), National Taiwan University of Science and Technology (NTUST), National Taiwan University (NTU), National Chiao-Tung University (NCTU), Stanford University, University of Illinois Champaign Urbana (UIUC), University Wisconsin Milwaukee, (UWM), and University of Arizona (UA).

Dr. Voldman serves on the technical program committees of the EOS/ESD Symposium, International ESD Workshop (IEW), Taiwan ESD Conference (T-ESDC, Hsinchu), International Conference on Electromagnetic Applications and Compatibility (ICEMAC, Taipei), International Physical and Failure Analysis (IPFA, Singapore), International Reliability Physics Symposium (IRPS), and Bipolar/BiCMOS Technology Meeting (BCTM).

Steve Voldman is an author of a three book series -- on ESD physics, ESD: Physics and Devices, a second text on ESD circuits, ESD: Circuits and Devices, and a new text ESD:RF Technology and Circuits, as well as a contributor to Silicon Germanium: Technology, Modeling and Design. He has written over 150 technical papers, and recipient of 156 issued US patents and 70 US patents pending in the area of semiconductor technology, CMOS latchup and ESD, where the patents include semiconductor devices, circuits and software.