IEEE Reliability / CPMT / ED Singapore Chapter

The 20th WIMNACT - Singapore

Workshop and IEEE EDS Mini-colloquium on NAnometer CMOS Technology

Organized and Sponsored by IEEE Rel/CPMT/ED Singapore Chapter
Co-hosted by Microelectronics Centre, School of EEE, Nanyang Technological University

Date/Time: **11 August 2009 (Tuesday), 1:15pm to 4:30pm**

Venue: **Executive Seminar Room, Block S2.2 (S2.2-B2-53), NTU**
Map:
http://www.street-directory.com/ntu/campus.cgi?no=School+of+Electrical+and+Electronic+Engineering+%28EEE%2C+Block+S2.2%29&map_search=nanyang&search.x=19&search.y=5

Admission: **Free -** Please pre-register with Ms Jasmine Leong by filling in the Registration Form (separate Word document file) and email to ipfa@pacific.net.sg

Program

1:15 – 1:30 ***REGISTRATION***

1:30 – 1:35 **Welcome Address by Chair, School of EEE, NTU**
Prof. Kam Chan Hin, Chair, School of EEE, NTU, Singapore

1:35 – 1:45 **Opening Address by IEEE Singapore Rel/CPMT/ED Chapter Chair**
Prof. Kin-Leong Pey, Head, Microelectronics Division, EEE, NTU, Singapore

1:45 – 1:55 **Introduction to IEEE EDS**
Dr. Samar Saha, IEEE EDS VP Publications

2:00 – 2:50 **Modeling and Simulation of Flash Memory Devices**
Prof. Juzer Vasi, Indian Institute of Technology, Bombay, India

2:50 – 3:40 **Polymer Based Sensor Systems for Healthcare & Homeland Security**
Prof. Ramgopal Rao, Indian Institute of Technology, Bombay, India

3:40 – 4:30 **Device Considerations for Ultra-Low Voltage Analog Integrated Circuits**
Dr. Samar Saha, Silterra USA Inc., USA

4:30 ***CLOSING REMARKS & REFRESHMENTS***

Related websites:

WIMNACT	`http://www.ntu.edu.sg/eee/eee6/conf/WIMNACT09.htm`
Rel/CPMT/ED	`http://ewh.ieee.org/soc/cpmt/singapore/`
IEEE/EDS	`http://www.ieee.org/portal/pages/society/eds/`

2:00 – 2:50 **Modeling and Simulation of Flash Memory Devices**
Prof. Juzer Vasi, Indian Institute of Technology, Bombay, India

***ABSTRACT*:**

Non-volatile flash memories constitute the fastest growing segment of semiconductors. Two recent charge-trap flash cells, the SONOS and the nanocrystal, show promise for continued scaling. To realize this promise, it is important to understand the physical mechanisms involved in the operation of the devices, and to model these well. This talk presents work done at IIT Bombay on the modeling and simulation of charge-trap flash memory cells.

***BIOGRAPHY*:**

Juzer Vasi obtained his B.Tech. from the Indian Institute of Technology, Bombay in 1969 and the Ph.D. from The Johns Hopkins University in 1973. He taught at The Johns Hopkins University and the Indian Institute of Technology, Delhi, before moving to the Indian Institute of Technology, Bombay in 1981, where he is currently a Professor. At IIT Bombay, he has been Head of the Department of Electrical Engineering from 1992-1994 and Deputy Director from 2006-2009.

His research interests are in the area of CMOS devices, technology and design. He has worked on CMOS insulators, reliability of CMOS devices and memories, and modeling and simulation of MOS devices. He was Editor of the IEEE Transactions on Electron Devices for MOS Devices and Technology from 1996 to 2003. He is a recipient of IIT Bombay's awards for Excellence in Teaching as well as Excellence in Research. He is a member of the Scientific Advisory Committee to the Cabinet of the Government of India. He is a Fellow of IEEE, a Fellow of the Indian National Academy of Engineering, and a Fellow of IETE.

2:50 – 3:40 **Polymer Based Sensor Systems for Healthcare & Homeland Security**
Prof. Ramgopal Rao, Indian Institute of Technology, Bombay, India

***ABSTRACT*:**

Micro fabricated sensors based on the detection of nano-mechanical motion are known to be promising for biochemical sensing. The use of conventional silicon based materials to fabricate microcantilevers results in a lower sensitivity and higher cost for the sensor depending on the Young's modulus of the structural material, the geometrical dimensions, as well as the process complexity. UV patternable polymer materials such as SU-8 have a very low Young's modulus compared to the silicon (Si) based materials, are cheaper, and show excellent promise as structural layers. In this talk, we discuss the progress made at IIT Bombay towards the development of a SU-8 microcantilever platform for sensing applications. The three approaches, namely the optical, piezo-resistive (with polysilicon films as well as with conductive nanoparticles dispersed in an epoxy matrix) and piezo-electric (based on a novel multi-ferroic material synthesized at IIT Bombay) read out schemes have been implemented using a low-cost polymeric cantilever platform. We demonstrate practical applications involving these novel cantilever platforms for cardiac diagnostics & explosive detection.

***BIOGRAPHY*:**

Dr. V. Ramgopal Rao is a Professor in the Department of Electrical Engineering, IIT Bombay. Dr. Rao has over 200 publications in the area of Electron Devices & Nanoelectronics in refereed international journals and conference proceedings and holds three patents, with seven US patents currently pending.

Prof. Rao received the coveted Shanti Swarup Bhatnagar Prize in Engineering Sciences (the highest scientific award for researchers in India) awarded by the Hon'ble Prime Minister, Govt of India in 2005 for his work on Electron Devices. He is also a recipient of the 2004 Swarnajayanti Fellowship award from DST, 2007 IBM Faculty award and the 2008 MRSI-ICSC Annual Prize. He is an Editor for the IEEE Transactions on Electron Devices in the CMOS Devices and Technology area and serves on the Editorial boards of three other international journals. Dr. Rao is a Fellow of the Indian National Academy of Engineering and a Fellow of the Indian Academy of Sciences. He is a

Distinguished Lecturer, IEEE Electron Devices Society and interacts closely with many semiconductor industries. He has served on the program/organizing committees of a large number of international conferences in the area of electron devices and was Chairman, IEEE AP/ED Bombay Chapter during 2002-2003. He currently serves on the executive committee of the IEEE Bombay Section besides being the vice-chair, IEEE Asia-Pacific Regions/Chapters Subcommittee.

For more information about Prof. Rao's current research interests, and a list of publications, please visit: http://www.ee.iitb.ac.in/~rrao.

3:40 – 4:30 **Device Considerations for Ultra-Low Voltage Analog Integrated Circuits**
Dr. Samar Saha, Silterra USA Inc., USA

***ABSTRACT*:**

The necessity for scaling power supply voltage in CMOS integrated circuits is mainly due to the scaling down of MOSFET devices, increasing power dissipation with increasing chip density, and mobile electronics. However, the standard CMOS technology has several limitations for ultra-low voltage analog operations. In this talk, the various limitations of standard scaled CMOS technologies for ultra-low voltage applications will be reviewed and the device techniques used to overcome theses limitations will be discussed. One of the devices used for the consideration of ultra-low voltage analog applications is the junction-field-effect transistor (JFET). In this talk a typical sub-90-nm n-channel JFET device will be introduced for ultra-low voltage operations. In order to achieve the target off-state leakage current and ON/OFF performance for 65-nm devices, the relevant device architecture and the corresponding device performance for the symmetric and asymmetric source-drain devices at ultra-low supply voltage of 0.5 V will be presented.

***BIOGRAPHY*:**

Dr. Samar K. Saha received the M.S degree in Engineering Management from Stanford University, CA, USA and the M.Sc. and Ph.D. degrees in Solid State Physics from Gauhati University, Guwahati, India. Dr. Saha worked as an Assistant Professor in Electrical Engineering Department at Southern Illinois University, Carbondale, IL, and Auburn University, Auburn, AL. Since 1984 he has worked in various positions for National Semiconductor Corporation, LSI Logic Corporation, Texas Instruments, Philips Semiconductors, Silicon Storage Technology, Synopsys, and DSM Solutions. Currently, he is the Director of Design Technology at Silterra USA, Inc., and an Adjunct Professor in Electrical Engineering Department at Santa Clara University, Santa Clara, CA. His research interests include nanoscale device and process architecture, Technology CAD, Compact modeling, and TCAD and R&D management. He has authored more than 70 research papers, holds six US patents, and offered numerous tutorials/short-courses on compact modeling and Technology CAD.

Dr. Saha is the Vice President of EDS Publications and elected member of Electron Devices Society (EDS) Administrative Committee. He is a senior member of IEEE and Distinguished Lecturer of EDS. He is, also, the principal guest editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES (T-ED) Special Issue (SI) on "Compact Interconnect Models for Giga Scale Integration." He has served as the principal guest-editor of the T-ED SI on "Advanced Compact Models and 45-nm Modeling Challenges," Region-5&6 editor of the EDS Newsletter, EDS representative to the editorial steering committee of IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, chair of IEEE-EDS Compact Modeling Technical Committee, chair of EDS SRC-NAW, member of EDS publications committee, EDS representative to the Council of Electronic Design Automation (C-EDA), and the chair of IEEE EDS Santa Clara Valley chapter. He is listed in *Who's Who in America* and *Who's Who in the World*.