“Optimization of Electrical Package Design and PCB Design for CSP Age”

Atsushi Nakamura

Assembly Technology Development Dept.,
SIC, Hitachi, Ltd., JAPAN
Package Miniaturization (QFP > BGA > CSP)

MPU for consumer products has been shaping up his body smaller and smaller

- **QFP**
  - Typical Die size
  - 28mm
  - 2828-208pin (256pin/0.4mm)

- **BGA**
  - 2727-256pin

- **CSP**
  - 1313-240pin
  - 1111-256pin

- **WLP**
  - FBGA (Fine-pitch BGA)
Bottleneck for High speed operation: **Interconnect Design**

- **Signal** [Reflection, Crosstalk, ……]
- **Supply** [SSN]
- **Supply** [Emission]

**SI (Signal Integrity)**
**PI (Power Integrity)**
**EMI (Electromagnetic Interference)**

**Higher Freq. Operation**

**Interconnect**

Driver - **Interconnect** - Receiver
Impedance matching at Driver/TML and TML/Receiver

Near End  Far End

Driver  Receiver
Waveform comparison on Termination, TML length

Case 1

Case 2

Case 3

Case 4

200mm

50mm

10mm
Miniaturization in Digital Consumer Products

Mega pixel capture in Less than “half inch”

“SiP vs SoC”, NIKKEI MICRODEVICES magazine, p65, No.208, Oct. 2002

Flip Chip “SiP”
(CPU, CPU/DSP, SDRAM, Flash)
Bottleneck for High speed operation: **Interconnect Design**

Higher Freq. Operation → **SI (Signal Integrity)**

**PI (Power Integrity)**

**EMI (Electromagnetic Interference)**

**Signal** [Reflection, Crosstalk, ……]

**Supply** [SSN]

**Supply** [Emission]

Driver to Receiver Interconnect

#7 Oct. 2002
PCB Modeling for Power Integrity Analysis

Analysis Vehicle

- BGA package
- PCB: 4 Layers
- PKG (BGA): 2 Layers
- Total: 6 Layers

LSI Package, BUS traces and V/G plane conductors in PCB should be analyzed in a single model for field solver.

Evaluation board for SH4(BGA)

Analysis model (Traces, planes, and PKG)
(1) Estimation from measured waveform

```
\[ \Delta V = 1.35 \text{V} \]
\[ \Delta V = -0.28 \text{V} \]
\[ di/dt = 0.261 \text{A/ns} \]
```

\[ L_{1\text{eff}} = 5.17 \text{nH} \]
\[ L_{2\text{eff}} = 1.07 \text{nH} \]

(2) EM analysis

```
\[ L_1 = 9.81 \text{nH} \]
\[ M = 4.65 \text{nH} \]
\[ L_2 = 5.74 \text{nH} \]
```

\[ L_{1\text{eff}} = L_1 - M = 5.16 \text{nH} \]
\[ L_{2\text{eff}} = L_2 - M = 1.09 \text{nH} \]
SSN waveform extraction at low frequency operation

Switching 63 I/O traces simultaneously
Comparison between measured and simulated waveform

SSN evaluation point

Switching 63 I/O traces simultaneously

SSN Waveform on a quiet line out of 31 switching lines

Data bus

Quiet (low)

0.09 V

Mes.

Sim.

0.06 V

Mes.

Sim.
SSN waveform difference obtained at different point on the quiet trace
Peak voltage increase proportional to trace length

(1) CPU (driver)
(2) SDRAM
(3) BUFFER

Initial SSN voltage
(package inductance)

Additional part
(crosstalk)

Quiet (Low)

SSN peak voltage (V)

Trace length from driver (mm)

Simulation

Experiment

SH4

SDRAM

BUFFER
Package dominant and PCB dominant region

Cross talk part is dominant on BUS system using low inductance packages (Less than 1nH)

![Graph showing the relationship between LSI package inductance and SSN induced by cross talk and package inductance with each noise peak voltage.](image-url)
Bottleneck for High speed operation: *Interconnect Design*

**Higher Freq. Operation**

- **SI (Signal Integrity)**
  - [Reflection, Crosstalk, ……]
- **PI (Power Integrity)**
- **EMI (Electromagnetic Interference)**
  - [SSN]
  - [Emission]

**Interconnect**

![Interconnect Diagram](image-url)

- **Driver**
- **Receiver**

**Graph**:

- **Active BUS Signal**
- **Quiet Sig.**
- **Threshold Level**

**Time (sec)**: 0.0E+00, 4.0E-08, 8.0E-08, 1.2E-07

**Voltage (volt)**: -1.0, 0.0, 1.0, 2.0, 3.0, 4.0
Low noise assembly Basics

- Minimize voltage fluctuation around CPU by Supply decoupling
- Increase current supply from DeCap (B) and decrease current from main Power supply (A)
- Current ratio A/C represents effectiveness of DeCaps

Diagram:

- Main Pwr. supply
- DeCap
- Measuring point (VDE method)
- Package
- Chip

Example of multiple Vcc/Vss micro
Noise current measurement

- Noise current can be measured by 1 ohm (VDE) probe
- Decoupling effect of Caps can be evaluated by w/ and w/o comparison

(1) VDE Method
Decoupling evaluation board

- Investigation for supply decoupling

  Current measurement point (Vcc, PVcc, Vss)

  Pads for Capacitors

  Pads for Inductor

  Ferrite Bead

  Capacitors
Supply Decoupling using Ferrite-Bead

- Ferrite Bead
- Core current
- I/O current
- Gnd Plane (w/o slit)
- Pwr plane
- Capacitor
- Slit (moat)
- Noise current (dBuV)

Graph:
- Noise current (dBuV) vs. # of capacitors
- Caps.
- Caps + F.Bead
- @ 80MHz
- Target Level
- -20dB
SH7055R(QFP) Supply Decoupling Evaluation

Compare the level of “RF current” in supply lines

Black bars represent current direction

Ref: No Cap  Cap(t12)  Cap(t12)+ FB
Four-axis Near Field Scanner

- **Scan area**: 300x300mm

[EMI-200](http://www.hitachi.co.jp/HDEV/products/production/emi2/)

Example of "Surface scanning"
NF-Probe evaluates Fwd/Bkd current balance in PCB

Far field field strength estimation

Point out the location generating Common mode current
Hitachi, Semiconductor

Narrow & Asymmetric Ref. plane effect

pitch : 5mm   Scan hight : 10mm
Scanned from bottom side (Ref. plane)

MSL

terminated

100MHz (Sinusoidal)
Vp-p:1.0 volt input applied

@100MHz

# 23
Oct. 2002
pitch: 5mm  Scan height: 10mm
Scanned from bottom side (Ref. plane)

Narrow & Asymmetric Ref. plane effect

100MHz (Sinusoidal)
Vp-p: 1.0 volt  input applied

@100MHz
“QFP vs WLP” Current distribution [NF-probe scan]

Pitch: 2mm, Height: 5mm (above board)

Oct. 2002

@80MHz
Conducted emission “QFP vs WLP” [VDE method]

- **QFP**
  - [w/o Cap]
  - [w/ Cap]

- **WLP**
  - [w/o Cap]
  - [w/ Cap]

- **Higher emission over 250MHz**
Inductance comparison “QFP vs WLP”

<table>
<thead>
<tr>
<th></th>
<th>QFP</th>
<th>BGA</th>
<th>Pwr/Gnd</th>
<th>CSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire part</td>
<td>2.0 - 3.0nH</td>
<td>2.0 - 3.0nH</td>
<td>(1.8 - 2.2nH)</td>
<td>-</td>
</tr>
<tr>
<td>Rest of wire part</td>
<td>5.0 - 8.5nH</td>
<td>2.0 - 3.5nH</td>
<td>(0.8 - 1.2nH)</td>
<td>0.7 - 2.5nH</td>
</tr>
<tr>
<td>Total</td>
<td><strong>7.0 - 11.5nH</strong></td>
<td><strong>4.0 - 6.5nH</strong></td>
<td><strong>(2.6 - 3.4nH)</strong></td>
<td><strong>0.7 - 2.5nH</strong></td>
</tr>
</tbody>
</table>

Mutual inductance

(Leff)

Wire part

Rest of wire part

Total

QFP

BGA

Pwr/Gnd

CSP

Single

Two conductor in parallel

10nH

(10nH+8nH) x 1/2 = 9nH

10mm

27mm

10nH

2.0 - 3.0nH

8nH

4.0 - 6.5nH

(10nH+8nH)

9nH

(0.7 - 2.5nH)

(2.6 - 3.4nH)

(0.8 - 1.2nH)

(1.8 - 2.2nH)

(0.7 - 2.5nH)
Decoupling Capacitor connection [QFP vs BGA]

- Typical DeCap connection for QFP is better than BGA
- V/G plane is closer to Vcc/Vss pin than DeCaps
- Needs treatment to reduce current flow from V/G plane

[ QFP package + PCB ]

[ BGA package + PCB ]

DeCap position A or B
Decoupling capacitors for BGA

Topside (BGA mount)

Bottom side
Cost effective Low ESL Capacitors

“IDC” type capacitor

Conventional SMD

Feed through (Three terminal)

No extra Path!
100% supply must be fed through

| GLLD11 SERIES | L (mm) | 2.00±0.15 |
|               | W (mm) | 1.25±0.15 |
|               | T (mm) | 0.65±0.10 |
|               | G (mm) | 0.20±0.10 |
|               | CL (mm) | 0.20±0.10 |
|               | P (mm) | 0.50±0.10 |

Capacitance: 1.0μF
Lower Tolerance: ±20%
Upper Tolerance: ±20%
Rated Current: 2A
Rated Voltage: 16Vdc
Insulation Resistance: 500M ohm min.
Withstand Voltage:
Max. of DC resistance: 0.03ohm
Min. of Operating Temp. : -40°C
Max. of Operating Temp.: +85°C
Length: 2.0mm
Width: 1.25mm
Thickness: 0.85mm
Near Field Scan [Macro (Sensitive) probe] @80MHz

8 DeCaps (0.1mF*8)

-20dB

One Feed Through Capacitor (BGA)

VDE measurement point

SH7055R (40MHz)
Near Field Scan [Macro (Sensitive) probe] @80MHz

12 DeCaps (0.1mF*12)

VDE Measurements

-20dB

One Feed Through (1mF)

-10 0 10 20 30 40 50 60 70 80

Frequency [MHz]

-20dB 0 100 200 300 400 500 600 700 800 900 1000

Noise [dBµV]

w/o DeCaps 12 DeCaps NFM21

SH7055R (40MHz)

NFM21

DeCaps (Vcc)

DeCaps (PVcc, AVcc)

QFP

QFP 256p

-10

0

10

20

30

40

50

60

70

80

0 100 200 300 400 500 600 700 800 900 1000

Frequency [MHz]

VDE Measurements

w/o DeCaps 12 DeCaps NFM21
Current distribution [Simulation/ECTAS]

No Decoupling Capacitor

@80MHz

140 dBuA/m
50

7 traditional Capacitors

- 20dB

- 40dB

One feed-through capacitor
Effectiveness of Feed-through capacitor [Exp. vs Sim.]

Current distribution at this frequency was shown in the previous slide.

Conducted emission reduction capability “Conventional” vs “Feed through”
Radiation from External BUS

Area and Level of RF currents can be reduced by using SiP --> Low radiation chance from PCB

[SH4+SDRAM] demo board(4L) (HJ940001BP) equivalent

MCM (HJ940001BP)

Scanned plane : above 5mm from board surface

@ 81.0MHz (Ext BUS Freq)

Prog Exec (same prog for Demo board and MCM)

Scanned plane : above 5mm from chip surface

Current Direction Plot

Common Scale

Current Direction Plot

92.0
90.0
88.0
86.0
84.0
82.0
80.0
78.0
76.0
74.0
72.0
70.0
68.0
66.0
64.0
62.0
60.0
58.0
56.0
54.0
52.0
50.0
48.0
46.0
44.0
42.0
40.0
38.0
36.0
34.0
32.0
30.0
28.0
26.0
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
Summary

- Short trace interconnection (in SiP) solves most of the SI concern
- V/G plane analysis takes more important role for CSP age system
- Reduced EMI design is base on “Supply decoupling.” (for Single chip MPU)
- NF-Scanner shows us locations generating “Common mode” current
- Direct connection to V/G plane for CSP (BGA) is not recommended
- Feed-through Capacitor is a good solution for CSP’s decoupling saving space, great decoupling capability, making sense (cents)
- PCB design locating RF current trace adjacent to Gnd (return) path reduces emission. (ex. FC-SiP)