
Clock Distribution for Multi-GHz Microprocessors

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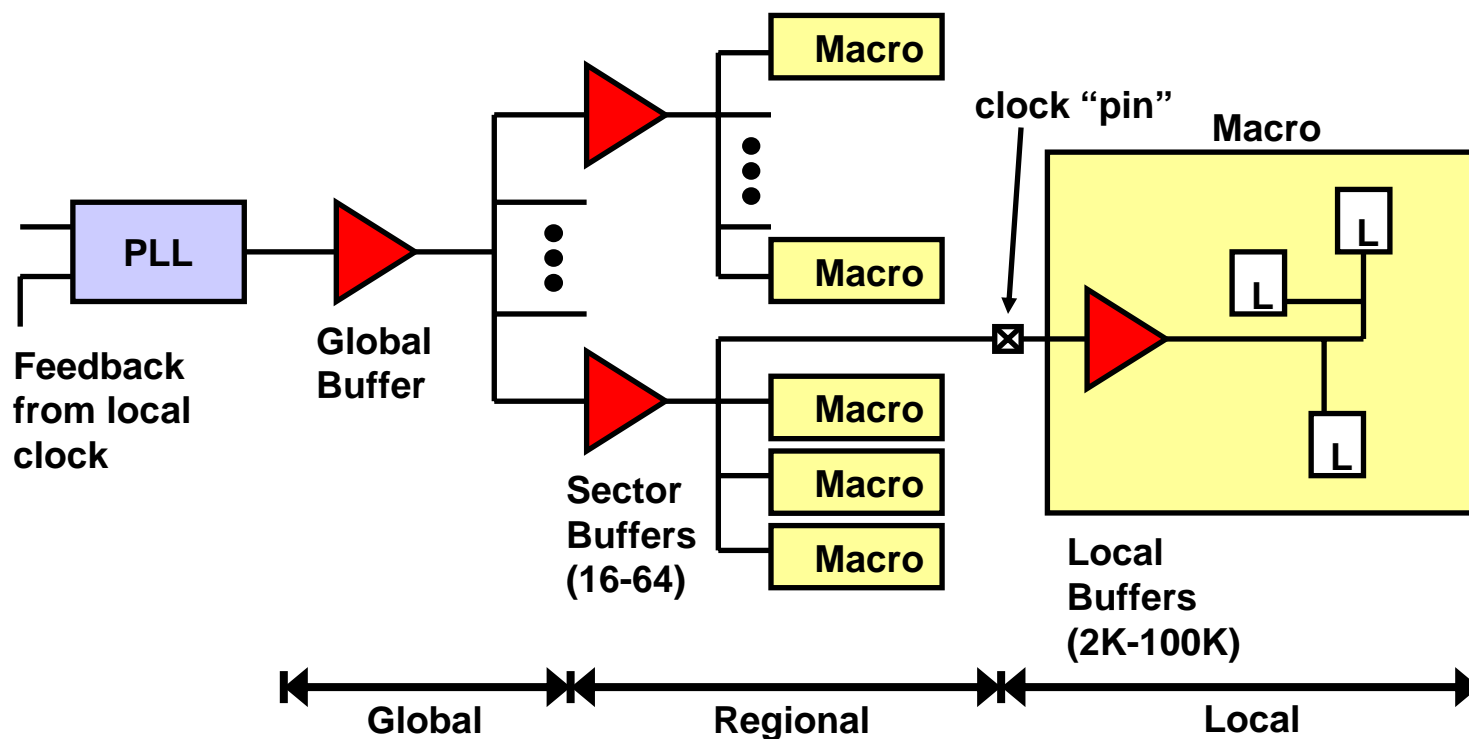
Outline

- I. Introduction to clock distribution
- II. Overview of conventional clock networks
- III. Scaling of clock networks
- IV. Directions for global clock networks
- V. Conclusions

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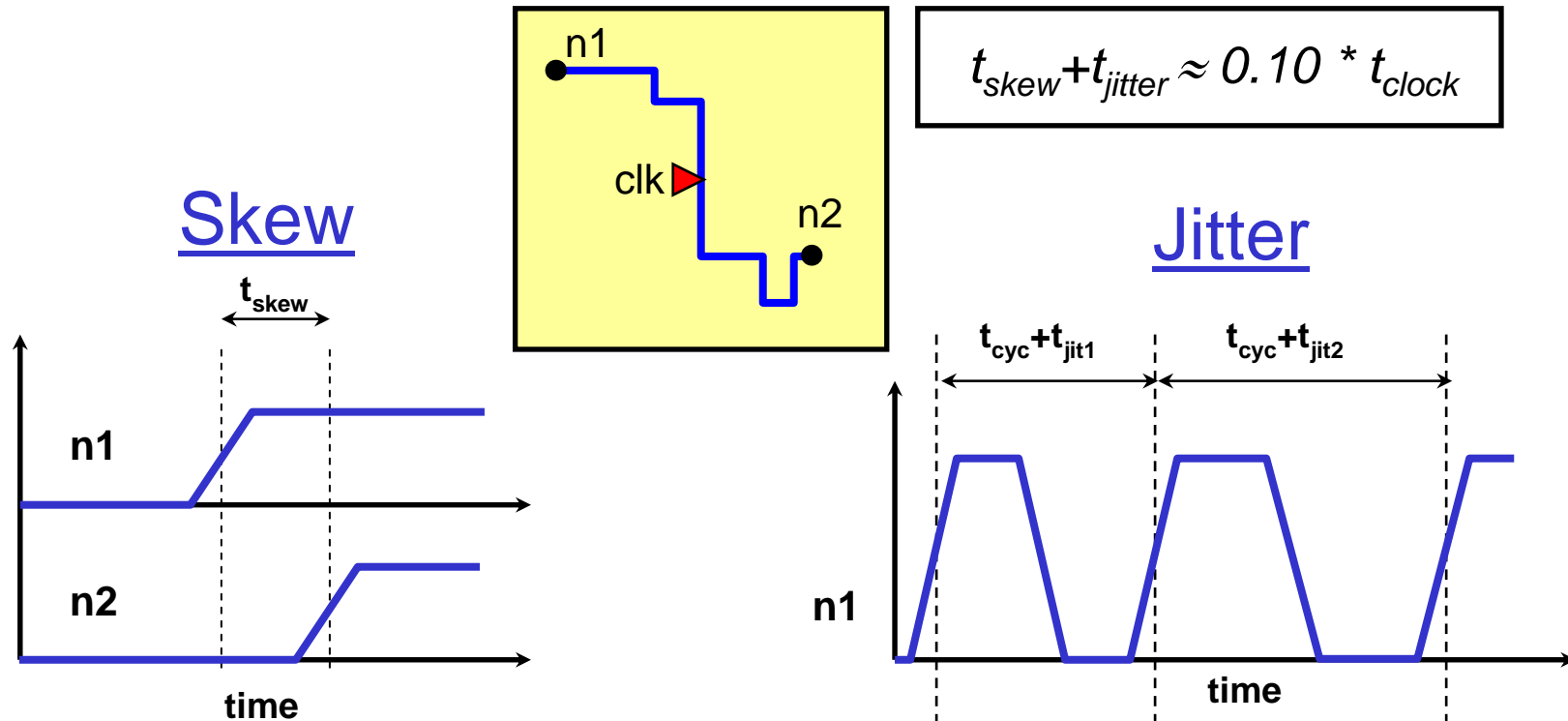
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Conventional Clock Networks



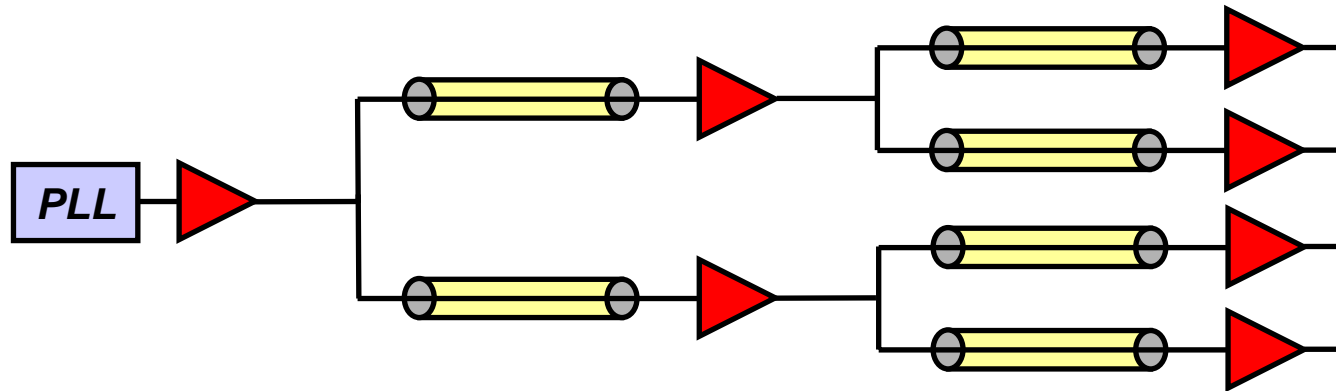
- Clock networks have a hierarchy
- Designed to minimize timing uncertainty, power, wire and silicon resources and maximize circuit performance

Clock Network Figures of Merit (I)



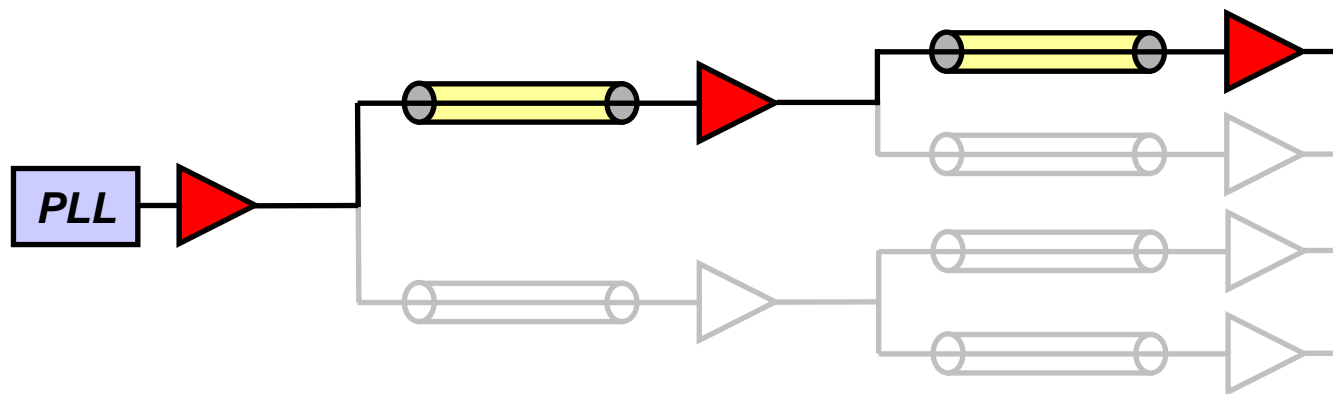
- Static timing error
- “Local” skew more important than “global” skew
- Dynamic timing error
- Divergence from nominal cycle time (*period jitter*)

Skew and Jitter Accumulation



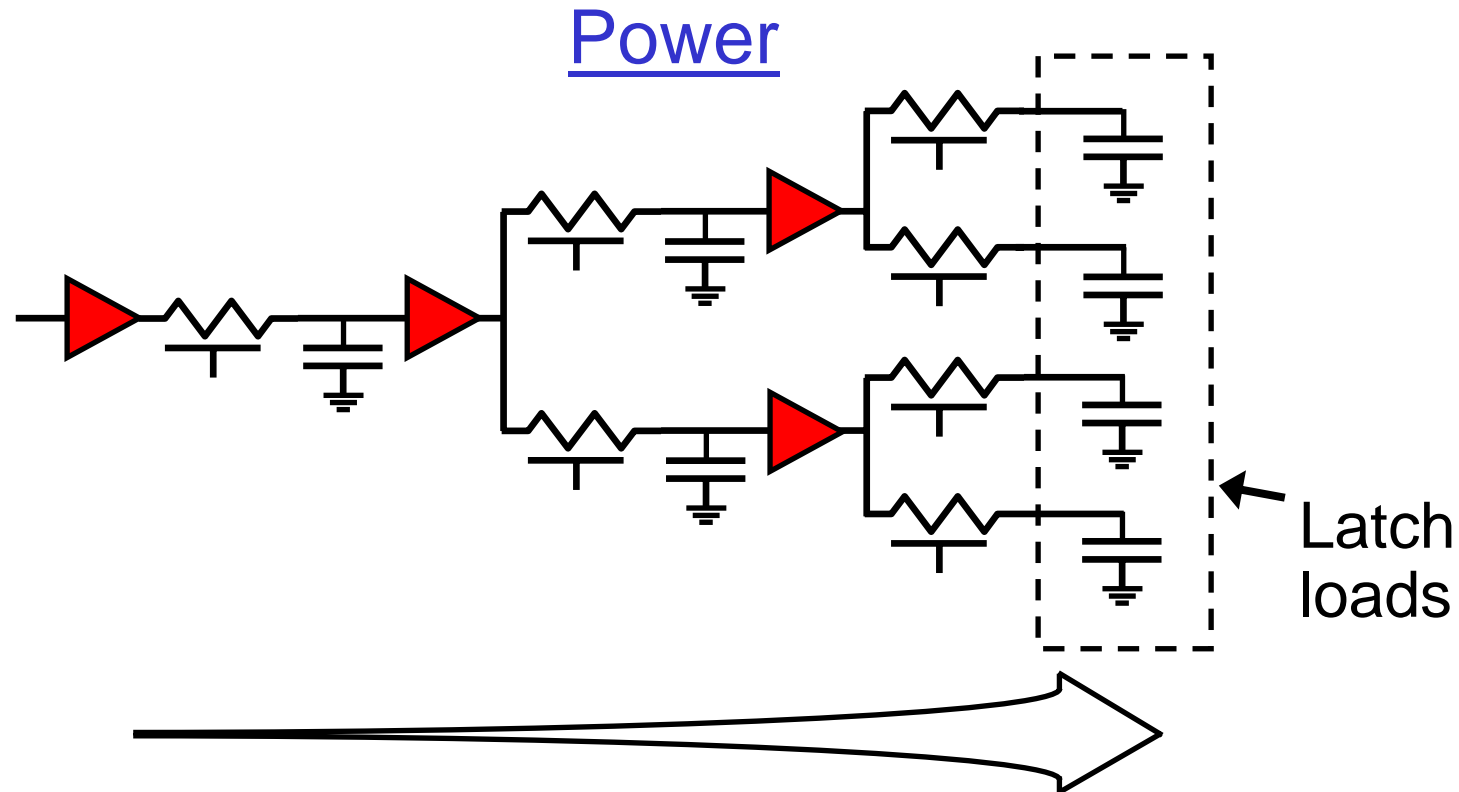
- Skew and jitter \propto Delay
 - Inverter delay
 - Power supply variation ($1\%t_{\text{delay}}/\%V_{\text{dd}}$)
 - Processing mismatch
 - Interconnect delay
 - Processing mismatch
 - Crosstalk
- Maximum slew rate possible reduces the impact of noise
 - This trades off with power, wire width, and number of buffer stages
- *Skew and jitter are dominated by the global and regional levels of the clock distribution network*

Skew and Jitter Accumulation



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Clock Network Figures of Merit (II)

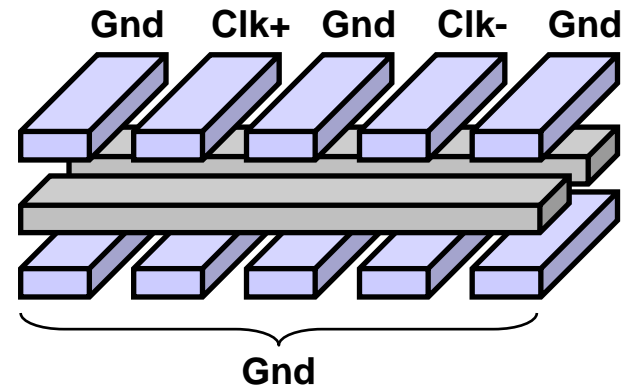
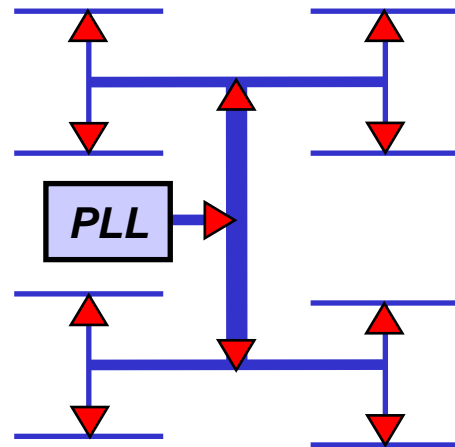


- Clock distribution is an exponential power fanout network ($\sim 10^5$)
- 20-40% of total microprocessor power
- *Power for local clock distribution is dominated by the local clock distribution ($\sim 10x$ the power in the other parts)*

Outline

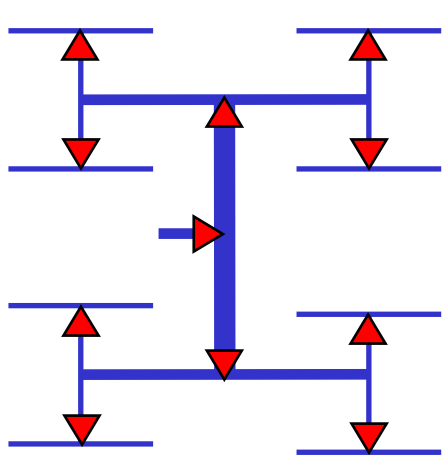
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Conventional: Global

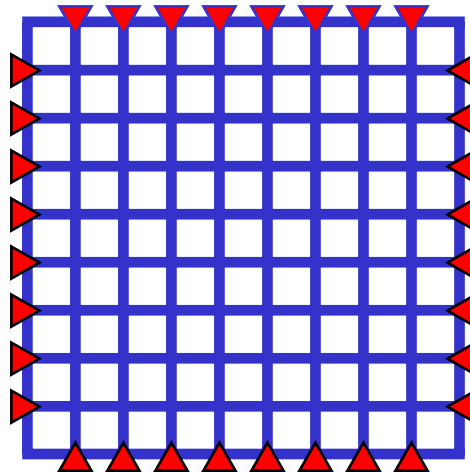


- H-tree is the dominant design
 - Provides nominally zero skew
 - Tunable for uneven loading
 - Easy to design
- Low fanout minimizes dispersion and timing uncertainty
- Interconnects are carefully designed
 - Differential, shielded, interleaved
 - RLC models

Conventional: Regional



H-tree



Grid

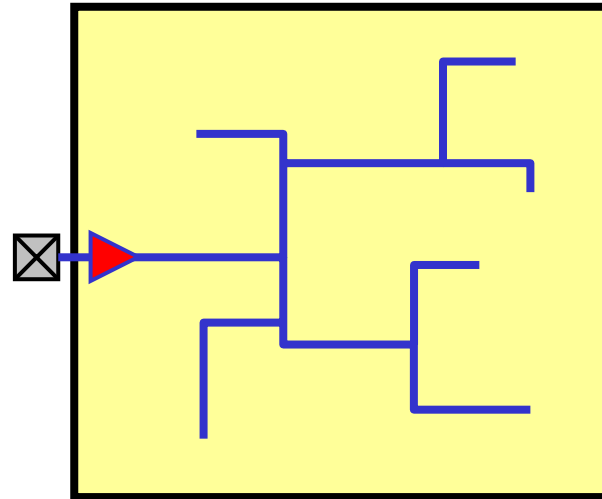


Serpentine

- No clear winner
 - Can have a significant impact on power and timing
- Interconnects may be shielded
- Hybrid clock networks
 - H-tree with grid

P. J. Restle and A. Deutsch, "Designing the best clock distribution network," Symp. VLSI Circuits '98.

Conventional: Local



Non-symmetric tree

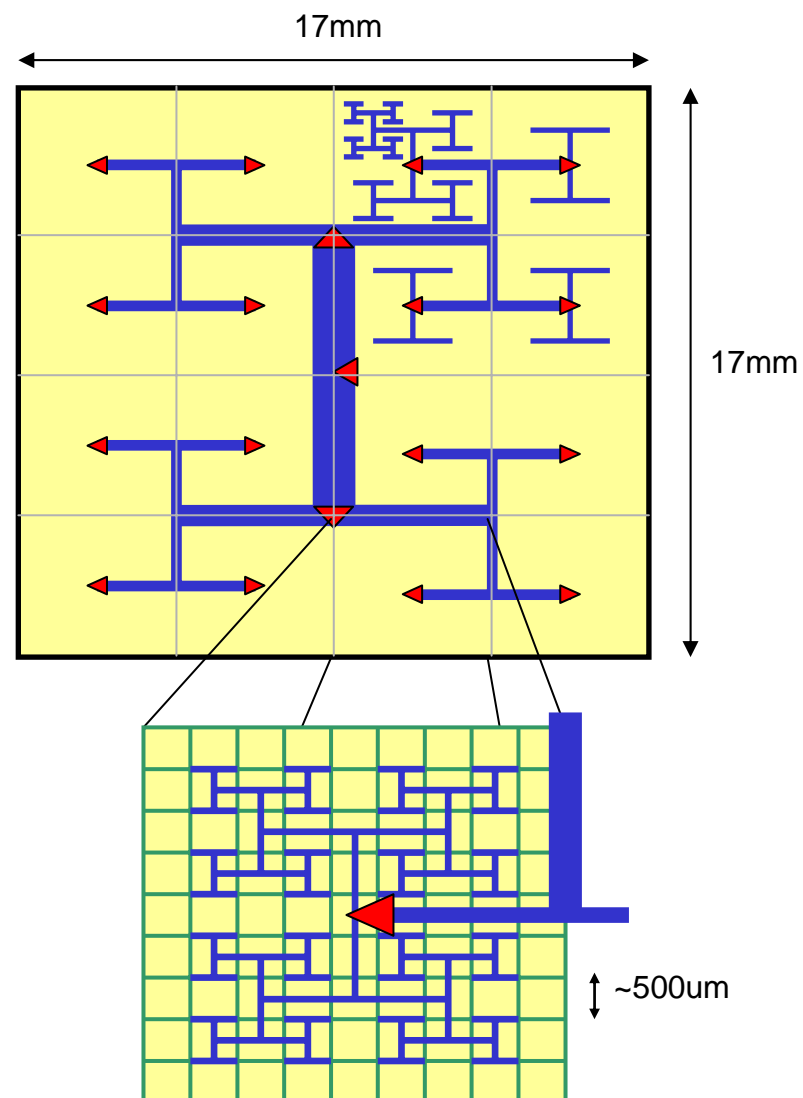
- Designed by macro owner using automatic synthesis tools
 - Change with loading changes within the macro
 - Less regular in structure than the upper levels of the hierarchy
- Clock may be a derivative of global clock

Example: 1GHz PowerPC, Y1999

	Y1999 PowerPC
Clock frequency	1.15GHz
Power	112W
Leff	0.12 μ m
Functions/chip	19M
Chip area	256mm ²
Clock pins	2339
Clock load	450-550pF
Clock node density	500 μ m
Levels of H-tree	5
Global buffers	1,2
Sector buffers	16

P. Hofstee et.al. "A 1GHz Single-Issue 64b PowerPC Processor", ISSCC'00

S. Posluszny et.al "Timing Closure by Design,' A High Frequency Microprocessor Design Methodology", DAC'00



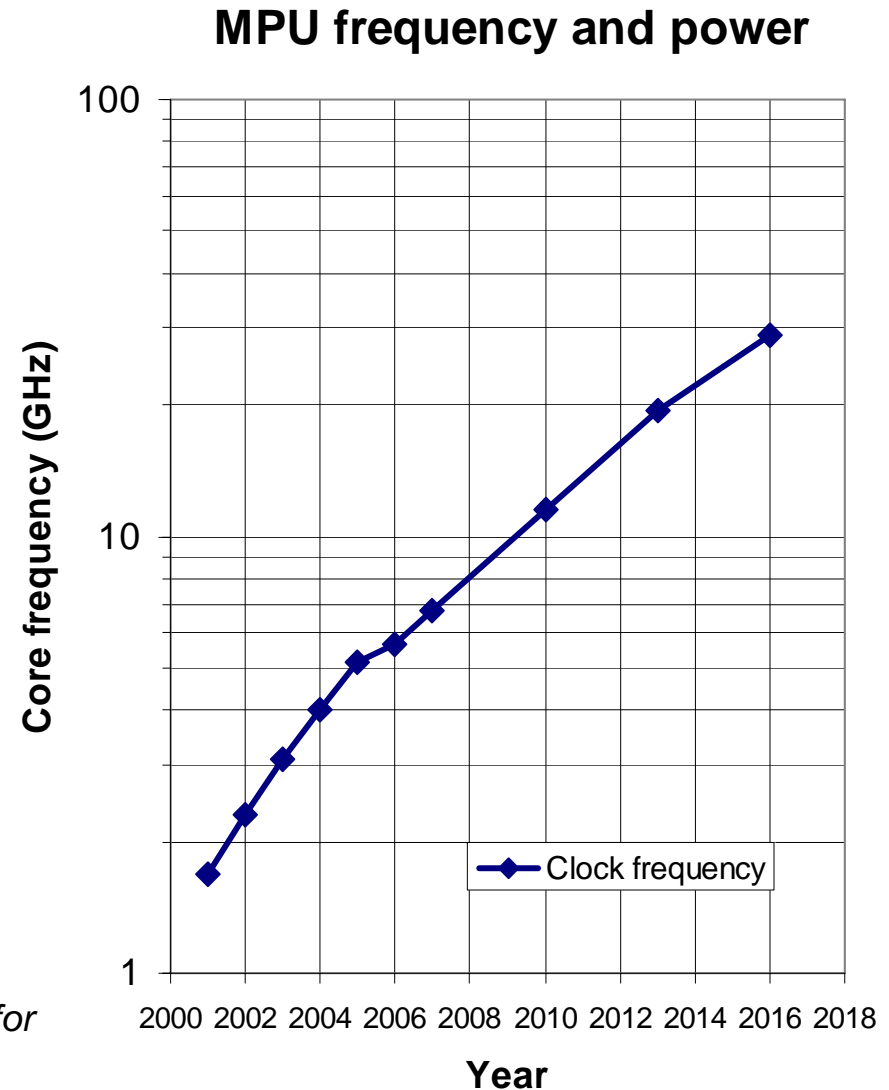
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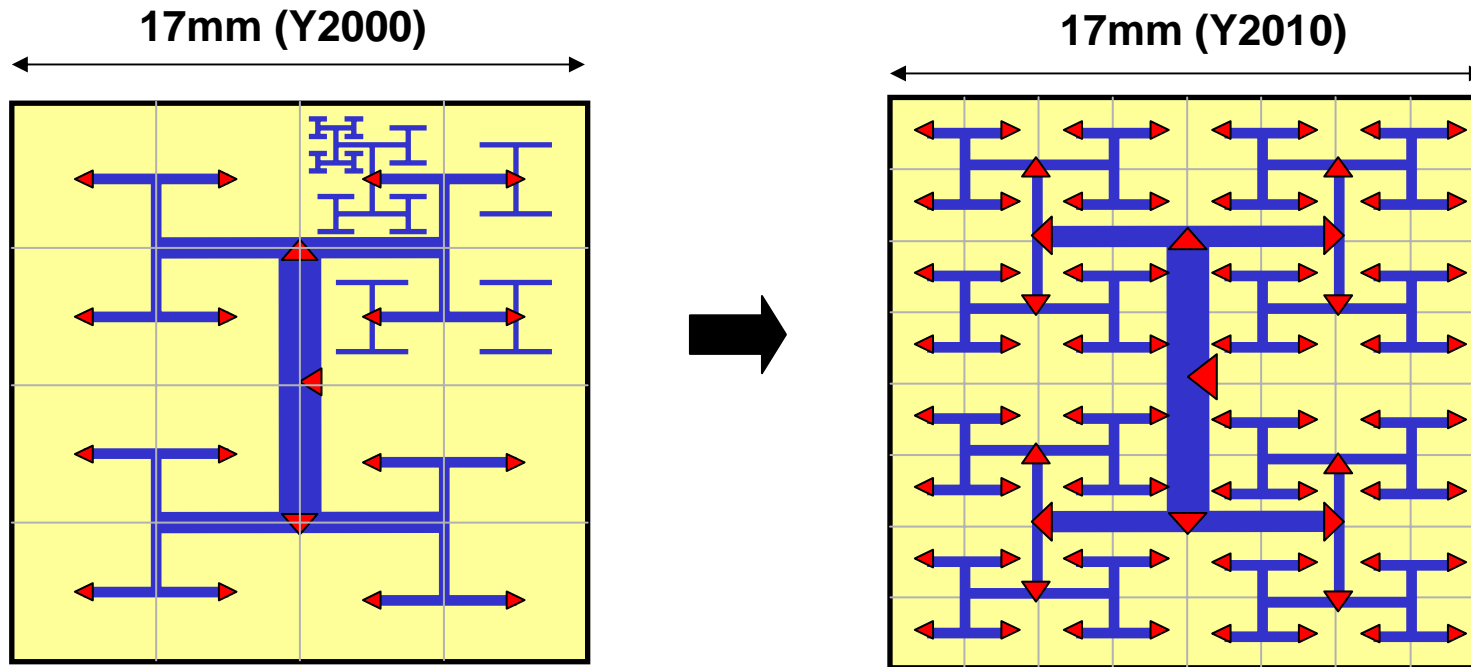
Microprocessor Scaling Trends

- Clock frequency
 - Maintain 16 FO4's between latches
- Area
 - 310mm² (~17.6mm / side)
- Power
 - V^2f product keeps pace with power prediction
- Device matching will get worse

Data based on International Technology Roadmap for Semiconductors (ITRS), 2001.



Scaling Global H-trees



Advantages	Disadvantages
<ul style="list-style-type: none">• Easy to design and layout• Low local skew• Design flexibility• Skew in a sector will be low	<ul style="list-style-type: none">• Skew and jitter accumulate• Latency does not scale• Interconnect effects

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Optimized buffered H-tree

- **Approach:** Use an algorithm and fast simulator to optimize H-tree timing uncertainty and power

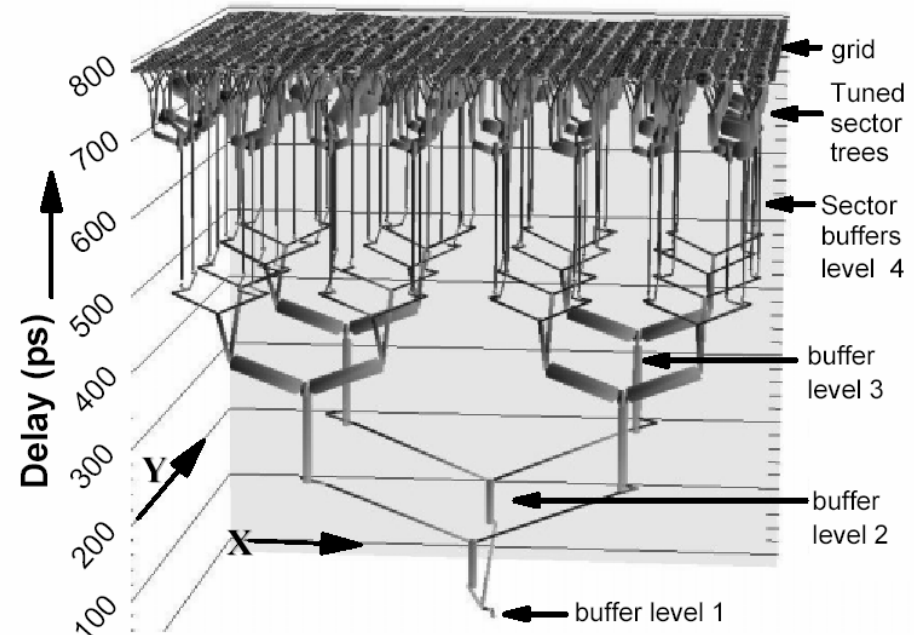
- Use adjacent return paths for all tree wires
- Short together clock at local grid
- Simulate worst-case buffer and wire delay variation using RLC wire models

- **Advantages**

- Regular geometric pattern is easy to design, analyze, and lay out
- Well known design issues since it has been the industry choice for clock distribution
- Local skew only determined by a small number of the buffers and wires
- Accommodates very nonuniform loading
- Paths can be intentionally skewed to improve the performance of some macro blocks
- Supports DFD/DFT

- **Disadvantages**

- Operates open-loop – no skew calibration
- Jitter is accumulated along the clock network
- Clock latency does not scale well



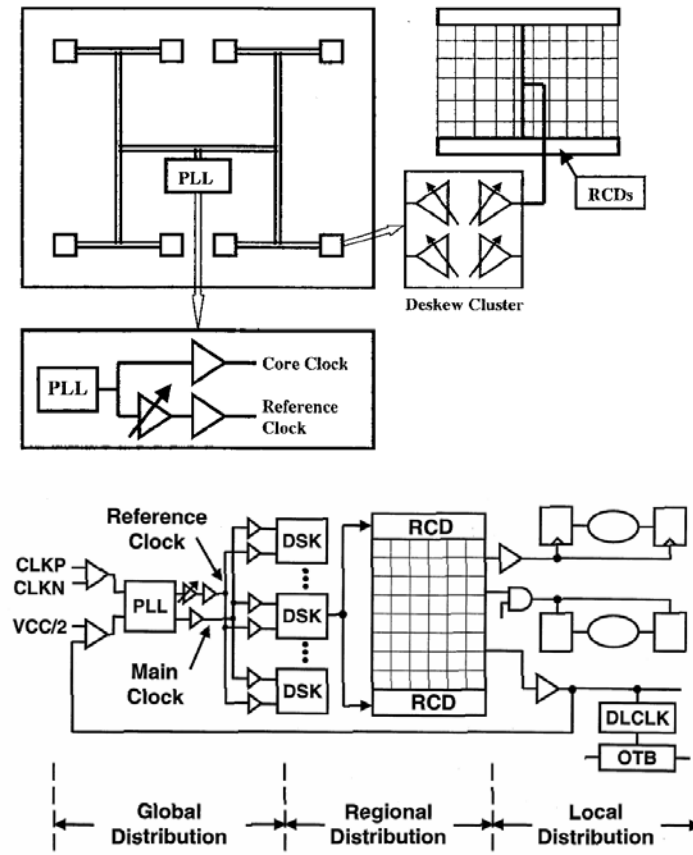
P. Restle et.al. "A clock distribution network for microprocessors", JSSC, May 2001.

P. Restle et.al. "The clock distribution of the POWER4 microprocessor", ISSCC 2002.

Clock frequency: 1.3GHz
Skew: 25ps (3.3%) measured
Jitter: 30ps p-p (3.9%) measured
<5ps (0.7%) for PLL

Buffered H-tree with deskew

- **Approach: Add deskew buffers to correct for within-die process variations**
 - Distribute two clock signals: the core clock and the reference clock
 - Reference clock has ideally balanced loading
 - Calibrate deskew buffers in the core clock path based on the timing of the reference clock
- **Advantages**
 - Same as for buffered H-tree
 - Compensates for within-die process variations and for modeling inaccuracies
 - Deskew buffers can be programmed to add and subtract delay manually for debug or to improve the performance of specific macros
- **Disadvantages**
 - Jitter is still accumulated along the clock network
 - Added complexity increases clock latency
 - Extra global clock network must be routed, using wire and silicon resources and power

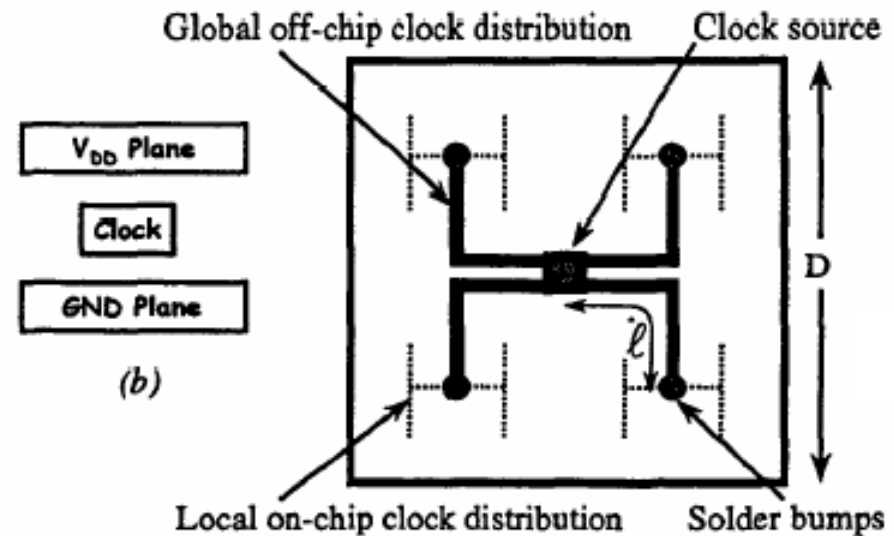


S. Tam et.al. "Clock generation and distribution for the first IA-64 microprocessor", JSSC, November 2000

Clock frequency: 800MHz
Skew: 28ps (2.2%) measured

Package level distribution

- **Approach: Use package-level transmission lines**
 - Push part of the global clock network to the package level
 - Conventional H-tree
 - Inject clock to chip at multiple points
- **Advantages**
 - Same as for buffered H-tree
 - Low wire loss and dispersion due to low-loss wires
 - Reduced area requirements
 - Potential for “energy recycling” with resonant lengths of transmission line
- **Disadvantages**
 - Solder-bump parasitics affect signal
 - ESD protection necessary on clock pad
 - Complicates testing



P. Zarkesh-Ha and J. Meindl, “Asymptotically zero power dissipation gigahertz clock distribution networks”, EPEP’99

Other Variations of H-tree

- **Shorting bars**
 - Phase-averaging similar to a grid at regional level
 - Bars become less effective at high frequencies
 - *N. Bindal et.al., “Scalable sub-10ps skew global clock distribution for a 90nm multi-GHz IA microprocessor,” ISSCC’03.*
- **Supply-invariant buffers**
 - Differential inverter buffers for common-mode rejection
 - Supply noise-tolerant inverters with loading that is inversely affected by power supply variations
 - *M. Mansuri and C.K. Yang, “A low-power low-jitter adaptive-bandwidth PLL and clock buffer”, ISSCC’03*
- **On-chip transmission lines**
 - Use extremely wide on-chip interconnects and large drivers
 - Extremely expensive for area and power
 - *M. Mizuno et.al. “On-chip multi-GHz clocking with transmission lines”, ISSCC’00*
- **Resonant H-tree**
 - Use multiple inductors to resonate out capacitance for reduced power dissipation
 - Unclear how this will effect skew and jitter
 - *S. Chen et.al, “Design of resonant global clock distributions,” ICCD’03*

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PLL Array

- *Approach:* Use a network of coupled PLLs to generate and distribute the sector clocks

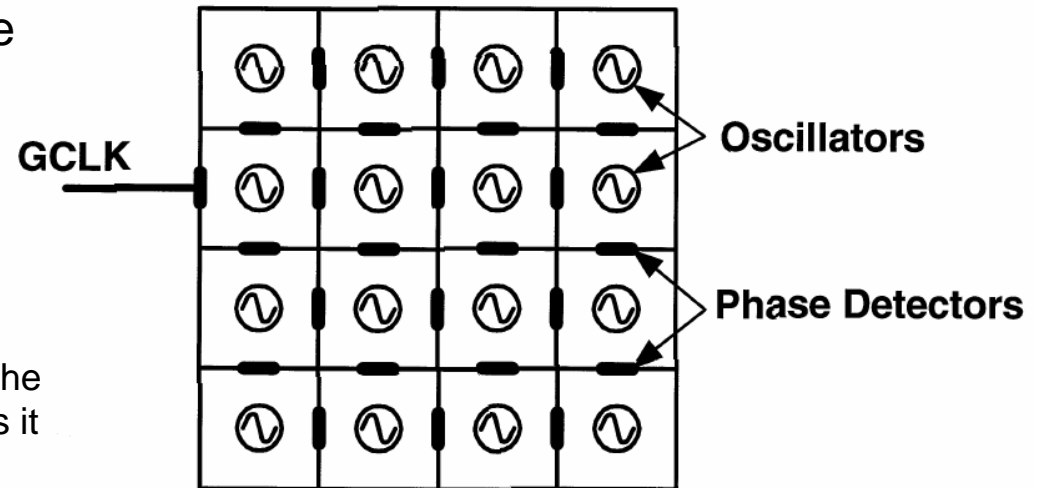
- Multiple PLLs generate clock signal
- Use phase detectors to lock the PLLs

- *Advantages*

- Coupled oscillator array reduces jitter
- Eliminates accumulated jitter above of the bandwidth of the loop filter and replaces it with the jitter of the PLL
- PLL jitter scales well with technology
- Skew is determined by mismatches in a phase detector, not by buffer mismatches

- *Disadvantages*

- Resources needed for PLLs (VCO, PD, loop filter); this is compensated by the elimination of the buffers and wiring for a global clock network
- To avoid “mode-lock”, PLLs are controlled by an analog signal that is distributed from the PD to the VCO
- Does not support DFD/DFT



V. Gutnik and A. Chandrakasan “Active GHz clock network using distributed PLLs”, ISSCC 2000

Clock frequency: 1.3GHz
Jitter: <30ps p-p (3.9%) measured

VCO Array

- **Approach:** Use a network of coupled VCOs to generate and distribute the sector clocks

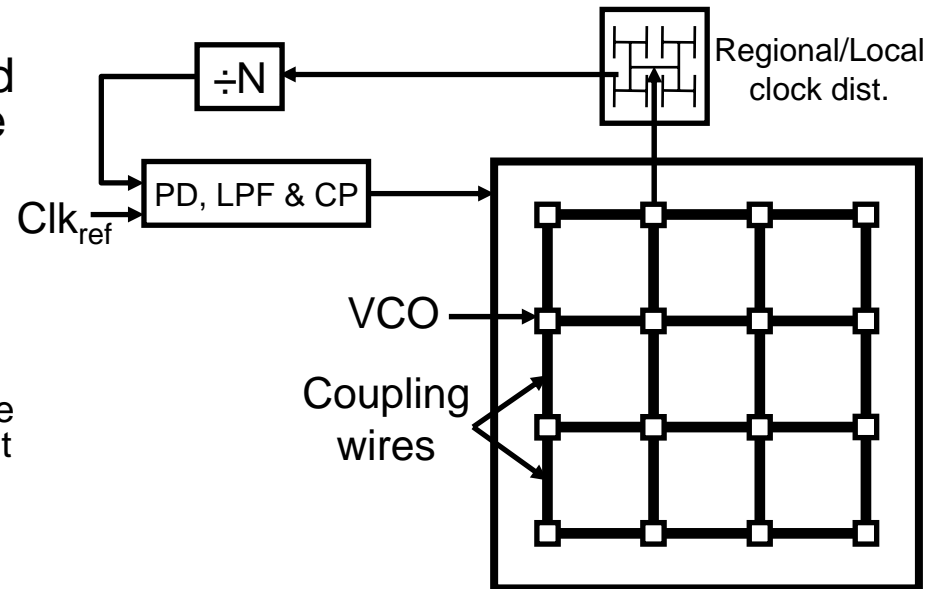
- Multiple VCOs generate clock signal
- Incorporate the VCO grid into a PLL

- **Advantages**

- Coupled oscillator array reduces jitter
- Eliminates accumulated jitter above of the bandwidth of the loop filter and replaces it with the jitter of the PLL
- VCO jitter scales well with technology
- Skew is determined by mismatches in a phase detector, not by buffer mismatches

- **Disadvantages**

- Oscillator detuning causes skew
- Does not support DFD/DFT
- Sensitive to noise on globally distributed VCO control signal



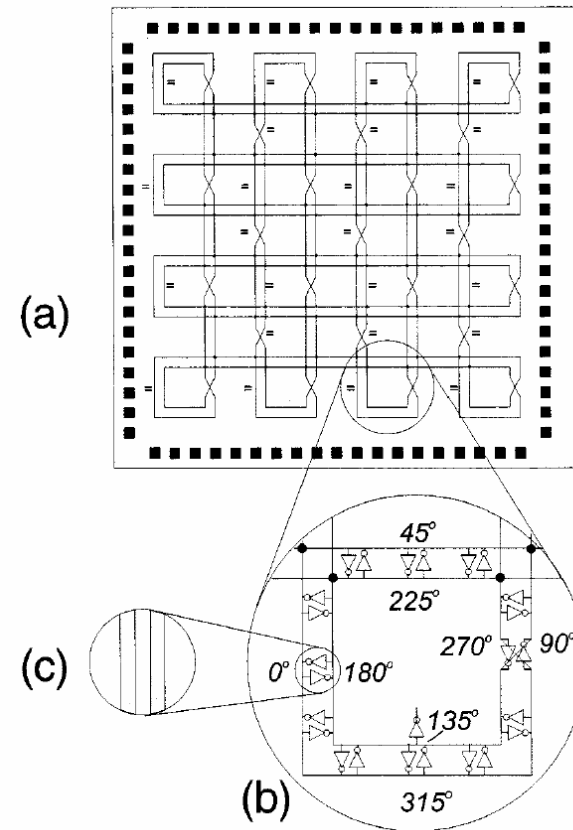
H. Mizuno and K. Ishibashi, "A noise-immune GHz-clock distribution scheme using synchronous distributed oscillators", ISSCC'00

Clock frequency: 435MHz
Skew: 17ps (0.7%) measured
Jitter: 170ps (7.4%) measured

“Rotary” oscillator array

- *Approach*: Use coupled, distributed oscillators to span a chip
 - Differential traveling waves that are in-phase oscillate around the network
 - Cross-coupled inverters “boost” the clock signal instead of regenerating it completely
 - Phase varies linearly around each loop
- *Advantages*
 - Coupled oscillator array reduces jitter
 - Clock signals naturally phase-lock at junctions between rings
 - Has the potential for low power since wave energy cycles around the ring
 - Good noise immunity since delay does not depend on inverter delay
- *Disadvantages*
 - Clock frequency is determined by on-chip dimensions and cannot be tuned
 - Does not support DFD/DFT

See also: L. Hall et.al., “Clock distribution using cooperative ring oscillators,” *Proc. Advanced Research in VLSI '97*.



J. Wood et.al. “Multi-GigaHertz low-power low-skew rotary clock scheme”, *ISSCC 2001*

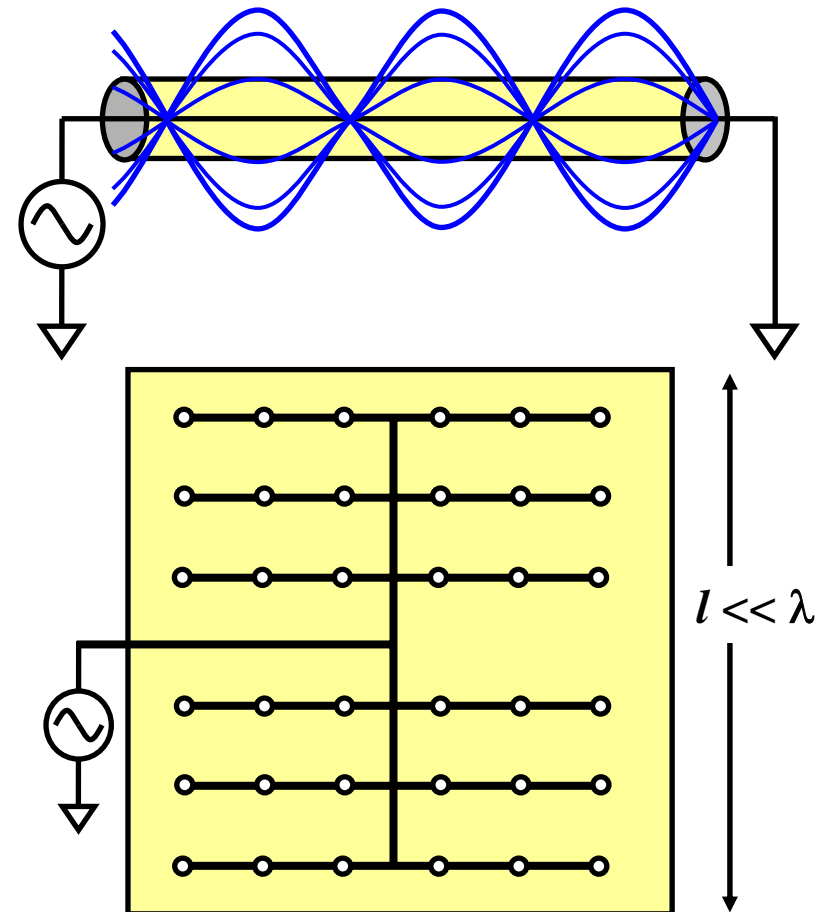
Clock frequency: 1GHz
Jitter: 5.5ps rms (5.5ps) measured

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Standing-wave (Salphasic) Clock

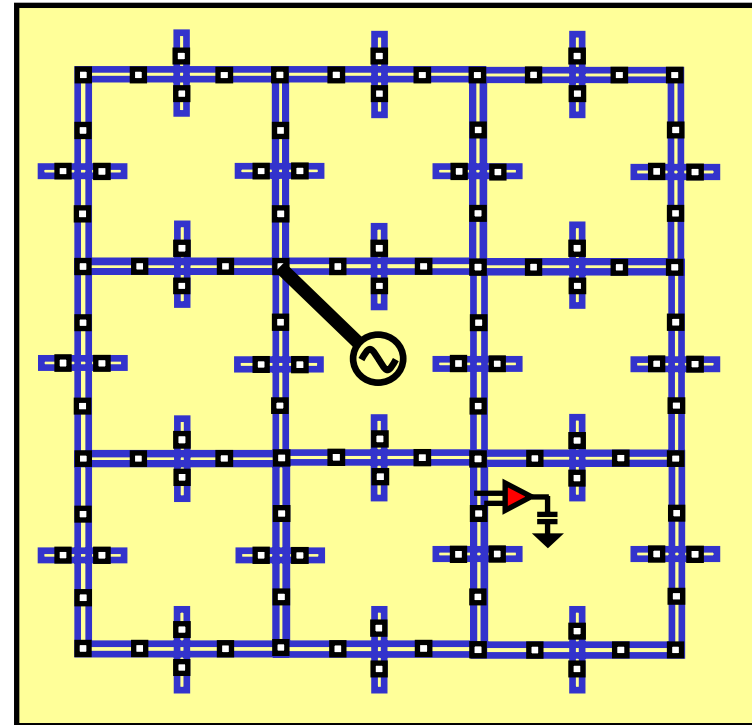
- Distribute clock as a standing wave
- *Advantages*
 - Constant phase with position
 - No dispersion effects
- *Disadvantages*
 - Amplitude varies with position
 - Performance degraded by interconnect loss
 - Requires a clock buffer (limiting amplifier) to convert from sinusoid to digital



V. Chi, "Salphasic distribution of clock signals for synchronous systems", *IEEE Trans. Comput.*, 1994.

Standing wave clock network

- **Approach:** Use coupled, distributed oscillators to span a chip
 - Differential standing waves that are in-phase oscillate around the network
 - Cross-coupled pairs “boost” the clock signal instead of regenerating it completely
- **Advantages**
 - Coupled oscillator array reduces jitter
 - Adjacent rings phase-lock to provide low local skew
 - Phase is constant around loop
 - Good noise immunity because delay does not depend on inverter delay
 - Allows injection of external clock over a limited bandwidth
- **Disadvantages**
 - Clock frequency range is determined by on-chip dimensions (but is tunable)
 - Requires a sine-to-square converter between global and sector clock trees
 - Requires nearly uniform loading
 - Does not support DFD/DFT



Clock frequency: 10GHz
Skew: 1.5ps (1.5%) measured
Jitter: 1ps rms (1%) measured
5ps p-p (5%) measured



F. O'Mahony et al., "10GHz clock distribution using coupled standing-wave oscillators", ISSCC'03.

F. O'Mahony et al., "A 10GHz global clock distribution using coupled standing-wave oscillators", JSSC'03.

Conclusions

- 1. Conventional global and regional clock distribution networks don't well.**
 - o Skew and jitter must decrease while latency, mismatch, and noise increase.
 - o On-chip wires limit clock network performance.
- 2. Jitter (not skew) will probably become the hardest specification to meet for clock networks.**
- 3. Continuing innovations to conventional techniques have extended their usefulness past 1GHz clock frequencies.**
- 4. A combination of architectural changes and more digital logic will likely extend clock distribution to 10GHz.**
- 5. The industry seems willing to explore many options before breaking the globally synchronous paradigm.**

Summary of clock networks

Global clock dist.	Product?	Clock freq. (MHz)	Dim. (mm)	Skew (% τ_{clk})	Jitter (% τ_{clk})
<i>Coupled oscillators - CROs</i>	no	53	1.4 x 1.4	n/a	n/a
<i>Standing waves (board level)</i>	no	160	19in. ^a	175ps (2.8%)	n/a
<i>Distributed VCOs</i>	no	435	7.2 ^b	17ps (0.7%)	170ps (7.4%)
<i>Coupled oscillators - Rotary</i>	no	965 ^c	3.0 x 3.0	n/a	5.5ps rms (0.5%)
<i>H-tree - Deskew & diff. signal</i>	Intel Itanium2	1200	14.1 x 18.6	52ps (6.2%)	n/a
<i>H-tree - Optimal</i>	IBM Power4	1300	20 x 20	25ps ^d (3.3%)	30ps p-p ^e (3.9%)
<i>Distributed PLLs</i>	no	1300	2.0 x 2.0	n/a	30ps p-p (1.3%)
<i>H-tree - Shorting bars</i>	Intel Pentium 4	<5000	10.2 x 10.7	n/a	n/a
<i>H-tree - On-chip LC trans. lines</i>	no	5000	10.0 x 10.0	20ps (10%)	n/a
<i>Standing waves and coupled oscillators</i>	no	10000	3.6 x 3.6 (unfolded)	2.5ps ^f (2.5%)	0.9ps rms ^g (0.9%) 5.0ps p-p (5.0%)

a. Board-level clock distribution on three 19in. equipment racks.

b. Maximum distance between VCOs on test chip.

c. A grid of four 3.4GHz rotary oscillators was also demonstrated but did not operate correctly due to layout issues.

d. Measurements reflect accumulated skew and jitter through global and regional clock distributions.

e. The PLL jitter was measured to be below 5ps, less than 17% of the total jitter.

f. For tuned grid with medium (125mV) injection amplitude. The skew for low (63mV) injection amplitude was 1.5ps.

g. Jitter added by clock network, not including the clock source which had 1.5ps rms and 10ps p-p jitter.