Signal Integrity Modeling and Simulation for IC/Package Co-Design

Ching-Chao Huang
Optimal Corp.

October 24, 2004
Why IC and package co-design?

- The same IC in different packages may not work
  - Package is the biggest discontinuity in entire channel
- Package is to be selected before IC is conceived
  - Many design parameters affect package decision

<table>
<thead>
<tr>
<th>IC</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. and assignment of I/O and P/G pads</td>
<td>Wire-bond or flip-chip</td>
</tr>
<tr>
<td>Maximum frequency and power</td>
<td>Cost vs. performance</td>
</tr>
<tr>
<td>Ri, Ci, at Input receiver</td>
<td>IR drop and ground bounce</td>
</tr>
<tr>
<td></td>
<td>RLGRC parasitics</td>
</tr>
<tr>
<td></td>
<td>Stackup, width and spacing</td>
</tr>
<tr>
<td></td>
<td>Thermal and mechanical</td>
</tr>
</tbody>
</table>
Signal Integrity Issues for IC/Package Co-Design
Issue 1: Want to optimize receiver inputs at silicon pads

- High impedance of bond wires can compensate ESD and receiver’s input capacitance and help open up eyes?

**Bond-Wire** vs. **Flip-Chip Package**
Issue 2: Want to optimize driver outputs at package pins, not silicon pads

- Need accurate package models!

Do not optimize driver outputs here.

Instead, optimize driver’s voltage swing, rise/fall time, and duty cycle here.
Issue 3: Hard to correlate measurement with simulation at silicon pads

- Rely on modeling and simulation to infer the actual received waveforms on-chip

What are the actual received waveforms here?

In actual system operation, we can only probe here.
Issue 4: Need to compensate package trace’s timing difference in PCB

- Trace routed to the corner is longer than trace routed to the edge of package

Insert extra length in PCB to adjust for timing in source-synchronous designs
Issue 5: Want to know DC IR drop from VRM to the die

- How many vias, bond wires, solder bumps, and solder balls are needed to support the IC currents?
- There are standalone, but no integrated, tools to simulate IR drop in IC, package, and PCB
  - P/G geometries are quite different in IC, package, and PCB
Methodologies and EDA Software for Signal and Power Integrity Simulation
Signal Integrity (Multi-Giga-Hertz Transmission)

- Create S-parameter models for time-domain simulations
  - Accurate over a wide bandwidth
  - Good for both design and verification
    - Insertion and return losses are key design specs.
- Flexible
  - Can perform many what-if analyses by combining or varying other component models in the channel
  - Multiple vendor tools to choose from

CAD Data
- .mcm, .brd, Gerber, ...

Optimal O-Wave
- Ansoft HFSS

S, Y, Z Parameters

Agilent ADS
- AWR Microwave Office
- Apache Nspice
- Synopsys Hspice
- Cadence Spectre RF

Time-Domain Waveforms
- Eye Diagrams, ...

Frequency Domain

Time Domain
IC and package co-design for timing closure (TSMC reference flow 5.0)

- Delay difference in package needs to be compensated on the board.

Diagram:
- Package Layout Cadence Allegro
- I/O Model RDL Parasitics
- Package Design Database
- Package RLGC Extraction Optimal PakSi-E
- SDF
- SPICE Netlists
- Static Timing Analysis
- Circuit Simulation
- Delay Time Table
- Trace Length Compensation Rules
Power Integrity (AC Ground Bounce)

- Create S-parameter models for time-domain simulations
  - Accurate over a wide bandwidth
  - Good for both design and verification
    - Identify resonant frequencies
    - Z parameters are key design specs.
- Flexible
  - Can perform many what-if analyses by combining or varying other component models in the channel
  - Multiple vendor tools to choose from

CAD Data
.mcm, .brd, Gerber, ...

Optimal PowerGrid
Sigrity PowerSI
Ansoft SIwave

S, Y, Z Parameters

Agilent ADS
AWR Microwave Office
Apache Nspice
Synopsys Hspice
Cadence Spectre RF

Frequency Domain

Time Domain

Time-Domain Waveforms
SSN, …
Meeting the Z11 design spec.

- Need to compute Z11 under various source excitations (e.g., group all solder bumps vs. excite one solder bump at a time)
- The package resonance is critical if the board is considered equi-potential.

Complex 8-layer BGA package

Assume same potential at the board.
Quantifying extraction accuracy

- Geometry is to be modeled closely in its entirety
  - Resonance depends on the shape and size of structure
  - Use triangular, not rectangular, meshes
- Have good agreements with other field solvers
  - Match 2D quasi-static solver in long narrow traces
  - Match 3D full-wave solver in simple 3D structures
- Have good correlation with measurements
  - Hard to probe the package directly with the right probes and correct open/short conditions
Power Integrity (DC IR Drop)

- Package’s DC IR drop is crucial for power integrity
  - Need voltage, current, current density distributions, and equivalent resistive networks
  - Structure is to be modeled closely by triangular, not rectangular, meshes
IC and package co-design for DC power closure (TSMC reference flow 5.0)

- IC and package extraction software provide chip and package loading for each other.
More EDA tools

- Integrated layout, extraction and simulation
  - Cadence Allgero Package Designer 620 and Allegro Package SI 620
- Direct time-domain simulation
  - CST Microwave Studio
  - Sigrity Speed2000
- Simulation framework
  - AWR Microwave Office with EM socket interface
- Links
  - Synopsys Encore + Ansoft TPA
Cadence Allegro Package Designer 620 and Allegro Package SI 620

- Simultaneous physical and electrical designs
  - LEF/DEF interface
  - Built-in 3D field solver and simulation
Summary

- Why IC/package co-design?
  - Same IC in different packages may not work
- Signal integrity issues that affect IC/package co-design
  - Want to optimize receiver inputs at silicon pads and driver outputs at package pins
  - Want to compensate package trace’s timing difference in PCB
- Methodologies and EDA software for signal and power integrity simulation
  - Using S parameters for time-domain simulation allows multiple vendor tools to choose from
  - Need to model geometries closely for accurate IR drop and ground bounce analyses
- More EDA tools
  - Cadence Allegro Package SI 620 has built-in 3D solver and allows simultaneous physical and electrical designs