High Volume Signal and Power Integrity Design for ASICs

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Agenda

- Background
- SI Methodology Outline
- SI Numerical Example
- PI Methodology Outline
- PI Numerical Example
- Summary
- Future Directions

ASIC Performance Hitting Custom Domain

- **Millions of gates**
  - Multiple MPU cores
  - Many PLLs; multiple clock domains
  - Complex multi-port memories
- **10s of W of power dissipation**
  - 100W+ on occasion
- **500MHz+ core clock rates**
  - Rapidly increasing
- **500MHz+ DDR interfaces**
  - DDR, DDR2, DDR3, custom; single-ended
  - LVDS even faster
- **6Gbps+ integrated SERDES**
- **Flipchip/wirebond; organic/ceramic packaging**
- **On-package bypass capacitors**
- **Very similar to full-custom microprocessor development of a few years ago.**

Same ASIC Business Model

- Rapid assembly of chips from modules
- Quick turnaround
- Limited custom design/involvement
- Large numbers of designs (dozens/year)

How do you support large numbers of high-performance ASICs with classic ASIC resources?

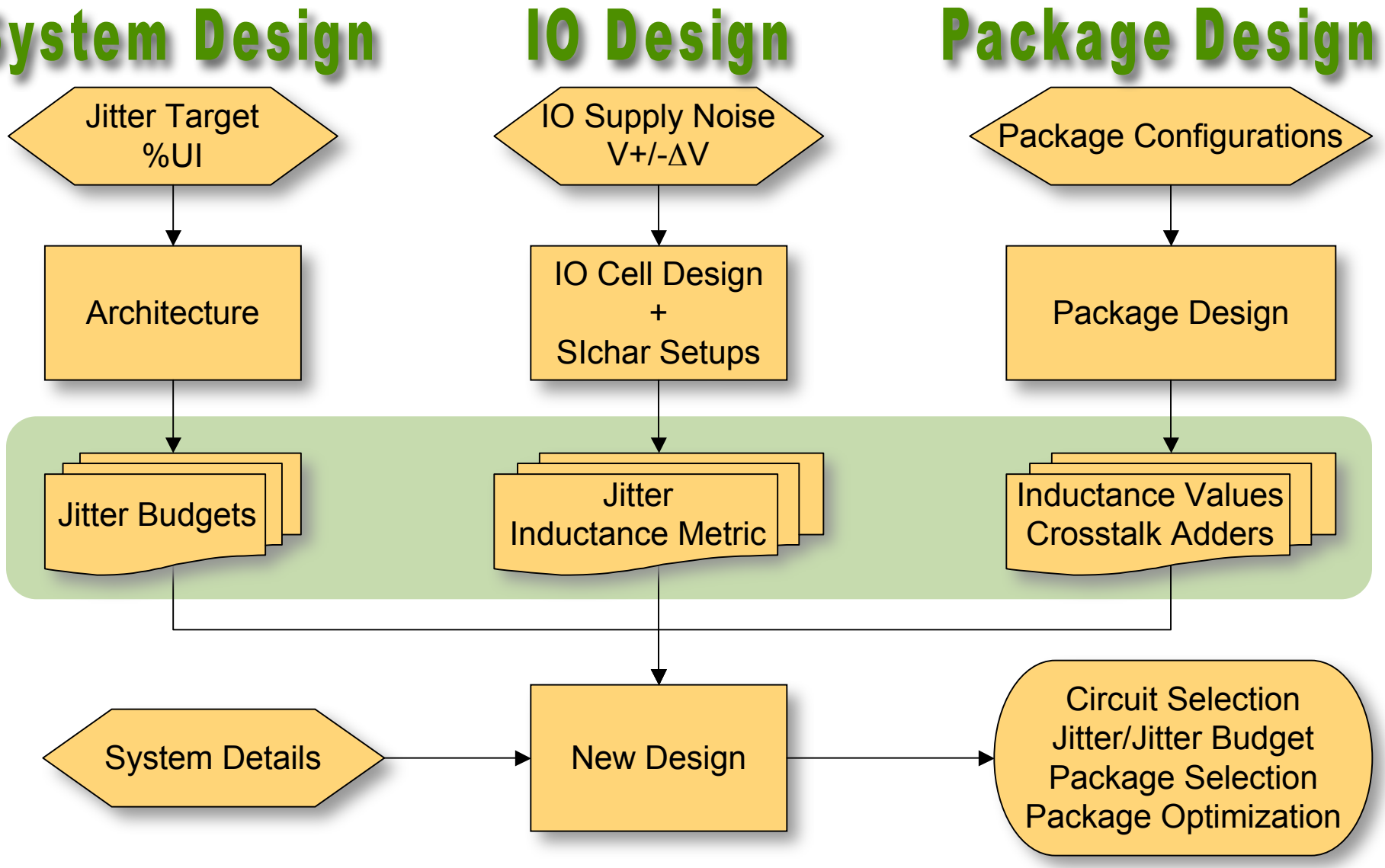
A Few Support Options

- **Staff up**
  - Extensive modeling and Spice simulation
  - Brute force approach; effective
  - Not sustainable within an ASIC business model ($$$)
- **Standardize substrates**
  - Fits with the history of ASIC with pre-characterized packages
  - Many tradeoffs involved
- **Rapid analysis capability ← *This presentation***
  - Avoid time-consuming analyses
  - Focus time on engineering decision making
  - Goal: Maintain a custom-level of optimization and support with ASIC-level staffing and time frames

High-Volume SI/PI Analyses

- **Partition the problem using cell pre-characterization and supply noise specifications**
  - Overall problem partitions into two parts
    - PI - Power Integrity Analysis
      - Verify that the assumed noise levels are achieved
    - SI - Signal Integrity Analysis
      - Look up jitter given assumed noise levels
- **Groups can work independently around the supply noise specifications**
  - Architecture definition; timing budget
    - Ex: +/-15% supply noise with 0.14UI jitter
  - IO circuit design
    - Ex: Pre-characterize jitter for 0, +/-5%, +/-10%, +/-15%
    - Pre-characterize quiet line noise vs. inductance
  - Package design
    - Pre-characterize package options for inductance
    - Pre-characterize package options for crosstalk

SI Design and Optimization

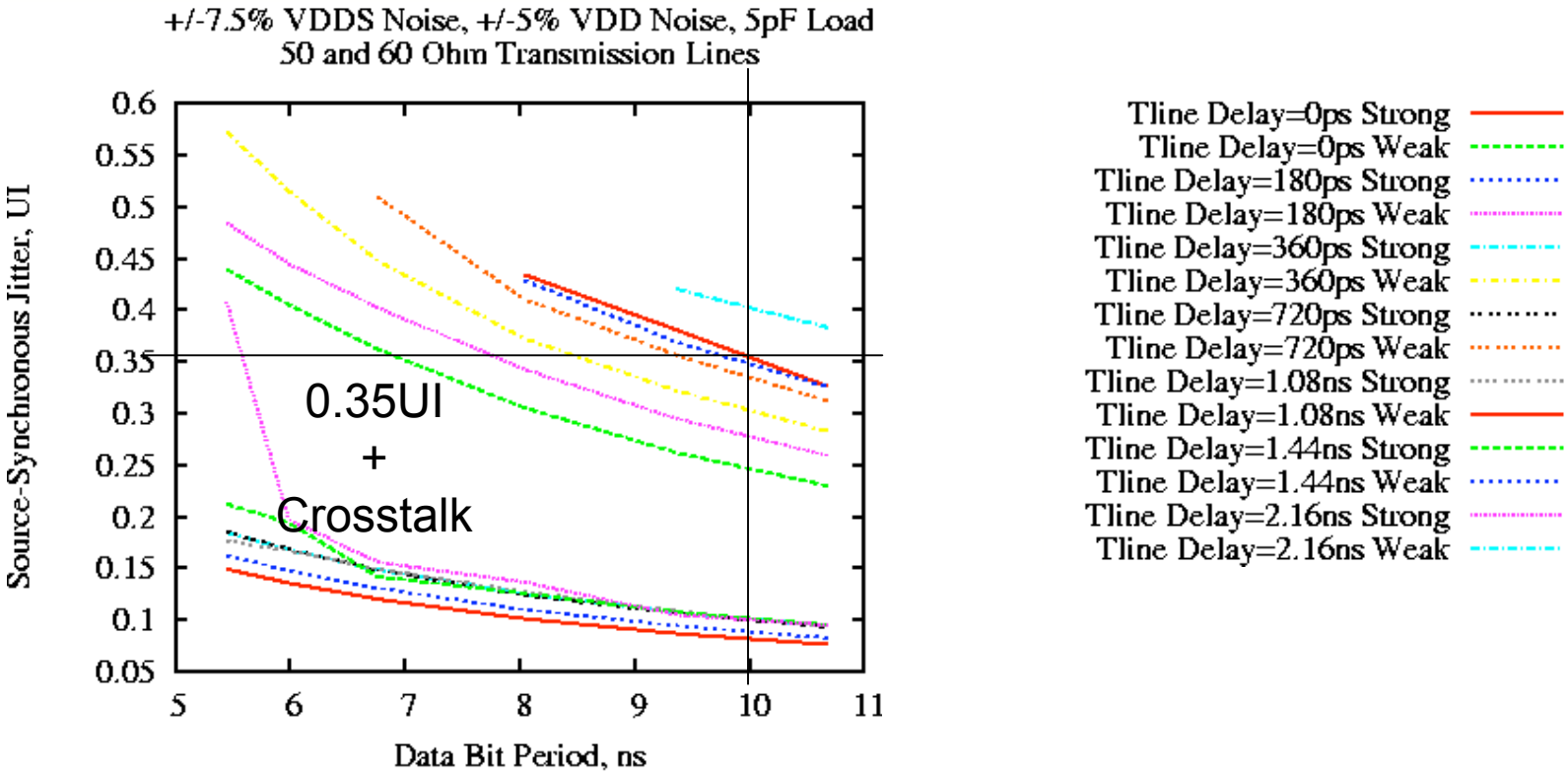


- **Benefits**
  - Speed: pre-calculated data enables look-up operation
    - minutes vs. days/weeks
    - avoid setup, complexity, runtime issues of Spice-level simulations
  - Optimization: speed enables tradeoffs
    - Check many circuits
    - Check many package styles and ratios
    - Tradeoff jitter vs. other variables
      - Package cost through signal-to-ground ratios
      - Die cost through circuit area
- **Cost**
  - Pre-calculation
    - Minimize by folding into standard cell characterization
  - Some accuracy hit

SI Numerical Example

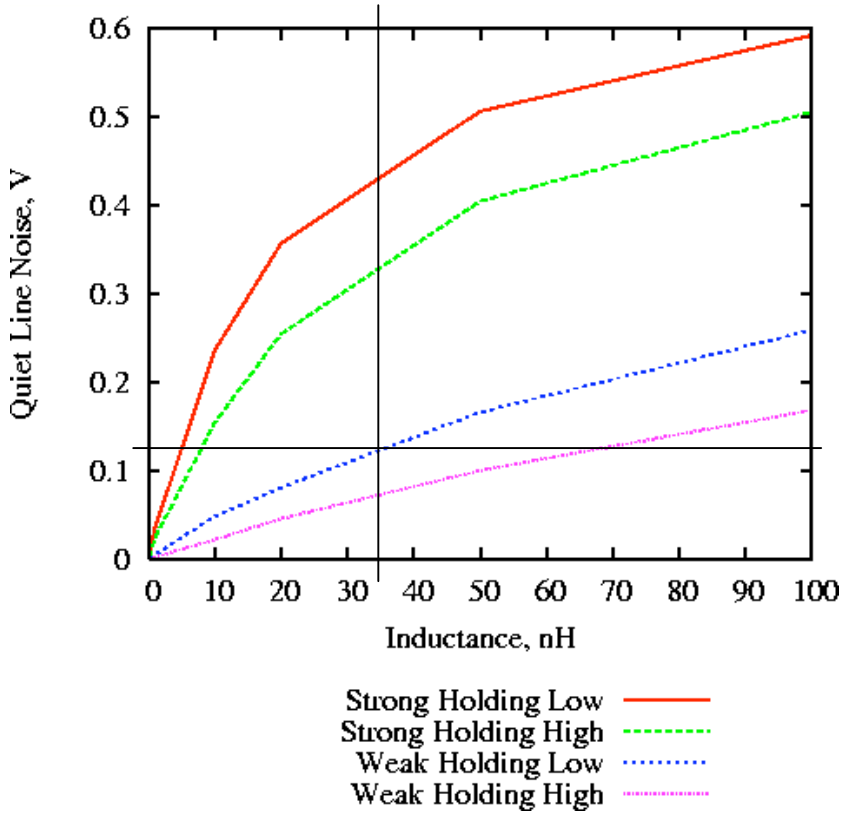
- How much DDR jitter at 50MHz is expected for a specific 1.8V LVCMOS driver for 55Ω +/- 10% unterminated nets 6” long with 5pF load?

Plot from SIchar pre-calculated data:



- **What signal to ground ratio does this buffer require to achieve the +/-7.5% supply noise target?**

Plot from SIchar pre-calculated data:



Weak (max jitter corner)
1.62V*7.5%=122mV

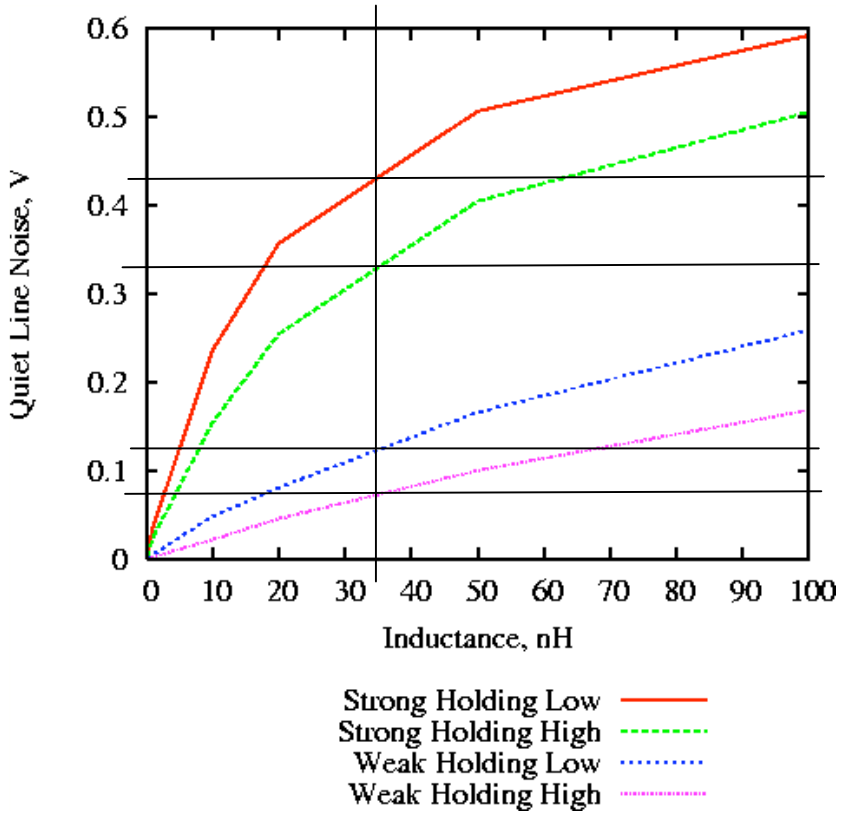
20mm Wirebond Package - Try 12:1
- 4L_PBGA_20mm_1mm_5R_14to1_5mm
- precalculated data

L=2.96nH
35nH/2.96nH=11.8

=> 12:1 works, iterate if mismatch

Note: 14 signal model to account for quiet low and quiet high lines.

• What quiet line noise is expected?



Strong Holding Low: 420mV

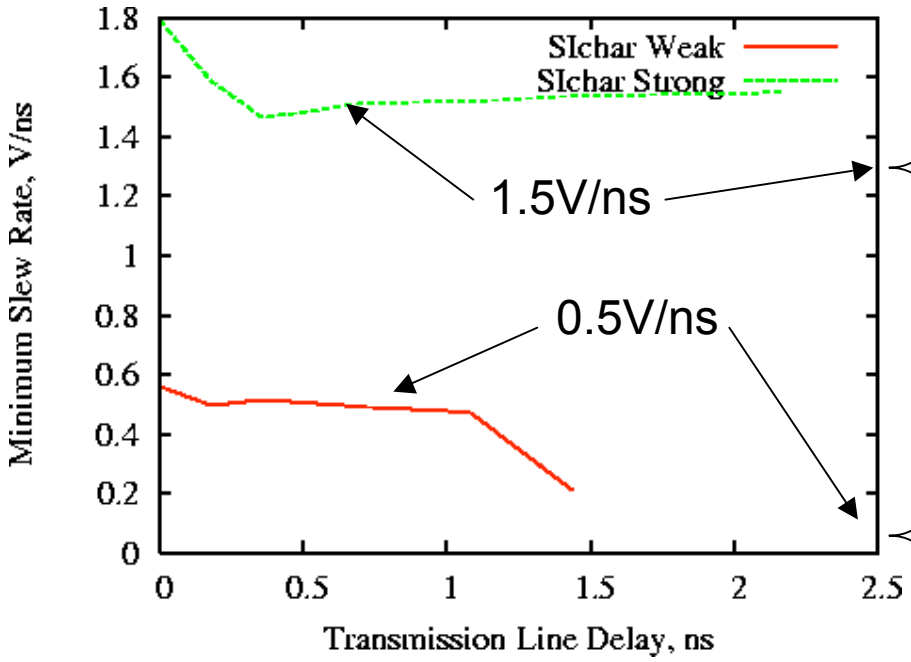
Strong Holding High: 320mV

Weak Holding Low: 120mV

Weak Holding High: 80mV

• What jitter adder is expected from crosstalk?

Plot from SIchar pre-calculated data:



From PKGchar
(4L_PBGA_20mm_1mm_5R_14to1_5mm)

Data available at 0.5ns (2V/ns), look up:
FE xtalk=134mV

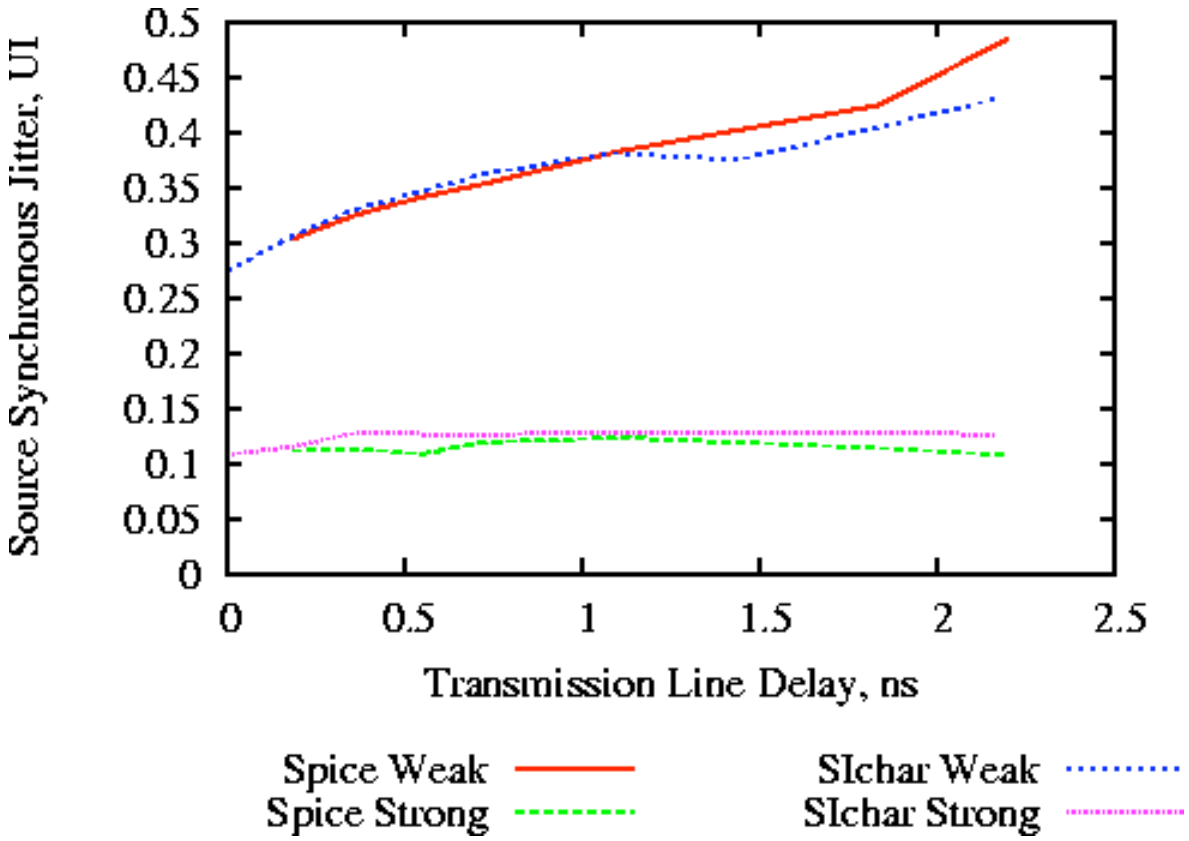
Calculate Adder:
0.5ns/V*134mV*4=268ps=0.0268UI
Total Jitter = 0.1+0.0268=0.127UI

Data available at 2ns (0.5V/ns), look up:
FE xtalk=35mV

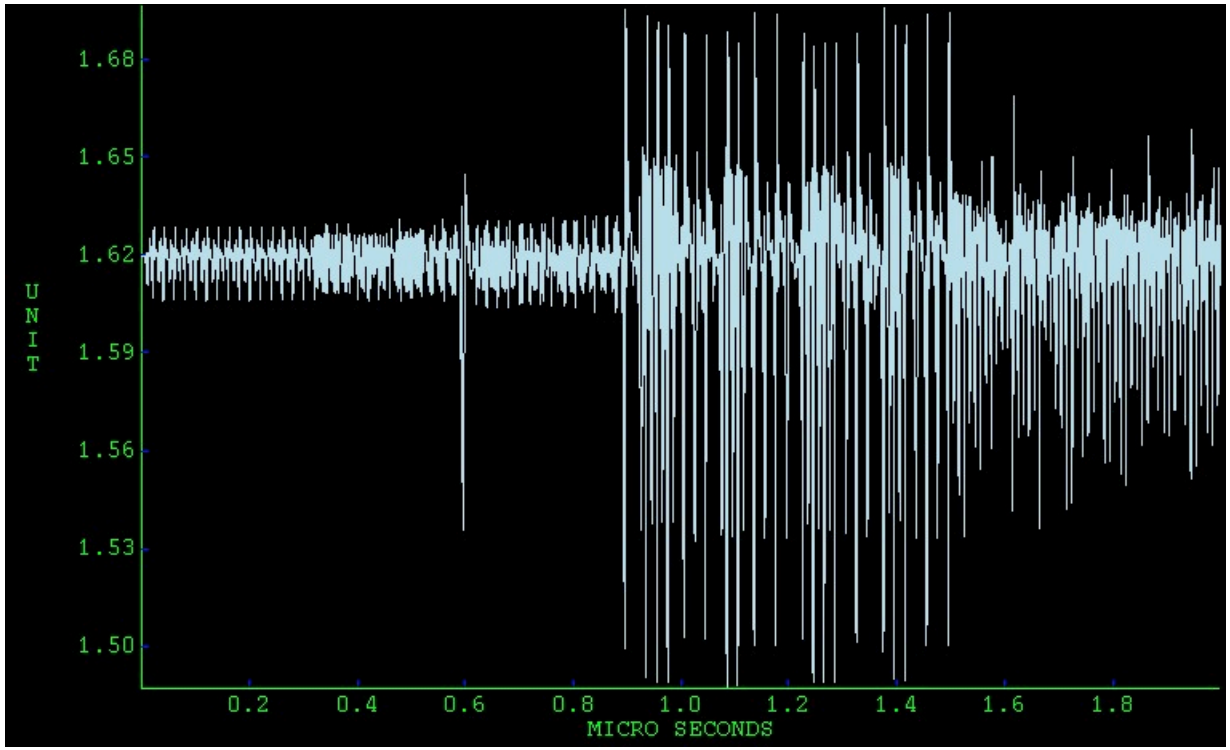
Calculate Adder:
2ns/V*35mV*4=280ps=0.028UI
Total Jitter = 0.35+0.028=0.378UI

- **Summary of predictions**
  - Source-synchronous jitter: 0.38UI (weak), 0.13UI (strong)
    - +/-7.5% VDDS noise
  - Signal-to-ground ratio: 12:1
  - Quiet Line Noise:
    - Strong holding low: 420mV
    - Strong holding high: 320mV
    - Weak holding low: 120mV
    - Weak holding high: 80mV

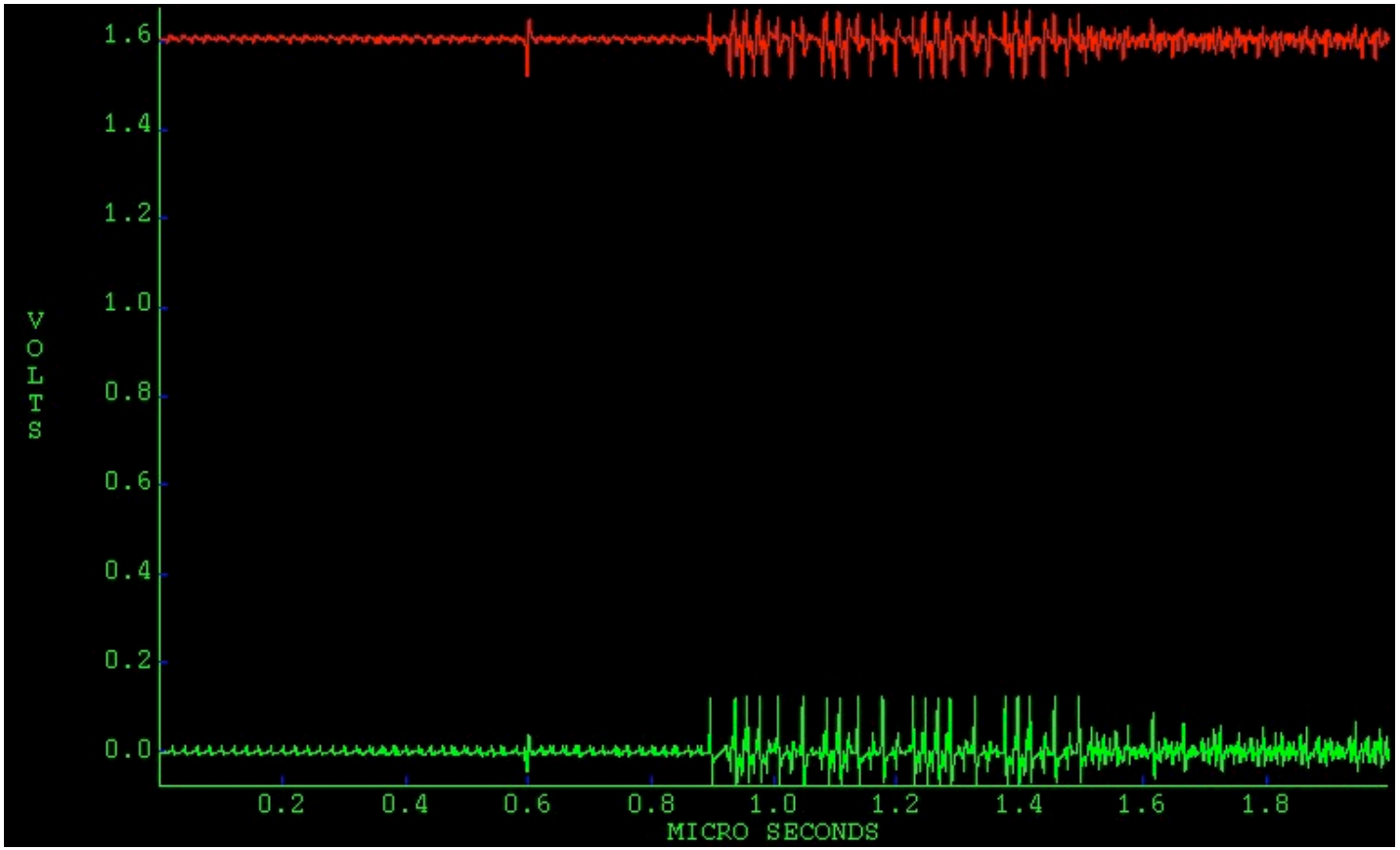
- **Full Spice-based SSO Simulation Results**



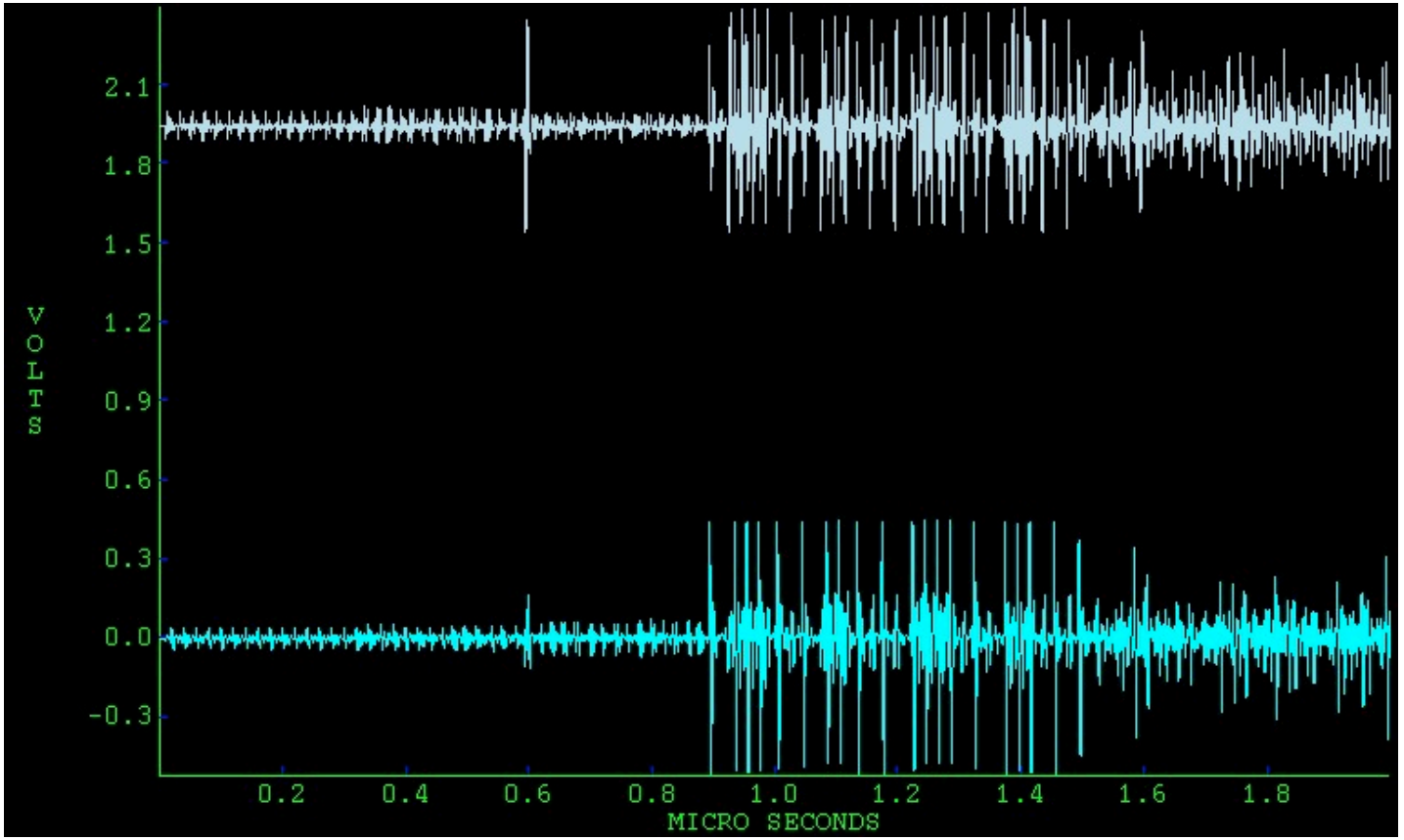
- **Supply Noise - 132mV of collapse, or 8.1%**
  - SIchar run at 7.5%



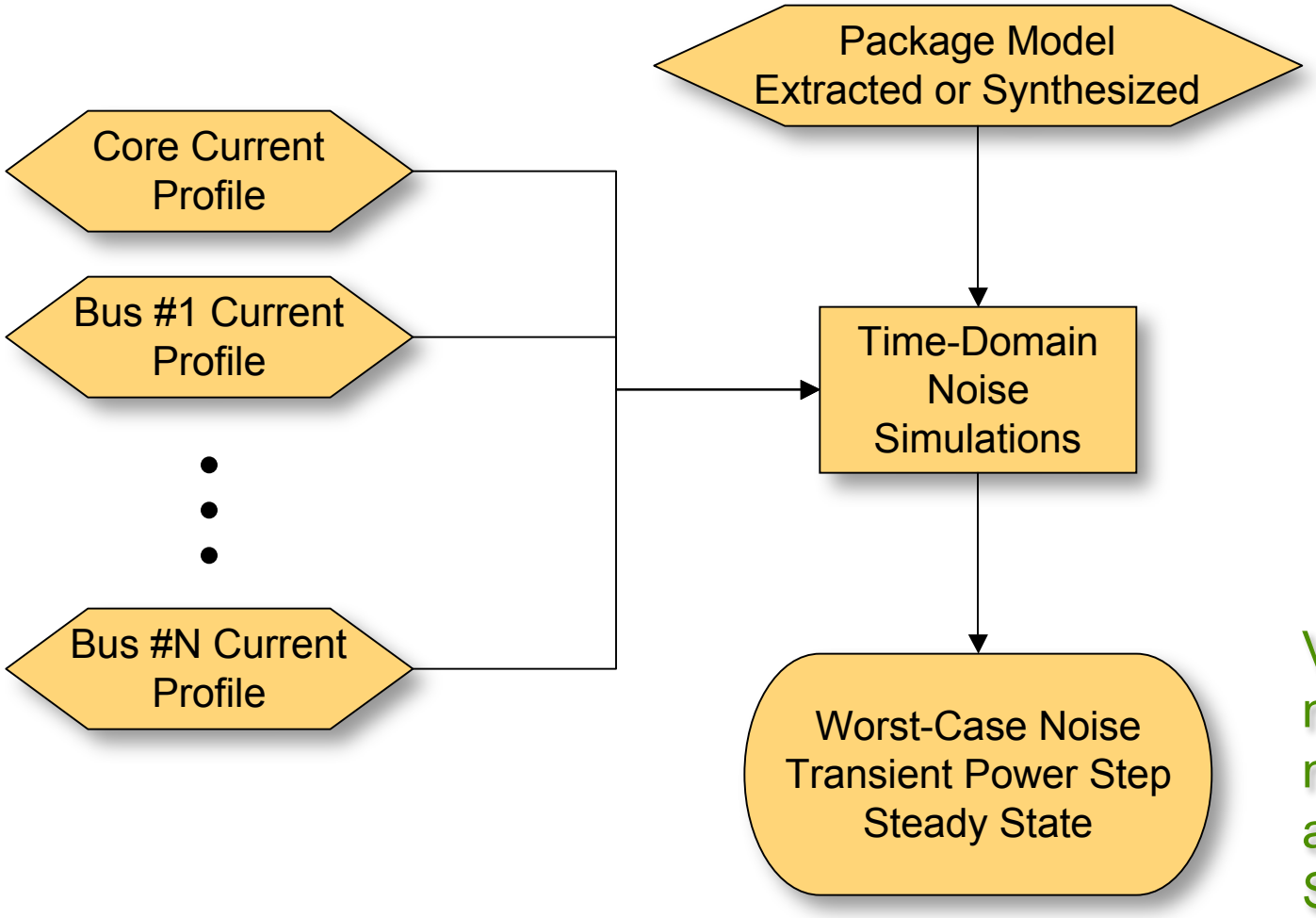
- Weak Quiet Low: 127mV (SIchar: 120mV)
- Weak Quiet High: 92mV (SIchar: 80mV)



- Strong holding low: 451mV (SIchar 420mV)
- Strong holding high: 408mV (SIchar 320mV)



PI Design and Optimization



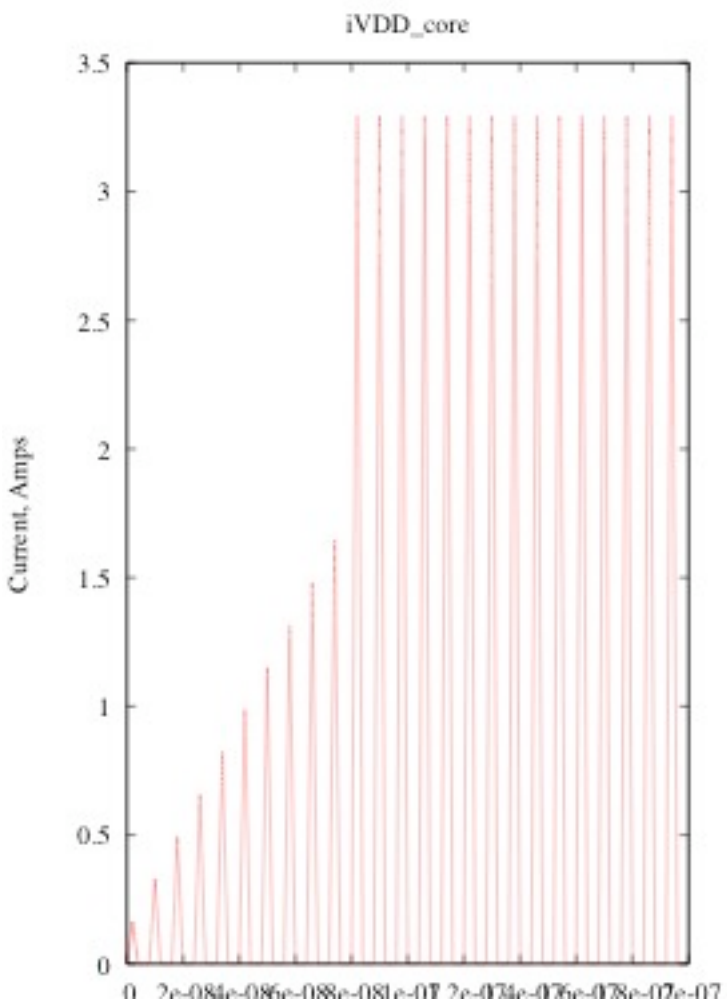
Verify that the noise levels meet those assumed in the SI analysis.

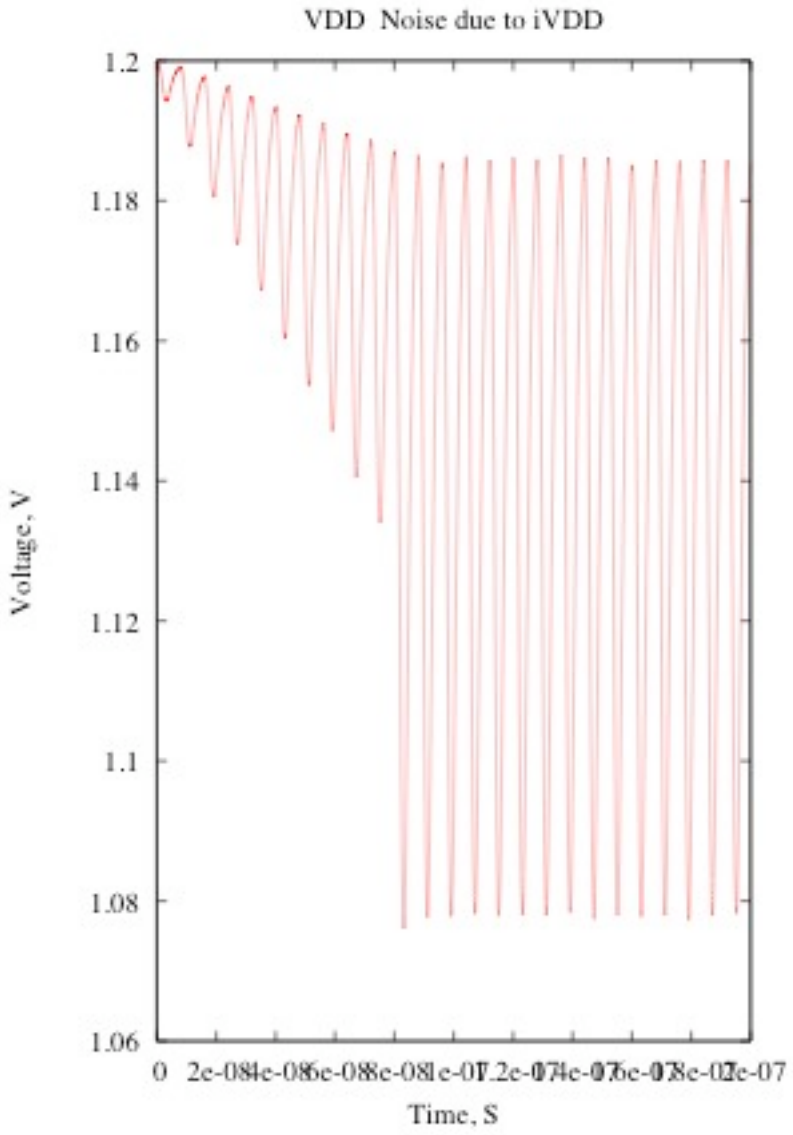
- **Benefit**
  - Fast simulation time due to use of current profiles
  - Full device simulation
    - Captures crosstalk from supply-to-supply
- **Cost**
  - Best accuracy for digital supplies requires current profiles pulled from an SSO simulation
    - Captures the feedback effect between voltage and current draw

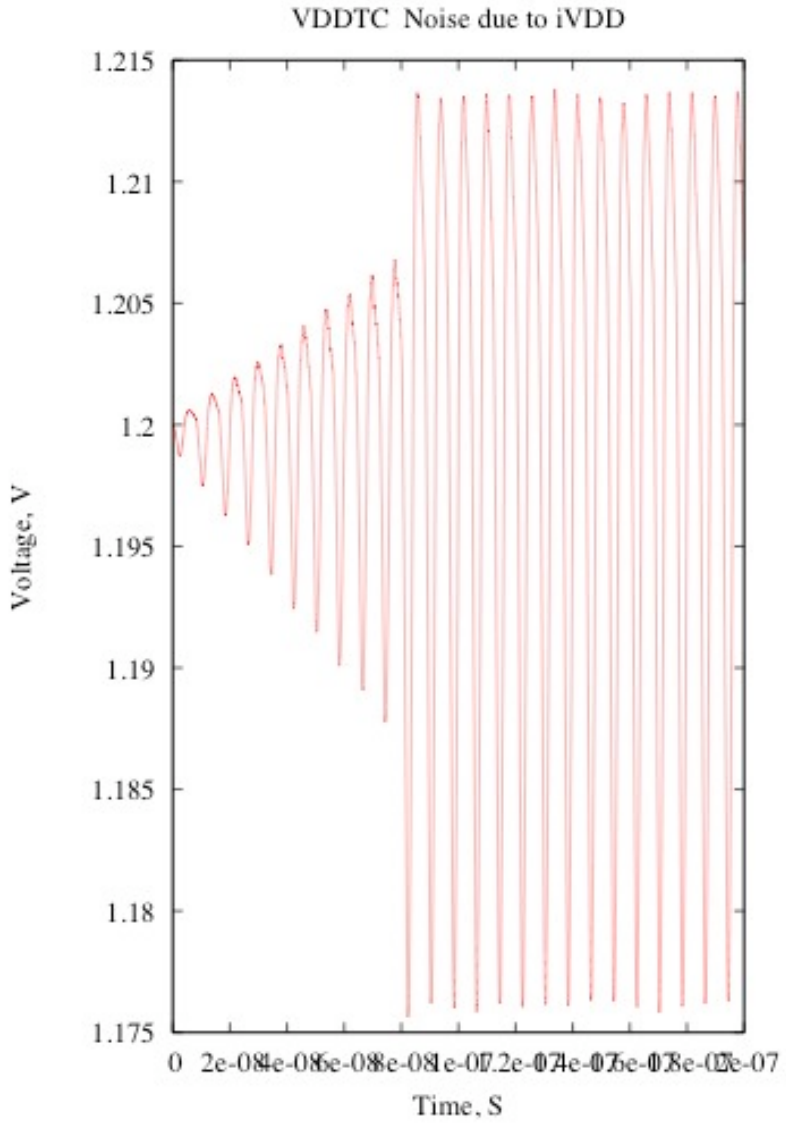
PI Numerical Example

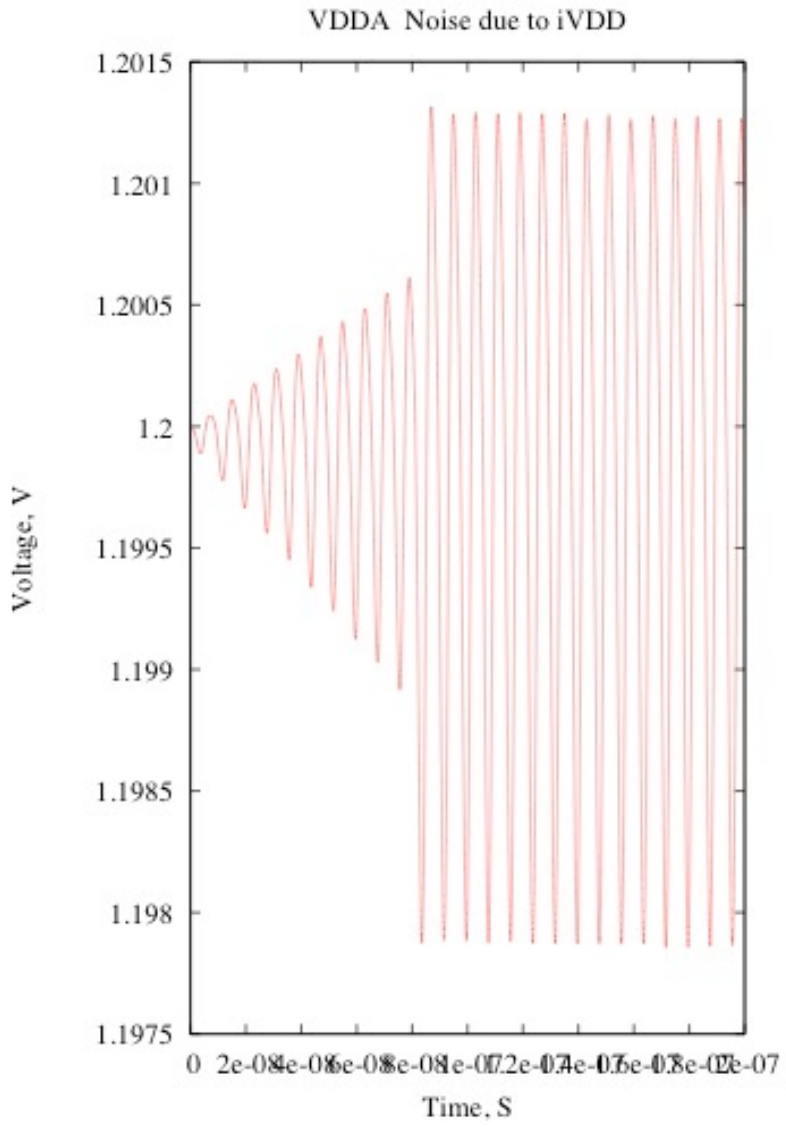
- 125MHz 7.9W ASIC with integrated Serdes
- 3 supplies
  - VDD (core)
  - VDDTC and VDDA (Serdes)
- Time-domain simulation results:

Supply	Package Noise Component (mV),%			Total (mV),%
	iVDDTC	iVDD	iVDDA	
vVDDTC	+60.0/-17.1 + 5.0/-1.4	+13.7/-24.4 + 1.1/-2.0	+ 0.7/-1.0 + 0.1/-0.1	+74.4/-42.5 + 6.2/-3.5
vVDD	+-0.0/-0.2 +-0.0/-0.0	+60.0/-63.9 + 5.0/-5.3	+-0.0/-0.1 +-0.0/-0.0	+60.0/-64.3 + 5.0/-5.4
vVDDA	+-0.0/-0.2 +-0.0/-0.0	+ 1.3/-2.1 + 0.1/-0.2	+60.0/-16.8 + 5.0/-1.4	+61.3/-19.1 + 5.1/-1.6


iVDD_core
Current, Amps
3.5
3
2.5
2
1.5
1
0.5
0


VDD Noise due to iVDD
Voltage, V
1.2
1.18
1.16
1.14
1.12
1.1
1.08
1.06
0
Time, S


VDDTC Noise due to iVDD
Voltage, V
1.215
1.21
1.205
1.2
1.195
1.19
1.185
1.18
1.175
0
2e-08
4e-08
6e-08
8e-08
1e-07
2e-07
4e-07
6e-07
8e-07
1e-06
2e-06
Time, S


VDDA Noise due to iVDD
Voltage, V
1.2015
1.201
1.2005
1.2
1.1995
1.199
1.1985
1.198
1.1975
0
2e-08
4e-08
6e-08
8e-08
1e-07
2e-07
4e-07
6e-07
8e-07
1e-06
2e-06
Time, S

Summary

- Pre-characterization of drivers enables lookup calculation of jitter and quiet line noise
  - Run for a range of supply noise levels
  - Run for a range of signaling environments
  - Characterize an inductance metric
- Assume a target level of supply noise
- Look up the jitter; compare to jitter spec
- Assume a level of quiet line noise
- Look up the needed inductance
- Pick or design the package to provide the needed inductance
- Verify noise levels with power integrity analysis

Future Directions

- Pre-characterization of drivers for signal integrity performance and package needs
- Look-up jitter and noise estimates; look-up package selection and optimization
- Rapid tradeoff of circuit and package performance
- Full-chip power integrity analysis with power supply crosstalk noise included