Characterizing and Managing Variability in Microprocessor Chips

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Acknowledgements

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References:
1. Manjul Bhushan, Anne Gattiker, Mark B. Ketchen, and K.K. Das
2. Manjul Bhushan, Mark B. Ketchen, Stas Polonsky and Anne Gattiker
   Proceedings of 2006 ICMTS
3. Mark B. Ketchen and Manjul Bhushan
Outline

- Source of Variability and Impact
- Measuring Variability
  - Process Induced
  - Design Induced
- Managing Variability
- Summary
Variability - Challenges

Characterization Goal: Reduce impact of variability on microprocessor performance, power and yield
Sources of Variability (CMOS Technology)

- Fundamental Random Variations
  - Dopant fluctuations induced Vt variations
  - Line edge roughness

- Systematic CMOS process induced variations
  - Across chip, across reticle, across wafer, wafer-to-wafer and lot-to-lot
  - Across circuit topology & metal wire R & C

- Time dependent variations, short term (10^{-9} s - 10^{-3} s)
  - SOI Floating body induced variations
  - Power supply transients

- Time dependent variations, long term (10^{8} s)
  - NBTI, hot-electron, electromigration
Sources of Variability (Package/Design)

- Chip integration induced variation
  - Power supply distribution
  - Hotspots

- Package/module induced variations
  - IR Drops
  - Temperature gradients

- Design tool induced variations
  - Hardware to parasitic and wire models
  - Hardware to BSIM model
  - BSIM model to piecewise linear model
Is Variability an Issue?

- Reduced yield for high performance parts
- SRAM yield – read/write fails
- Analog circuits – functionality, out of specifications
Characterizing Variability

- Product representative test structures
  - on chip placement for ongoing evaluation
  - design tools based target parameters
  - experimental designs to minimize ambiguity

- Ease of data collection, development and manufacturing

- Techniques for effective data analysis

- Rapid feedback to CMOS process and design teams
“At Speed” Test Structures

- Strategic placement
- Ring oscillator and pulse based
- Differential measurements/analysis
- DC I/O’s for ease of measurement
- Circuit delays directly relate to process/device parameters

μP μP

Scribe line

High Speed
Circuits

Set / Reset Inputs
Analog Inputs for Tuning
Enable / Launch
Low Frequency / DC Output
Digital Inputs for Decoders
GND VDD’s
Variability in Circuit Performance

- Process induced systematic variations
  - Across chip
  - Across circuit topologies / layout Styles

- Random variations in closely spaced identical circuits, arising from variations in Vt, Line width (Lpoly), Tox ..

Test Structures for rapid measurements of product representative identical ckt. delays to obtain underlying parametric variations
Across Chip Variation
Multiple Identical Ring Oscillators

• Placement of identical ring oscillators on a grid

• > 50 stages/ring to remove impact of random variations in MOSFET parameters

• Measurement (w & w/o clock) for CMOS performance variations vs. power supply and temperature variations

• Correlation of ring and chip frequency by location
Delay Variation Across Chip

- Higher IDDQ for constant Fmax
- Fmax variation across wafer
Across Circuit Type/Process Variability

- Expected correlation
Ring Oscillator Stage Designs
Differencing Schemes

(a) Reference Stage
(b) Capacitance Load - C
c
Rw
Cw

(c) Wire Load - RC
(d) MOSFET Load - R

Cg

NPG
Design of a 32 Ring Oscillator Macro

8 RO's

Decoder

OUT

Frequency Divider and I/O Driver

2.5 mm
Average Current from RO Delay/Stage

Inverter Stage

\[ R_{sw} = \frac{D}{Cs} \]

NAND3 Stage

Inverter + N_passgate Stage
“At Speed” Test Structure for Vt Variations

**Diagram:**
- ENABLE
- CLOCK RO
- Divide by m
- Counter
- Decoder
- Array RO’s
- MUX
- F_OUT
- Frequency Modulated Output

**Graph:**
- Time
- 8T
- Oct 22, 2006
- FDIP-06
Extraction of Vt Variations from Circuit Delays

Simulated % Change in RO Freq. vs. Vdd
\( \delta Vt = +/- 40 \text{ mV}, \delta Lp = +/- 12\% \)

![Diagram of RO Stage with NFET Passgate and Inverter](image)

- RO Stage
- NFET Passgate
- Inverter
Temporal Variability – SOI History Effect

Primary Delay Chain  1SW Delay > 2SW Delay

IN  Stg  Stg  Stg  Stg  Stg  OUT

12  12  9  9  12  12

9  12  9  12

Wi  Wafer  Wo
Variability introduced by Chip Timing Tools

- Simulated circuit delays vary with parasitic models
- Model assumptions to reduce simulation time add to inaccuracies in timing

Example: Circuit delay w & w/o node-to-node coupling capacitance
Multiple Vt MOSFETs – Inverter FO3

- IDDQ vs. Delay for two different Vt’s
- Shifts in relative Vt centering in the hardware may merge the distributions

Vdd=0.8V

Vt1

Vt2

Ckt Delay

Vdd =1.0V

Vt1

Vt2

Ckt Delay
Multiple Vt’s, Critical Path Example

Leakage Power (IDDQ) /Performance Trade-off varies with mixed Vt gates and Vt centering in the Hardware

Path composition
All Gates Vt1
All Gates Vt2
Mixed Gates Vt1/Vt2
Mixed Gates (Vt1+30mV)/Vt2
Summary

- Characterization of variability on an on-going basis is key to its minimization and accommodation in design.

- “At Speed” test structures for variability characterization aid in technology development and manufacturing.

- Judicious composition of device menu and restrictive designs reduce the impact of variability.