Signal Integrity Design of TSV-Based 3D IC

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1) Driving Forces of TSV based 3D IC
2) Signal Integrity Issues
3) Noise Coupling Issues
4) Noise Isolation Methods
5) Conclusion
TSV Based 3D IC

Chip

Silicon Interposer

Package

PCB
Major Advantages of TSV-based 3D IC

- Large interconnection density
- Small for factor
- High performance: high-bandwidth, high I/O counts
- Low power
- Potentially low cost
**Key Technology for 3D IC: TSV (Through Silicon Via)**

- Short Interconnection Length
  - Reduced Delays
  - Low Impedance for PDN
  - Low Power Consumption
  - Heat Dissipation Through Via

- Less Space for Interconnection
  - High Density Chip Wiring
  - Large Number of I/O
  - Small Area Package
High-frequency Channel Loss in TSV

S21 (magnitude) [dB]

Frequency [GHz]

SiO₂ Ta Cu

0.1 μm

1 μm

Acc. V Spat. Mag. Def. WD 10.0 kV 2.0 20000x SE 11.2
Frequency-dependent Loss of Through Silicon Via

![Diagram of Frequency-dependent Loss of Through Silicon Via]

- **Frequency dependent term**
- **Leakage current**
- **Loss term**
- **Insertion loss (dB)**
- **Frequency (GHz)**

- Capacitive region
- Resistive region

- $C_{\text{insulator}}$, $G_{\text{Si sub}}$
TSV Channel Loss with Various Insulator Thickness of TSV

Signal Top

Ground Top

Signal Bottom

Ground Bottom

\( \text{Leakage current} \)

\( \text{Insulator thickness of TSV} \downarrow \)

\( C_{\text{Insulator}} = 1.6 \text{ pF} \)

\( C_{\text{Insulator}} = 2.6 \text{ pF} \)

\( C_{\text{Insulator}} = 7.8 \text{ pF} \)

\( [A] \)

\( \text{Frequency (GHz)} \)

\( \text{S21 magnitude (dB)} \)

( \( t = 0.5\text{um} \) )

( \( t = 0.3\text{um} \) )

( \( t = 0.1\text{um} \) )
The Proposed TSV Equalizer using an Ohmic Contact

Ohmic contact (Al/n+ type)

n+ high doped Silicon

Signal TSV

Ground TSV

n-type Silicon Substrate
Insertion loss of 8 TSVs with TSV equalizer

-4.8 dB

-3.8 dB

0 dB

Insertion loss of 8 TSVs without TSV equalizer

1 dB

0.7 dB

Frequency (GHz)

Insertion loss (dB)
Eye opening by the TSV Equalizer

Time (ps) vs. Voltage (V) graph showing before and after equalization.

- Before equalization:
  - Eye opening: 10 mV
  - Pk-pk jitter: 10 ps

- After equalization:
  - Eye opening: improved
  - Pk-pk jitter: reduced
High speed channel loss by TSV

- High frequency loss
- Non uniform loss
- Loss increases as higher die stack and TSV numbers
- Passive and active equalization methods needed
Noise Coupling Paths in Stacked Dies using TSV

1. TSV to TSV Coupling
2. TSV to Active Circuit Coupling
3. Metal to Metal Coupling
Coupling between TSVs

![Diagram of coupling between TSVs]

Coupling coefficient [dB] vs. Freq [GHz]

- Measurement
- Model

Cox

Gsi

Csi + C_{parasitics}
Noise Coupling from TSV to Active Circuits

Distance between contact and TSV: 100 μm
Substrate height: 100 μm
TSV diameter: 30 μm
TSV SiO₂ thickness: 0.5 μm

Silicon resistance dominant
TSV SiO₂ capacitance dominant
Silicon capacitance dominant

Frequency [GHz]
Coupling coefficient [dB]
Shielding Methods for TSV Coupling
Shielding Effect Measurement: Guard Ring

![Graph showing coupling coefficient vs. frequency for w/o and w/ guard ring. The graph illustrates a significant improvement in shielding effect with the inclusion of a guard ring.]
Shielding Methods for TSV Coupling
Crosstalk between TSV

- High frequency coupling
- Dependent on TVS designs: dimensions and materials
- Proper shielding methods are needed
- Shielding structures can be significant overhead of chip area
- Special I/O scheme may be needed to compensate or to avoid the crosstalk effects
Vertical Noise Coupling Issues in Mixed-Signal 3D-IC

- Only tens µm distance: Tight near-field coupling and conductive coupling
- ~hundreds µm: Interconnection Inductor
- ~tens µm: Digital Logic Chip Substrate, RF/Analog Block Substrate
- N-Well, N+, P+, Guard ring, Clock Tree, Interconnection, Transmitter, Receiver, Inductor, Interconnection, Substrate, TSV, RF/Analog Chip Substrate, Digital Logic Chip Substrate

Terahertz Interconnection and Package Laboratory
3D IC for 2.4GHz VCO in Zigbee module

Noise Source at Port #1: DDR 3 Clock

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rising/Falling Time (T_r/T_f)</td>
<td>35ps</td>
</tr>
<tr>
<td>Operation Frequency (1/T_D)</td>
<td>800MHz (1.25ns)</td>
</tr>
<tr>
<td>V peak</td>
<td>1.5V</td>
</tr>
</tbody>
</table>

Spur. & Phase noise at VCO output
Impact of Vertical Coupling on VCO Output Spur.

Vertical coupling causes Spur. Mask Violation!
Solutions to Reduce Vertical Coupling in Mixed-Signal 3D-IC

- Mesh shield using back-side re-distribution layer (RDL)
- Magnetic material shielding
- Dedicated chip for on-chip decoupling cap
- or re-distribution layer

Additional chip:
- For dedicated power/ground with on-chip de-cap.
- For re-distribution layer
Vertical Coupling from On-Chip DC-DC Converter to LNA

200MHz, Duty 0.5 Clock at DC-DC Converter Driver

Off-Chip Port: LNA Output; Out +

Off-Chip Port: LNA Output; Out -

On-Chip Port: DC-DC Converter Output; VDD_out

LNA chip

Epoxy

50μm/100μm

20μm

On-chip DC-DC Converter Chip

PCB
Inductive and Capacitive Coupling Model

Simplified Model of On-Chip DC-DC Converter

\[ L_M = 600\, \text{pH} \]
\[ C_C = 60\, \text{fF} \]

Simplified Model of LNA

\[ VDD \]
\[ \text{On-chip} \]
\[ \text{Out} \]
\[ 50\, \Omega \]
Measurement of Vertical Coupling

![Graph showing coupled noise at LNA output vs time from triggered point. The graph displays two traces: red for LNA Out+ and blue for LNA Out-. A peak at 5ns with a labeled frequency of 200MHz is noticeable.]

- **LNA Out+**
- **LNA Out-**

**DUT 1-50μm**

Coupled Noise at LNA output(mV)

Time from Triggered point(ns)
SSN Sensitive Circuits in IC

- VCO: Voltage Controlled Oscillator
- PLL: Phase Locked Loop
- ADC: Analog to Digital Converter
- DAC: Digital to Analog Converter
- LNA: Low Noise Amplifier
- RF Mixers
Hierarchical PDN in 3D IC

Chip

Silicon Interposer

Package

PCB

ADC, DAC

RF

Analog

Inductor

NMOS Cap

n-well

p+

p+

GPU

ground

power

TERA

KAIST

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**PDN Impedance Curves in 3D IC**

![PDN Impedance Curves in 3D IC](image)

<table>
<thead>
<tr>
<th>Figure</th>
<th>Peak (region V)</th>
<th>Mode number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig. 3-(a)</td>
<td>a, b, d, f</td>
<td>(1,0), (2,0), (3,0), (4,0)/(0,1) - Mode @ DRAM</td>
</tr>
<tr>
<td></td>
<td>c, e</td>
<td>(2,1), (3,1) - Mode @ Interposer</td>
</tr>
</tbody>
</table>

**Legend:**
- @ 3rd stacked DRAM
- @ 2nd stacked DRAM
- @ 1st stacked DRAM

**Equation:**
\[ Z_{\text{target}} = 0.21 \, \Omega \]
PDN Impedance of 3D IC with On-chip Decoupling Capacitors

Frequency (GHz)

PDN Impedance ($Z_{11}$) ($\Omega$)

$Z_{\text{target}} = 0.21 \, \Omega$

@ 3$^{\text{rd}}$ stacked DRAM

- Gray: No on-chip decap
- Black: On-chip decap (15.3nF)
- Dot-dashed: On-chip decap (30.6nF)
- Dotted: On-chip decap (45.9nF)
Lowering PDN impedance in TSV based 3D IC

- On-chip and Off-chip decoupling capacitors
- Lower inductance TSV,
- Higher number of TSV
- Lower inductance of PDN interconnections in RDL, on-chip, and interposer
- Lower resistance of PDN interconnections in RDL, on-chip, and interposer
SSN Noise Coupling Paths

- On-chip and Off-chip PDN
- Si substrate
- Interposer substrate
- RDL patterns
- TSV
- Coupling
Clock Jitter Due to the SSN Coupling

- **w/o PDN Noise**
- **100MHz PDN Noise**
- **800MHz PDN Noise**
- **1GHz PDN Noise**

- 1.45 ps
- 321.4 ps
- 33 ps
- 2.3 ps

Duty Cycle Distortion

PDN Noise

w/o PDN Noise

100MHz PDN Noise

800MHz PDN Noise

1GHz PDN Noise

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Noise level : 100 mV
Input Clock Frequency of DLL = 1 GHz

Jitter w/o and w PDN Models

- Voltage of SSN w/o PDN models
- Voltage of SSN w PDN models
- Jitter due to SSN w/o PDN models
- Jitter due to SSN w PDN models

Noise Freq. (Hz) vs Jitter (ps)
• At Low Frequency Region
  (< several hundred MHz)
  – Off-chip decap
  – Split P/G planes

• At Mid. Frequency Region
  (< several GHz)
  – On-chip decap
  – Embedded cap in interposer
  – Trench, MiM cap with a high K material

• At High Frequency Region
  (> tens GHz)
  – On-chip EBG in the interposer
  – Connected with TSVs
  – Design issues: High Q inductor and Low ESR
On-Interposer EBG Structure

Capacitive P/G mesh
Width: 80um
Space: 120um

Inductive P/G mesh
Width: 40um
Space: 360um

Capacitive P/G mesh
Width: 80um
Space: 120um

Inductive P/G mesh
Width: 40um
Space: 360um
Measurement Results of On-interposer EBG

![Graph showing coupling coefficients S21 (dB) vs frequency (GHz) for Mesh PDN and TV A (Mesh) and TV B (EBG). The graph highlights the stopband and interposer EBG regions.]
Measurement Results of On-interposer EBG

![Graph showing coupled noise spectrum vs frequency (GHz)]

- Coupled Noise Spectrum (dBm)
- Frequency (GHz)

Key:
- TV A (Mesh)
- TV B (EBG)

1GHz
On-chip CMOS Active EBG

Spiral inductor

W_{inductor}

W_{inductor}

\( t_{top} \)

Si-substrate

NMOS cap.
Spiral inductor (portion) $t_{\text{top}}$

Via $t_{\text{metal}}$ $t_{\text{IMD}}$

Gate (1µm) Gate finger

* MagnaChip 0.18µm standard CMOS Process
Measured S21 of On-chip Active CMOS EBG

Frequency [GHz]

S21 [dB]

2.3 ~ 11.3 GHz (9 GHz)

- TV A (Meshed plane)
- TV B (Decap. Array)
- TV C (Active EBG)
Frequency [GHz]

S21 [dB]

--- TV C with 0V power (OFF)
--- TV C with 1.8V power (ON)

4.7 ~ 13.3 GHz

2.3 ~ 11.3 GHz

Tuning of On-chip Active CMOS EBG
Measured SSN Waveforms with a 3-GHz Clock Noise Input

TV A

TV B

TV C with 0V power

TV C with 1.8V power
Summary

- TSV is the most critical interconnection structure in 3D IC.

- TSV can cause significant channel loss for high-speed signaling.

- Equalizer or specific I/O schemes are needed to support low power and high-speed data transmissions.

- Crosstalk and coupling between TSV and active circuit need to be considered when designing the TSV arrangement configurations.

- Vertical coupling should be considered in mixed mode 3D IC.

- Shielding structures are needed to reduce the TSV crosstalks and noise couplings.