Reliability Evaluation of RF Amplifier Flip Chip Bumps

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Introduction:

Flip chip assembly offers a reliable, small footprint, thermally enhanced alternative to wirebonding. Copper "bumps" increase flip chip advantages for RF devices compared to solder bumps. This study will address failure mechanisms accelerated by thermal excursions and compare to volume production experiences. Thermal excursion mechanisms are ones accelerated by temperature cycling, thermal shock, reflow simulation and power cycling.

Purpose:

The intent of this work is to provide information on the methodology, implementation, and results of reliability assessments enacted on flip chip structures by thermal excursion testing. This project addresses these questions: 1) what are the expected failure mechanisms for flip chip assemblies? 2) Can on-chip power cycling be used to simulate and accelerate thermal excursion failure mechanisms? 3) What are the factors accelerating thermal excursion failure mechanisms? And 4) how is thermal excursion testing related to what is expected during use?

Bump and Test Structure Description:

A special test structure was designed and manufactured to investigate the primary failure mechanisms expected for the Flip Chip construction. The test structure includes a daisy chain of 36 bumps, a special detector, and a 15-Watt heater.

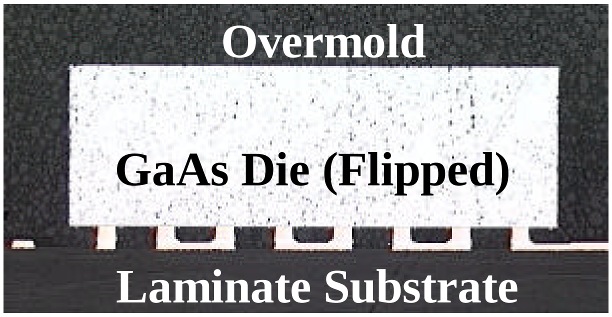

Figure 1. Cross-section of the Test Structure.

The detector was designed for multiple purposes. It serves as a temperature monitor, a mechanical fracture detector, a solder creep detector, and a leakage monitor. A laminate-based substrate was designed to match up with the flipped test structure. Normal manufacture includes a standard encapsulate. Various underfill materials and bump configurations were investigated using the test structures.

Test Methodology:

Thermal excursion testing is accomplished by subjecting samples to temperature extremes. These extremes are generated by thermal conduction in air, immersion in inert liquids, by infrared radiation, or by power dissipated within the device. All of the excursion testing is designed to alternate rapidly between the extremes. The reference level of testing used in this study is temperature cycling, per JESD22-A104-A Condition G, -40ºC to +125ºC, 1,000 cycles. In this study, excursions were accelerated using on-chip power cycling. An on-chip thermometer, as characterized in Figure 2 verified temperatures.

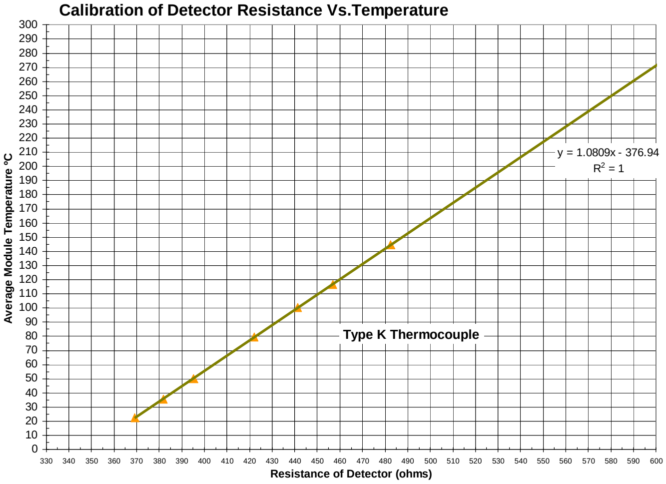

Figure 2. Thermal Characterization.

Various power cycling conditions were applied to several different flip chip lots. The cycling parameters of power, time on, and time off were varied and compared to results from the reference level test results. Figure 3 shows an example of data collected during accelerated power cycling.

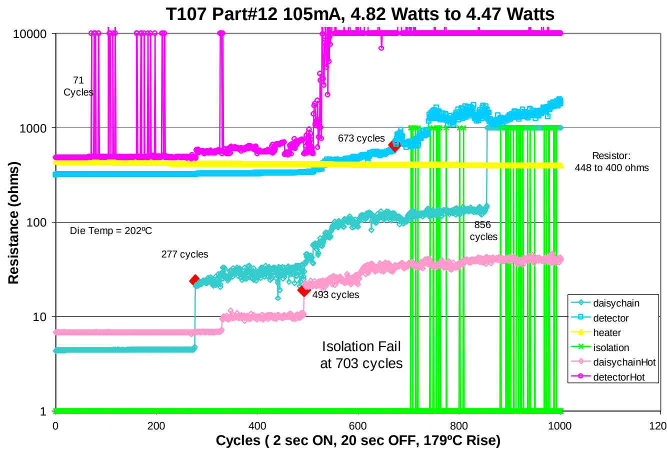

Figure 3. Typical Resistance Changes Observed During Power Cycling.

The failure mechanism for these special sample devices is a loss of functionality caused by an increase in resistance of certain interconnect pathways – basically, an open circuit. Example data indicating the effect of power cycling parameters is shown in Figure 4.

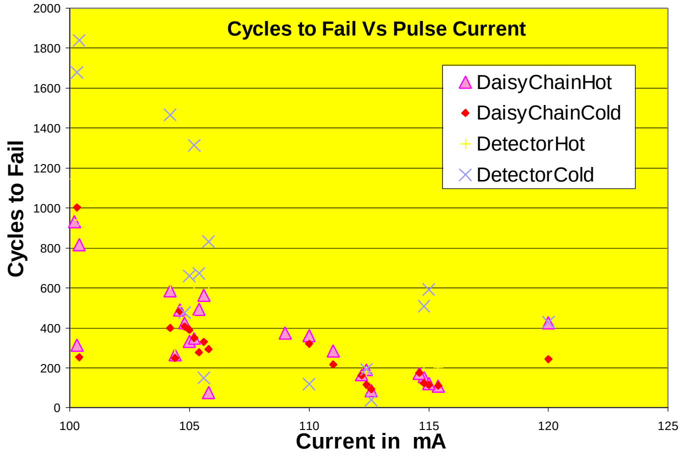

Figure 4. Typical Results of Various Current Levels Applied During Power Cycling.

Failure Mechanism:
Multiple failure mechanisms were generated using power cycling on the test structure. One of those generated was identical to failures observed during traditional air-to-air temperature cycling tests.

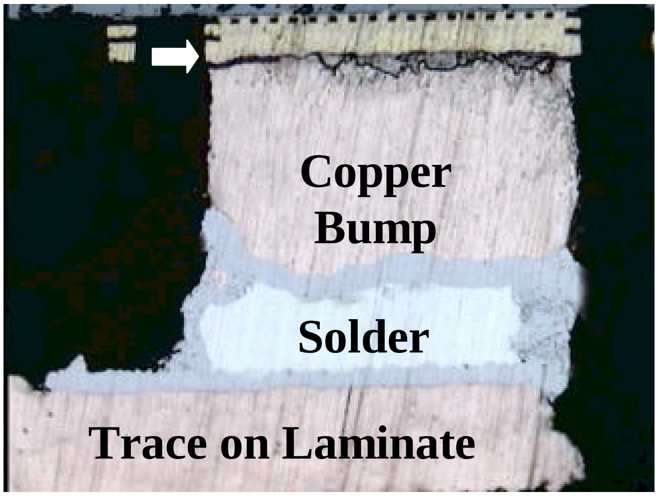

Figure 5. Typical Flip Chip Failure Cross-Section – Separation at Die Metallization.

Figure 6. Typical Flip Chip Failure Cross-Section – Separation Within Solder.

Conclusions:

1) A special structure can be designed based upon a Failure Modes and Effects Analysis (FMEA) investigation. The structure can perform as designed. 2) On-chip power cycling can be used to simulate and accelerate thermal excursion failure mechanisms. (See Figure 6) 3) Upon analysis and experimental design, factors of the power cycling can be adjusted to match results of longer thermal excursion testing. And 4) Thermal excursion mechanism can be accelerated to assess Flip Chip reliability in very short times.

Additional comparisons will be made between copper and more traditional solder bumps and between SIP and BGA package styles.