IEEE 2017 International Memory Workshop

May 14th – 17th, 2017 Hyatt Regency, Monterey, California

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- **Invited talks given by renowned experts**
- **Eric Shiu, SukHwan Lim, *Google*, « Memory architecture of consumer mobile devices in the era of machine intelligence and digital photography »**
- **Su Jin Ahn, *Samsung Electronics*, « Evolution of NAND Flash Memory: from 2D to 3D as a storage market leader »**
- **Dejan Vucinic, *Western Digital*, « Latency tails of byte-addressable non-volatile memories in systems »**
- **Kirk Prall, *Micron*, « Benchmarking and Metrics for Emerging Memories »**
- **Tom Andre, *Everspin*, « MRAM Fundamentals, Challenges, and Outlook »**
- **Hongshin Jun, *SKhynix*, « HBM (High Bandwidth Memory) DRAM Technology and Architecture »**
- **Nakayama Masayoshi, *Panasonic*, « ReRAM technologies: Applications and outlook »**
- **Jan Van Houdt, *IMEC, KU Leuven*, « 3D memories and ferroelectrics »**
- **Franck Arnaud, *STMicroelectronics*, « 16MB Phase Change Memory for Automotive and IoT Applications on 28nm FDSOI Technology »**
- **Pritish Narayanan, Geoffrey Burr et al., *IBM*, « Neuromorphic Technologies for Next-Generation Cognitive Computing »**

- **Papers solicited in all aspects of semiconductor memory technology (Flash, DRAM, PCRAM, RRAM, MRAM, SRAM, embedded memory, system, and other NV memories)**
- **Evening panel discussion**
- **Tutorial on Sunday 14th**
- **Submission deadline February 1st 2017**
- **Single submission of final, up to 4-page paper**

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The 9th IEEE International Memory Workshop (IMW) will be held at the Hyatt Regency, Monterey, California from Sunday May 14th though Wednesday May 17th, 2017. It is sponsored by the IEEE Electron Devices Society and meets annually in May. The IMW is a unique forum for specialists in all aspects of memory microelectronics and people with different backgrounds who wish to gain a better understanding of the field. The morning and afternoon technical sessions are organized in a manner to provide ample time for informal exchanges amongst presenters and attendees. The evening panel discussions will address hot topics in the memory field.

Papers are solicited in all aspects of semiconductor memory technology (Flash, DRAM, SRAM, PCRAM, RRAM, MRAM, embedded memory, system, and other NV memories), including but are not limited to:

Device Physics / Cell Design & Scaling / System Architecture
Error Management & Algorithms
New Concepts & Disruptive Technologies
Quality & Reliability / Circuit Design & Algorithms
SSD / Modeling / Emerging Applications & Markets

PAPER SUBMISSION

Please submit an electronic abstract in Adobe Acrobat (preferred) or Microsoft Word.
The suggested format can be found at: http://www.ieee.org/documents/MSW_USltr_format.doc.
Submit your abstract on the IEEE IMW website (http://www.ewh.ieee.org/soc/eds/imw/).
The abstract should be no more than four pages including supporting figures and tables.
The deadline for submitting abstracts is February 1st , 2017.
A very limited number of Late News Papers will be accepted (deadline to be announced).
The proceeding with all the accepted abstracts will be provided to the participants at the workshop as a bound book and in electronic format. It will also be submitted to the IEEE for submission to the Xplore database for easy referencing. In keeping with the workshop nature of the meeting, no photograph or recording will be allowed. Submissions from universities are encouraged.
There is a subsidized registration fee for students and IEEE Members. The maximum attendance at the workshop is limited. Therefore, advance registration is highly recommended.

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