8th International Memory Workshop

May 14th – 17th 2017

Hyatt Regency, Monterey, CA, US

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Intel	CEA LETI	Micron	U. of Wisconsin
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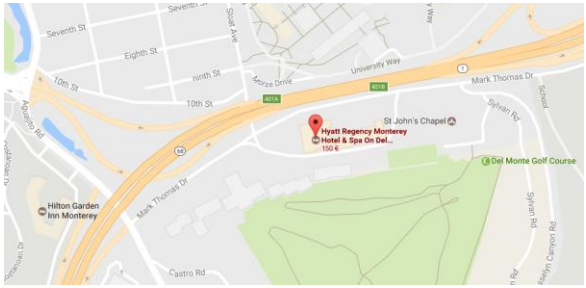
Advisory Committee

Jan Van Houdt, IMEC, Belgium
Agostino Pirovano, Micron, Italy
Sung-Yong Chung, SKHynix, Korea

Summary of Events

Sunday, 5/14	
Registration	7:00AM – 5:00PM
Tutorial	8:30AM – 11:45AM
Lunch Break (provided)	11:45AM – 1:45PM
Tutorial	1:45PM– 5:00PM
Monday, 5/15	
Registration	7:00AM – 6:00PM
Opening remarks	8:00AM – 8:20AM
Session #1	8:20AM – 11:20AM
Committee Luncheon	12:00PM – 2:00PM
Lunch Break (on your own)	
Session #2	2:00PM – 3:40PM
Panel discussion	4 :00PM – 5:30PM
Reception	5:30 PM
Poster Session	6:00PM – 8:30PM
Tuesday, 5/16	
Registration	7:00AM – 5:00PM
Session #3	8:30AM – 9:45AM
Session #4	10:15AM –12:20PM
Lunch Break (on your own)	12:20PM – 2:30PM
Session #5	2:30PM – 5:30PM
Banquet (provided)	7:00PM – 9:00PM
Wednesday, 5/17	
Registration	7:00AM – 12:00PM
Session #6	9:00AM– 12:00PM
Lunch Break (provided)	12:00 PM – 2:00PM
Session #7	2:00 PM– 3:15PM
Closing Remarks	3:15 PM – 3:30PM

Conference location:
Hyatt Regency, Monterey, California



Hyatt Regency Monterey Hotel and Spa on Del Monte Golf Course
1 Old Golf Course Road
Monterey, California, USA, 93940-4908
Tel: +1 831 372 1234

Sunday May 14th, 2017
Tutorial Registration on site: 7:00AM – 5:00PM

Tutorials **8:30AM-5:00 PM**
Chairs: Michael Gaidis (Crocus, USA)
Robert Strenz (Infineon, Germany)

PART I - Flash and emerging memories 8:30AM – 2:45PM

Yoshiaki Fukuzumi, Toshiba, « 3D memories, concepts, status, limitations, perspectives »
Daniele Ielmini, Politecnico di Milano, « Physics of emerging memories »
Keiichi Tsutsui, SONY, « Redefine Memory-System Interactions of SCM »
Lunch, provided (11:45 – 1:45)
Subhasish Mitra, Stanford, « Abundant-Data Computing: The N3XT 1,000X »

PART II - Ferroelectric Memories 2:45PM– 5PM

Thomas Mikolajick, TU Dresden « Basics, History and conventional FeRAM »
Uwe Schroeder, NaMLab GmbH, Dresden, "Ferroelectric HfO2: Basics, material properties and optimization »
Uwe Schroeder, NaMLab GmbH, Dresden, « HfO2 based FeRAM and NVDRAM »
Thomas Mikolajick, TU Dresden, « 1T FeFET Memory and an outlook to NCFET »

Poster Session

Monday May 15th, 2017 6:00 PM – 8:30 PM

1) A. Hayakawa, Department of Electrical, Electronic, and Communication Engineering, Chuo University, "Resolving Endurance and Program Time Trade-off of 40nm TaOx-based ReRAM by Co-optimizing Verify Cycles, Reset Voltage and ECC Strength"
2) T. Nakamura, Department of Electrical, Electronic, and Communication Engineering Chuo University, "AEP-LDPC ECC with Error Dispersion Coding for Burst Error Reduction of 2D and 3D NAND Flash Memories"
3) H. Zhang, Nanyang Technological University, "Single ITO/HfOx/TiN Complementary Switch with a Wide Read Voltage Window for Selector-less Crossbar RRAM Application"
4) Huaqiang Wu, Tsinghua University, "Performance Improvements by SL-Current Limiter and Novel Programming Methods on 16Mb RRAM Chip"
5) Yen-Chin Liao, National Chiao Tung University, "Data Analysis and Prediction for NAND Flash Decoding Status"
6) C. Zambelli, Universita degli Studi di Ferrara, "Characterization of TLC 3D-NAND Flash Endurance through Machine Learning for LDPC Code Rate Optimization"
7) Y. Tkachev, Silicon Storage Technology, "A Detailed Analysis of Hot-Electron Programming Efficiency in 40-nm Split-Gate Flash Memory Cells"
8) S. Agarwal, Sandia National Laboratories, "Compensating for Parasitic Voltage Drops in Resistive Memory Arrays"
9) H. Luan, Kilopass Technology, Inc. , "Minority Carrier Disturb in Thyristor Memory Arrays and a Novel Cell Design for High Density DRAM"
10) Y. Sugiyama, Department of Electrical, Electronic and Communication Engineering, Chuo University, Tokyo, Japan, "Reconfigurable SCM capacity Identification Method for SCM/NAND Flash Hybrid Disaggregated Storage"
11) S. J. Kim, The University of Texas at Dallas, "Low Temperature (400°C) Ferroelectric Hf0.5Zr0.5O2 Capacitors for Next-Generation FRAM Applications"

Monday May 15th, 2017

Registration 7:00 AM - 6:00 PM

Session #1 8:00 AM – 11:20 AM — Invited keynotes

Chairs: **Randy Koval, Intel, USA**
Gabriel Molas, CEA LETI, France

8:00 AM	Randy Koval, Opening Remarks
8:20 AM	Eric Shiu, SukHwan Lim, Google, "Driving innovation in memory architecture of consumer hardware with digital photography and machine intelligence use cases"
8:50 AM	Hyunsuk Kim, Su Jin Ahn, Samsung Electronics, "Evolution of NAND Flash Memory : From 2D to 3D as a Storage Market Leader"
9:20 AM	Dejan Vucinic, WDC, "Latency tails of byte-addressable non-volatile memories in system"
9:50 AM	Break (Refreshments Provided)
10:20 AM	Kirk Prall, Micron, "Benchmarking and Metrics for Emerging Memories"
10:50 AM	Pritish Narayanan, Geoffrey Burr, IBM, « Neuromorphic Technologies for Next-Generation Cognitive Computing »
11:20 AM	Lunch Break (on your own)
12:00 PM	Committee Luncheon

Session #2 2 PM – 3:40 PM — RRAM I

Chairs: **Zvonimir Bandic, Western Digital, USA**
Pawan Singh, Cypress, USA

2:00 PM	M. Nakayama, Panasonic Semiconductor Solutions Co., Ltd, "ReRAM technologies: Applications and outlook", ***invited***
2:25 PM	N. S. Avasarala, imec Leuven and KU Leuven, "Switching Behavior of HfO2-based Resistive RAM with Vertical CNT Bottom Electrode"
2:50 PM	C. Cagli, CEA LETI, "Study of the energy consumption optimization on RRAM memory array for SCM applications"
3:15 PM	C. Nguyen, CEA LETI, "Study of Forming impact on 4Kbit RRAM array performances and reliability"
3:40 PM	Break (Refreshments Provided)

Panel discussion 4:00 PM – 5:30 PM

The role of memory in the connected world and its readiness

Moderator: Scott Summerfelt, TI, USA

Reception: 5:30 PM

Chair: Gill Lee, Applied Materials, USA

Sponsor: Applied Materials, Inc., USA

Poster Session: 6:00 PM – 8:30 PM

Chair: Gill Lee, Applied Materials, USA

6:00 PM Poster Introduction
(See the front page for the list of poster papers)

Tuesday May 16th, 2017

Registration 7:00 AM - 5:00 PM

Session #3 8:30 AM – 9:45 AM — PCM and selectors

Chairs: **Alfonso Maurelli, STMicroelectronics, Italy**
Wei-Chen Chen, Macronix, Taiwan

8:30 AM	F. Arnaud, P. Zuliani, B. Giraud, STMICROELECTRONICS, "Embedded Phase Change Memory Solution Enablement based on 28FDSOI CMOS Technology", ***invited***
8:55 AM	A. Verdy, CEA LETI, "Improved Electrical Performance Thanks to Sb and N Doping in Se-rich GeSe-Based OTS Selector Devices"
9:20 AM	Scott W. Fong, Stanford University, "Dual-layer Dielectric Stack for Thermally-isolated Low-power Phase-change Memory"
9:45 AM	Break (Refreshments Provided)

Session #4 10:15 AM – 12:20 PM — FRAM and DRAM

Chairs: **Syed M. Alam, Everspin, USA**
Jan Van Houdt, IMEC, Belgium

10:15 AM	J.Van Houdt, IMEC, KU Leuven, "3D memories and ferroelectrics", ***invited***
10:40 AM	M. Takahashi, National Institute of Advanced Industrial Science and Technology, "Dynamic Analog Characteristics of 10^9 cycle-Endurance Low-voltage Nonvolatile Ferroelectric-gate Memory Transistors"
11:05 AM	Hongshin Jun, SK Hynix, "HBM (High Bandwidth Memory) DRAM Technology and Architecture", ***invited***
11:30 AM	M. S. Parihar, Univ. Grenoble Alpes, IMEP-LAHC, Grenoble INP Minatec, CNRS, F-38000 Grenoble, France, "Low-Power Z^2-FET Capacitorless 1T-DRAM"
11:55 AM	T. Maeda, Toshiba Corporation, Stanford University, "Identifying Ferroelectric Switching Pathways in HfO2 First Principles Calculations Under Electric Fields"
12:20 PM	Lunch (On your own)

Session #5 2:30 PM – 5:30 PM — 3D-NAND and embedded

Chairs: **Jungdal Choi, SK Hynix, Korea**
Rino Micheloni, Microsemi, Italy

2:30 PM	C. Caillat, Micron Technology, "3DNAND GIDL-Assisted Body Biasing for Erase Enabling CMOS Under Array (CUA) Architecture"
2:55 PM	A. Arreghini, IMEC, "First demonstration of SiGe channel in Macaroni geometry for future 3D NAND"
3:20 PM	K. Mizoguchi, Department of Electrical, Electronic, and Communication Engineering, Chuo University, "Data-Retention Characteristics Comparison of 2D and 3D TLC NAND Flash Memories"
3:45 PM	Break (Refreshments Provided)
4:15 PM	D. Shum, Globalfoundries, "40nm Embedded Self-Aligned Split-Gate Flash Technology for High-Density Automotive Microcontrollers"
4:40 PM	T. Saito, Renesas Electronics Corporation, "High-temperature stable Physical Unclonable Functions with error-free readout scheme based on 28nm SG-MONOS flash memory for security applications"
5:05 PM	C.-L. Tan, IMEC, "In depth analysis of 3D NAND enablers in Gate Stack Integration and Demonstration in 3D devices"

Banquet 7:00 PM - 9:00 PM (provided)

Wednesday May 17th, 2017

Registration 7:00 AM - 12:00 PM

Session #6 9 AM – 12 PM — RRAM and neuromorphic

Chairs: **Wataru Otsuka, SONY, Japan**
Zhiqiang Wei, Panasonic, Japan

9 AM	E. Vianello, CEA LETI, "RRAM memories for spike-based neuromorphic circuits", ***invited***
9:25 AM	M. Alayan, CEA LETI, "Self-rectifying Behavior and Analog Switching Under Identical Pulses Using Tri-layer RRAM Crossbar Array for Neuromorphic System"
9:50 AM	D. Wouters, RWTH Aachen Univeristy, Aachen, Germany, "Overcoming the RESET Limitation in Tantalum Oxide-Based ReRAM Using an Oxygen-Blocking Layer"
10:15 AM	Break (Refreshments Provided)
10:45 AM	C. Adda, J. Tranchant, Institut des Matériaux Jean Rouxel (IMN), Université de Nantes, CNRS , "An artificial neuron founded on resistive switching of Mott insulators"
11:05 AM	M. Suri, Indian Institute of Technology, Delhi, "Experimental Validation of CBRAM Performance Enhancement Using FNW Soft-Technique"
11:30 AM	Y. Song, Stanford University, "Improving the High Resistance State Retention Degradation of Al-doped HfOx Based on Ab Initio Simulations"
12 PM	Lunch (Provided)

Session #7 2 PM – 3:15 PM — MRAM

Chairs: **Michael Gaidis, Crocus, USA**
Tom André, Everspin, USA

2 PM	T. Andre, Everspin, "MRAM Fundamentals, Challenges, and Outlook", ***invited***
2:25 PM	H. Yoda, Toshiba Corporation, "High-Speed Voltage-Control Spintronics Memory"
2:50 PM	A. Cagliani, Capres A/S - DTU-Nanotech, "Breakthrough In Current In Plane Metrology For Monitoring Large Scale MRAM Production"

3:15 PM – 3:30 PM Closing Remarks & Adjourn