



## 10<sup>th</sup> International Memory Workshop

May 13<sup>th</sup> – 16<sup>th</sup> 2018

*The Westin Miyako, Kyoto, Japan*

Keage, Sanjo, Higashiyama-ku Kyoto,

Kyoto 605-0052 Japan

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## Summary of Events

### Sunday, 5/13

Registration	7:00AM – 5:00PM
Tutorial	8:30AM – 11:45AM
Lunch Break (provided)	11:45AM – 1:45PM
Tutorial	1:45PM – 4:45PM

### Monday, 5/14

Registration	7:00AM – 6:00PM
Opening remarks	8:30AM – 8:50AM
<b>Session #1</b>	8:50AM – 11:20AM
Committee Luncheon	12:00PM – 2:00PM
Lunch Break (on your own)	
<b>Session #2</b>	2:00PM – 3:40PM
Panel discussion	4 :00PM – 5:30PM
Reception	5:30 PM - 8:30PM
Poster Session	6:00PM – 8:30PM

### Sunday May 13<sup>th</sup>, 2018

Tutorial Registration on site: 7:00AM – 5:00PM

### Tutorials

**8:30AM-4:45 PM**

**Chairs: Alfonso Maurelli, STMicroelectronics, Italy**  
**Anirban Roy, NXP, Netherlands**

### PART I – 3D NAND and Embedded Memories

**8:30AM – 11:45AM**

**Tomoya Saito**, Renesas, « Split-Gate MONOS embedded Flash Technology for Automotive Applications »

**Igor Kouznetsov**, Cypress, « Embedded Flash for Consumer and Industrial Applications in the age of IoT »

**Sean Kang**, Applied Materials, « Materials, Processes, Equipment Perspectives of 3D NAND Technology and Its Scaling »

**Geert Van den bosch**, IMEC, « Understanding and improving conduction in 3D NAND channels »

*Lunch, provided (11:45 – 1:45)*

### PART II - Neuromorphic Memories

**1:45PM– 4:45PM**

**Damien Querlioz**, Univ. Paris-Sud, « Correspondence between emerging memories and neuromorphic computing: the case of spintronic devices »

**Philippe Talatchian**, CNRS, « Neuromorphic Computing with Spintronic Nano-Oscillators »

**Dmitri Strukov**, UC Santa Barbara, « Opportunities and challenges for neurocomputing with nonvolatile memory devices »

**Tian-Sheuan Chang**, National Chiao Tung University, « Current status and future outlook of AI accelerator: from digital to in-memory computing »

**Tuo-Hung Hou**, National Chiao Tung University, «RRAM-based neuromorphic computing: Device and algorithm co-design»

### Tuesday, 5/15

Registration	7:00AM – 5:00PM
<b>Session #3</b>	8:30AM – 11:30AM
Lunch Break (on your own)	11:30AM – 2:00PM
<b>Session #4</b>	2:00PM – 5:00PM
Banquet (provided)	7:00PM – 9:00PM

### Wednesday, 5/16

Registration	7:00AM – 12:00PM
<b>Session #5</b>	8:30AM– 11:10AM
Lunch Break (provided)	11:10 AM – 1:00PM
<b>Session #6</b>	1:00 PM – 2:40PM
Award & Closing Remarks	2:40 PM – 3:30PM

### Poster Session

**Monday May 14<sup>th</sup>, 2018** **6:00 PM – 8:30 PM**

**[P1]** Si Joon Kim, The University of Texas at Dallas, “Ferroelectric TiN/Hf0.5Zr0.5O2/TiN Capacitors with Low-Voltage Operation and High Reliability for Next-Generation FRAM Applications”

**[P2]** Hangbing Lv, “Switching and Failure Mechanism of Self-selective Cell in 3D VRRAM by RTN-based Defect Tracking Technique”

**[P3]** Roger Lo, Macronix International Co., Ltd., “Study of Thyristor-Mode Dual-Channel NAND Flash Devices”

**[P4]** Juseop Park, Samsung Electronics, “A Built-In Self Test Compensating Process-Voltage Variation in Data Paths of High Performance DRAMs”

**[P5]** Fiona Wang, Rambus Inc. “DRAM Retention at Cryogenic Temperatures”

**[P6]** Yuri Tkachev, Silicon Storage Technology, “The Analysis of Erase Voltage Variability in 70-nm Split-Gate Flash Memory Arrays”

**[P7]** Manan Suri, Indian Institute of Technology – Delhi, “High-Quality PUF Extraction from Commercial RRAM using Switching-Time Variability”

**[P8]** Nhan Do, Silicon Storage Technology, A subsidiary of Microchip Technology Inc “Scaling of Split-Gate Flash Memory with 1.05V Select Transistor for 28nm Embedded Flash Technology”

**[P9]** S.H. Ku, Macronix International Co., “Error Characterization and ECC Usage Relaxation beyond 20nm Floating Gate NAND Flash Memory”

**[P10]** Gilbert Sassine, CEA-LETI, “Optimizing programming energy for improved RRAM reliability for high endurance applications”

**[P11]** Mitsue Takahashi, National Institute of Advanced Industrial Science and Technology, “High-Endurance Ferroelectric NOR Flash Memory Using (Ca,Sr)Bi2Ta2O9 FeFETs”

**[P12]** Yi Li, Huazhong University of Science and Technology, “Implementation of Functionally Complete Boolean Logic and 8-bit Adder in CMOS Compatible 1T1R RRAMs for In-Memory Computing”

**[P13]** Mrinmoy Dutta, Chang Gung University, “Cu filament based resistive switching and oxidation-reduction through dopamine sensing in novel Cu/MoS2/TiN structure”

**[P14]** Shogo Matsumoto, Graduate School of Informatics, Kyoto University, “RRAM/CMOS-Hybrid Architecture of Annealing Processor for Fully Connected Ising Model”

**[P15]** Julien Tranchant, Institut des Matériaux Jean Rouxel (IMN), Université de Nantes, CNRS, “Mott memory devices based on the Mott insulator (V1-xCr)x2O3”

## Monday May 14<sup>th</sup>, 2018

Registration 7:00 AM - 6:00 PM

### Session #1 8:30 AM – 11:20 AM [Invited keynotes](#)

**Chairs:** Gabriel Molas, CEA LETI, France  
Akira Goda, Micron, USA

- 8:30 AM Gabriel Molas, Opening Remarks  
8:50 AM **[1-1]** Satoshi Inaba, Toshiba Memory “3D Flash Memory for Data-intensive Applications”  
9:20 AM **[1-2]** Gurtej S. Sandhu, Micron “Future of DRAM”  
9:50 AM Break (Refreshments Provided)  
10:20 AM **[1-3]** Hai Wang, NXP, “Challenges in Automotive Memory Solutions”  
10:50 AM **[1-4]** Stefan Müller, FMC, « Ferroelectric HfO<sub>2</sub> and its Impact on the Memory Landscape »  
11:20 AM Lunch Break (on your own)  
12:00 PM Committee Luncheon

### Session #2 2PM – 3:40 PM [PCM and selectors](#)

**Chairs:** Wataru Otsuka, SONY, Japan  
TBD

- 2:00 PM **[2-1]** Gabriele Navarro, LETI, “Phase-Change Memory: Performance, Roles and Challenges”, *invited*  
2:25 PM **[2-2]** Anthonin Verdy, CEA-LETI, “High Temperature Stability and Performance Analysis of N-doped Ge-Se-Sb based OTS Selector Devices”  
2:50 PM **[2-3]** Jean-Jacques Fagot, STMicroelectronics, “Low Cost Diode as Selector Device for Embedded Phase Change Memory in Advanced FD-SOI Technology”  
3:15 PM **[2-4]** Marinela Barci, IMEC, “Engineering and Stack Optimization of Cu-based Selector Devices for Low Power SCM Applications”  
3:40 PM Break (Refreshments Provided)

### Panel discussion 4:00 PM – 5:30 PM

#### In-Memory Computing

Moderator: Zvonimir Bandic, Western Digital, USA

### Reception: 5:30 PM

**Chair:** Gill Lee, Applied Materials, USA  
**Sponsor:** Applied Materials, Inc., USA

### Poster Session: 6:00 PM – 8:30 PM

**Chair:** Gill Lee, Applied Materials, USA  
6:00 PM Poster Introduction  
(See the front page for the list of poster papers)

## Tuesday May 15<sup>th</sup>, 2018

Registration 7:00 AM - 5:00 PM

### Session #3 8:30 AM – 11:30 AM [RRAM and Emerging Memories](#)

**Chairs:** Pawan Singh, Cypress, USA  
Damien Deleruyelle, INSA de Lyon, France

- 8:30 AM **[3-1]** Kazuhiro Ohba, SONY, “Cross point Cu ReRAM with BC doped Selector”, *invited*  
8:55 AM **[3-2]** Janaki Radhakrishnan, IMEC & KU Leuven, “On the key impact of composition of Ge-Te and Ge-Se electrolytes on CBRAM properties”  
9:20 AM **[3-3]** Masashi Arita, Hokkaido University, “Oxygen distribution around filament in Ta-O resistive RAM fabricated using 40 nm CMOS technology”  
9:45 AM Break (Refreshments Provided)  
10:15 AM **[3-4]** Subhali Subhechha, imec/KU Leuven, imec/KU Leuven, “Understanding endurance in TiN/a-Si/TiO<sub>x</sub>/TiN RRAM devices”  
10:40 AM **[3-5]** Mahendra Pakala, Applied Materials, “Materials & Processes for Emerging Memory”, *invited*

### Session #3 (continued) Embedded Memory (Late News)

- 11:05 AM **[3-6]** James Pak, Cypress Semiconductor Corporation, “40nm & 22nm Embedded Charge Trap Flash for Automotive Applications”, *Late News*  
11:30 AM Lunch (On your own)

### Session #4 2:00 PM – 5:00 PM [MRAM and Memory Periphery](#)

**Chairs:** Gwan-Hyeob Koh, Samsung, Korea  
Tomoya Sanuki, Toshiba Memory, Japan

- 2:00 PM **[4-1]** Yiming Huai, Avalanche, “High density 3D Cross-point STT-MRAM”, *invited*  
2:25 PM **[4-2]** Luc Tillie, CEA-LETI, “Temperature limits of single and composite storage layer with different thicknesses and capping materials for p-STT-MRAM applications”  
2:50 PM **[4-3]** Hideo Sato, Center for Innovative Integrated Electronic Systems, Tohoku University, “1T-1MTJ type embedded STT-MRAM with advanced low-damage and short-failure-free RIE technology down to 32 nm MTJ patterning”  
3:15 PM Break (Refreshments Provided)  
3:45 PM **[4-4]** Bharat Bhushan, GLOBALFOUNDRIES Singapore Pte. Ltd., “Enhancing Magnetic Immunity of STT-MRAM with Magnetic Shielding”  
4:10 PM **[4-5]** Won Ho Choi, Western Digital Research, “A Comprehensive Study on DDR4 MRAM and ReRAM Power Estimation using a Parameterized NVM Power Calculator”  
4:35 PM **[4-6]** Alessio Spessot, IMEC, “Cost effective FinFET platform for Stand Alone DRAM 1Y and beyond memory periphery”

**Banquet 7:00 PM - 9:00 PM (provided)**

## Wednesday May 16<sup>th</sup>, 2018

Registration 7:00 AM - 12:00 PM

### Session #5 8:30 AM – 11:10 AM [RRAM and Neuromorphic](#)

**Chairs:** Hangbing Lv, IME, China  
Wei-Chen Chen, Macronix, Taiwan

- 8:30 AM **[5-1]** Satoru Ito, Panasonic, “ReRAM technologies for embedded memory and further applications”, *invited*  
8:55 AM **[5-2]** Yoshiaki Deguchi, Chuo University, “Error-Reduction Controller Techniques of TaO<sub>x</sub>-based ReRAM for Deep Neural Networks to Extend Data-Retention Lifetime by Over 1700x”  
9:20 AM **[5-3]** Qiangfei Xia, University of Massachusetts Amherst, In-Memory Computing with Memristor Arrays”  
9:45 AM Break (Refreshments Provided)  
10:15 AM **[5-4]** Toshitsugu Sakamoto, NEC, “Atom switch with improved cycle endurance using field enhancement for nonvolatile SoC”  
10:40 AM **[5-5]** Marco Sforzin, Micron, “Self-Referenced Read methodology for EMs”  
11:10 AM Lunch (Provided)

### Session #6 1:00 PM – 2:40 PM [3D NAND and Embedded](#)

**Chairs:** Tomoya Sanuki, Toshiba Memory, Japan  
Rino Micheloni, Microsemi, Italy

- 1:00 PM **[6-1]** Hung-Sheng Chang, Macronix, “System Performance Analysis of Bit-Alterable 3D NAND Flash Devices for High-Performance Solid-State Drive (SSD) Applications”  
1:25 PM **[6-2]** Yung Chun Lee, Macronix, “Study of Counter-Pulse (CP) Programming Method to Improve the Vt Distribution for 3D Charge-Trapping NAND Flash Devices”  
1:50 PM **[6-3]** Yoshiaki Deguchi, Chuo University, “3D-NAND Flash Solid-State Drive (SSD) for Deep Neural Network Weight Storage of IoT Edge Devices with 700x Data-retention Lifetime Extension”  
2:15 PM **[6-4]** Igor Kouznetsov, Cypress Semiconductor, “40 nm Ultralow-Power Charge-Trap Embedded NVM Technology for IoT Applications”

### 2:40 PM – 3:30 PM

**Best Paper Award announcement**  
**Closing Remarks & Adjourn**