Virtual Event Details

• The workshop will be a virtual On-Demand event with the logistics set-up by the IEEE Meetings, Conferences & Events (MCE) Digital Events team. All presentations (tutorials, invited/accepted papers, and posters) and opening/closing remarks will be posted online video presentation with pre-recorded audio narration. Please note that IMW has a DO NOT record policy, and contact presenters for presentation material.

• Program is divided into 13 Virtual sessions: Tutorial 2 sessions, Opening Remarks, Technical Program 9 sessions and Closing Remarks. Virtual sessions will be made available in a staggered manner based on virtual program (suggested schedule) – May 17th: Tutorials, May 18th: Session 1-3, May 19th: Sessions 4-6, and May 20th: Sessions 7-9. All sessions in a given day will be made available in Asia time-zone.

• All sessions will be available until May 25th for on-demand viewing at any time after release. Please note program schedule is only suggested viewing schedule. However, for Q&A, only questions submitted within 24 hours of session schedule (US Pacific time) will get responses.

• To access the Virtual sessions, please visit the corresponding side-tab on the conference site and click on the session you wish to attend. In order to access the Virtual sessions, you must have a paid registration to IMW 2020. Enter the Registration Email used for your Conference Registration. Please note that it must match the email address in your confirmation email or you will be unable to access the Session. Under the Virtual sessions, each paper presentation is indexed as a Chapter. You can also navigate forward/back with the Presentation or pause/play using the Media Player controls. You can hit “enlarge” button on the controls to move it to the top of the screen if it is hidden behind the bottom icons. If you experience interruptions in audio/video while playing the presentations, it may be related to internet connection issues, and we found that rewinding or restarting helps in such cases.

• Tutorial eBook PDF and Technical Digest (papers) PDF will be available for download under “Resource List” in any of the Tutorial and Technical Program virtual sessions, respectively. Alternatively, both PDFs are available in Opening/Closing Remarks sessions.

• Q&A: Attendees can submit questions using “Q&A” button for each session and will need to identify the paper number within the session in the question (for eg., paper 1.3, 2.4, so on). Questions submitted until session day + 1 (5PM US Pacific) will get responses. Session chair will coordinate & moderate the Q&A, and both the question and the answer will be posted to the chat window which will be visible to all attendees. Attendees are requested to refrain from using the chat window.

Help Desk Information: Please direct any questions about access or the Virtual Conference platform to IEEE MCE’s Brett Houseal at b.houseal@ieee.org

For any other questions, please email at imw2020.org@gmail.com
**Summary of Events**

Virtual On-Demand Event May 17th-25th : suggested schedule only

### Sunday, 5/17
- **Tutorial – 3D NAND**
  - 8:00AM – 11:00AM
  - 11:00AM – 1:00PM
- **Tutorial – MRAM**
  - 1:00PM – 3:00PM

**Lunch Break**
1:00PM – 1:30PM

### Monday, 5/18
- **Session #1 – Invited Keynotes**
  - 8:00AM – 8:30AM
- **Session #2 – 3D NAND**
  - 8:30AM – 10:00AM
- **Lunch Break**
  - 10:00AM – 11:00AM
- **Session #3 – RRAM**
  - 11:00AM – 1:00PM

**Lunch Break**
1:00PM – 1:30PM

### Tuesday, 5/19
- **Session #4 – FRAM and MRAM - 1**
  - 8:30AM – 9:40AM
- **Session #5 – FRAM and MRAM - 2**
  - 10:30AM – 11:40AM
- **Lunch Break**
  - 11:40AM – 1:00PM
- **Session #6 - Embedded**
  - 1:00PM – 2:40PM

### Wednesday, 5/20
- **Session #7 – Computing In-Memory 1**
  - 8:30AM – 9:50AM
- **Session #8 – Computing In-Memory 2**
  - 10:30AM – 11:40AM
- **Lunch Break**
  - 11:40AM – 1:00PM
- **Session #9 – PCM and Selectors**
  - 1:00PM – 2:10PM
- **Closing Remarks**
  - 2:10PM – 2:30PM

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**Sunday May 17th, 2020**

- **Tutorials**
  - 8:00AM-3:00PM

**PART I – 3D NAND**
8:00AM – 11AM

- **Noboru Shibata**, Kioxia Corporation, « History and Future of Multi-Level-Cell Technology in 2D and 3D Flash Memory »
- **Yan Li**, Western Digital Corporation, « 3D NAND Architecture and its Application »

**PART II - MRAM**
1:00PM– 3:00PM

- **Thibaut Devolder**, Université Paris-Saclay, « STT-MRAM switching: key features of the dynamics and modulation knobs »
- **Arnaud Furnemont**, imec, « Beyond 1T-1STTMRAM: magnetic memory challenges and opportunities »
Monday May 18th, 2020

Session #1 8:00 AM – 09:30 AM  Invited Keynotes
Chairs: Zhiqiang Wei, Avalanche Technology, USA
Srivardhan Gowda, Intel, China
8:00 AM Zhiqiang Wei, Opening Remarks
8:30 AM [1.1] Shigeru Shiratate, Micron Technology, "Scalability and Performance Challenges of Future DRAM"
8:50 AM [1.2] Pranav Kalavade, Intel Corporation, "4 bits/cell 96 Layer Floating Gate 3D NAND with CMOS under Array Technology and SSDs"
9:30 AM Break

Session #2 10:00 AM – 10:50 AM  3D NAND
Chairs: Tomoya Sanuki, Kioxia, Japan
Wei-Chen Chen, Macronix, Taiwan
10:00 AM [2.1] Laurent Breuil, imec, "Integration of Ruthenium-based Wordline in a 3-D NAND Memory Devices"
10:20 AM [2.2] Hideo Horii, Kioxia Corporation, "Thyristor Operation for High Speed Read / Program Performance in 3D Flash Memory with Highly Stacked WL-Layers"
10:40 AM [2.3] Hiroki Ahara, Chuo University, "Extremely Biased Error Correction Method to Reduce Read Disturb Errors of 3D-TLC NAND Flash Memories by 60%", Poster
10:50 AM Lunch Break

Session #3 1:00 PM – 2:10 PM  RRAM
Chairs: Georg Tempel, Infineon, Germany
Dirk Wouters, RWTH, Germany
1:00 PM [3.1] Gabriel Molas, CEA LETI, "Crosspoint Memory Arrays: Principle, Strengths and Challenges", Invited
1:20 PM [3.2] Stefan Wiefels, I2EW, RWTH Aachen University, "Statistical Modeling and Understanding of HRS Retention in 2.5 Mbit HIQO based ReRAM"
1:40 PM [3.3] Joel Minguet Lopez, CEA LETI, "Optimization of RRAM and OTS selector for advanced low voltage CMOS compatibility"
2:00 PM [3.4] Yachuan PANG, Tsinghua University, "A RRAM-based Data Hiding Technique Utilizing the Impact of Form Condition on SET Performance", Poster

Tuesday May 19th, 2020

Session #4 8:30 AM – 09:40 AM  FRAM and MRAM - I
Chairs: Jane Yater, NXP Semiconductors, USA
Thomas Mikolajick, NaMLab and TU Dresden, Germany
8:30 AM [4.1] Zhihu Wang, Avalanche Technology, "STT-MRAM for Embedded Memory Applications", Invited
8:50 AM [4.2] Tarek Ali, Fraunhofer IPMS Center Nanoelectronic Technologies, "Effect of Substrate Implant Tuning on the Performance of MFIS Silicon Doped Hafnium Oxide (HSO) FeFET Memory"
9:10 AM [4.3] Marco Mansueto, Univ. Grenoble Alpes, CEACNRs, "Isotropically coercive free layer integration in a magnetic tunnel junction for neuromorphic applications"
9:30 AM [4.4] Hao Jiang, Yale University, "A Study of BEOL Processed Hf0.5Zr0.5O2-based Ferroelectric Capacitors and Their Potential for Automotive Applications", Poster
9:40 AM Break

Session #5 10:30 AM – 11:40 AM  FRAM and MRAM - II
Chairs: Lucian Prejeanu, CEA-SpiPtec, France
Damien Deleruyelle, INSa Lyon, France
10:30 AM [5.1] Sven Beyer, GLOBALFOUNDRIES, "FeFET: A versatile CMOS compatible device with game-changing potential", Invited
10:50 AM [5.2] Patrick Lomenzo, NaMLab and TU Dresden, "Thickness Scaling of AFE-RAM ZrO2 Capacitors with High Cycling Endurance and Low Process Temperature"
11:10 AM [5.3] Joel Molina Reyes, National Institute of Astrophysics, Optics and Electronics, Mexico, "Interface engineering of BEOL compatible ferroelectric Y-HIO2 device for enhanced endurance"
11:30 AM [5.4] Nicolo Ronchi, imec, "Endurance of ferroelectric La-doped HIO2 for SFS gate-stack memory devices", Poster
11:40 AM Lunch Break

Session #6 1:00 PM – 2:40 PM  Embedded
Chairs: Alfonso Maurelli, STMicroelectronics, Italy
Yong Kyu Lee, Samsung, Korea
1:20 PM [6.2] Haidi Zhou, Ferroelectric Memory GmbH, "Endurance and targeted programming behavior of HIQO2-FeFETs"
1:40 PM [6.3] Sergioj Jourba, Silicon Storage Technology, "Performance and Reliability of 4 Mb eFLASH Memory Array Featuring 28 nm Split-Gate Cell with HKMG Select Transistors"
2:00 PM [6.4] Yanzhe Wang, Renesas Electronics Corporation, "Sub-6V operation of split-gate type charge-trapping nonvolatile memory with high-k trapping and blocking layers for high-speed and highly-reliable embedded Flash"

Wednesday May 20th, 2020

Session #7 8:30 AM – 09:50 AM  Computing In-Memory - I
Chairs: Tomoya Saito, Renesas, Japan
Tomoya Sanuki, Kioxia, Japan
8:50 AM [7.2] Masanori Hayashikoshi, Renesas Electronics Corporation, "Processing In-Memory Architecture with On-Chip Transfer Learning Function for Compensating Characteristic Variation"
9:10 AM [7.3] Po-Kai Hsu, Macronix International Co., Ltd., "An Approach of 3D NAND Flash Based Nonvolatile Computing-In-Memory (nvCIM) Accelerator for Deep Neural Networks (DNNs) with Calibration and Read Disturb Analysis"
9:30 AM [7.4] Masaki Abe, Chuo University, "Computational Approximate Storage with Neural-Network-based Error Patrol of 3D-TLC NAND Flash Memory for Machine Learning Applications", Poster
9:40 AM [7.5] Vineet Agrawal, Cypress Semiconductor Corp., "In-Memory Computing array using 40nm multibit SONOS achieving 100 TOPS/W energy efficiency for Deep Neural Network Edge Inference Accelerators", Poster
9:50 AM Break

Session #8 10:30 AM – 11:40 AM  Computing In-Memory - II
Chairs: Thomas Mikolajick, NaMLab and TU Dresden, Germany
Stephen Heinrich-Barna, Texas Instruments, USA
10:50 AM [8.2] Umberto Minucci, Micron, "A Neural Network implemented on NAND memory"
11:20 AM [8.4] Shubham Sahay, University of California, Santa Barbara, "A 2T-1R Cell Array with High Dynamic Range for Mismatch-Robust and Efficient Neurocomputing", Poster
11:30 AM [8.5] Yan Liao, Tsinghua University, "Parallel Resistance Effect Analysis in RRAM-based TCAM for Memory Augmented Neural Networks", Poster
11:40 AM Lunch Break

Session #9 1:00 PM – 2:30 PM  PCM and selectors
Chairs: Akira Goda, Micron, Japan
Wataru Otsuka, Sony, Japan
1:00 PM [9.1] Mario Laudato, Intermolecular Inc., "ALD GeAsSeTe Transistor Threshold Switch for 3D stackable crosspoint memory"
1:20 PM [9.2] Shamin Housham Sharif, imec, "Sub-Åµm a-IGZO, Fully integrated, Process improved, Vertical diode for Crosspoint arrays"
1:40 PM [9.3] Camille Laguna, CEA LETI, "Innovative Multilayer OTS Selectors for Performance Tuning and Improved Reliability"
2:00 PM [9.4] Yusuke Hine, Chuo University, "Data Allocation Algorithm based on Write and Read Frequency for Double Asymmetric-latency SCM SSD", Poster
2:10 PM Zhiqiang Wei, Closing Remarks