

# Building and Testing a 100 MHz Filter

Michael Andrew Cracraft and Todd Hubing  
EMC Laboratory, University of Missouri - Rolla

## 1. Objectives

Parasitic inductance and capacitance play an important role in circuitry beyond a few hundred MHz. The objective of this experiment is to enhance the understanding of the parasitic parameters through building a 100 MHz low-pass filter that functions up to 1 GHz.

## 2. Equipment

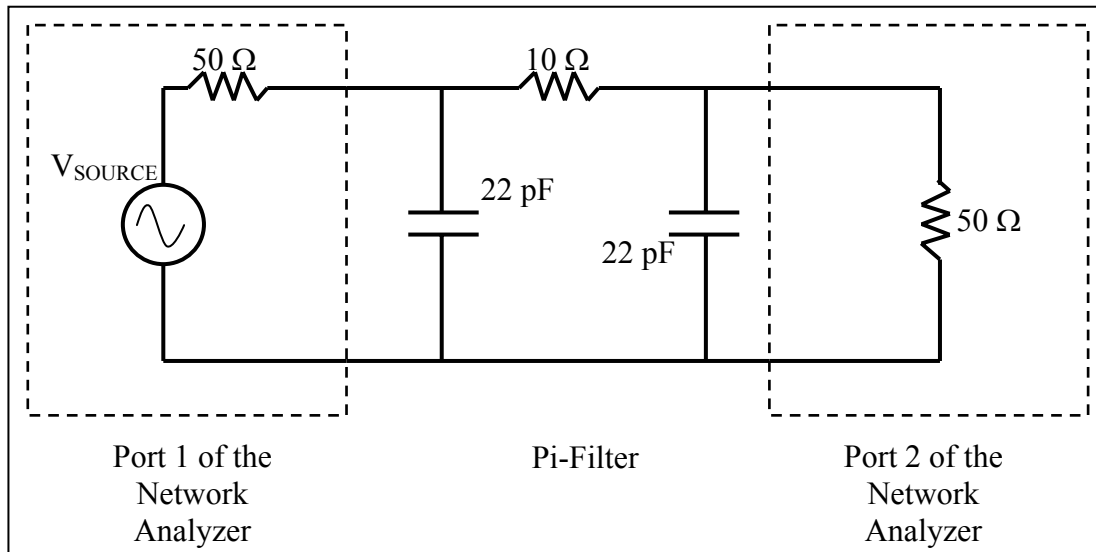
1. HP8753D Network Analyzer
2. Two phase-matched armored cables with precision 3.5-mm connectors
3. Two 3.5-mm (f) – 7-mm adaptors (m)
4. Copper-tape, utility knives, solder, and soldering stations as needed
5. One filter kit, including
  - a. Two 85-mil SMA probes with semi-rigid coax
  - b. One 3" x 3" copper-clad board
  - c. One 10- $\Omega$  surface-mount (SMT) resistor
  - d. Two 22-pF SMT capacitors

## 3. Introduction

Input/Output (I/O) lines often comprise one part of the antenna in radiated electromagnetic interference (EMI) problems. To mitigate the EMI, the I/O lines are often filtered before being routed off the printed circuit board (PCB) and onto the I/O line. Low-pass lossy pi-filters are preferred for this task because the insertion loss increases 40 dB/decade beyond the cut-off frequency.

Implementing the filter provides some significant obstacles. The capacitor is intended to shunt high-frequency noise currents from the I/O lines to the reference structure. However, fabrication techniques typically define a minimum separation between a capacitor and the signal conductor or reference conductor, which results in a parasitic inductance. In this design, the parasitic inductance associated with the current flowing in the part of the circuit where the 10-ohm resistor works to our advantage allowing us to achieve a 40-dB/decade roll off above the cut-off frequency. However the parasitic inductance associated with the current flowing through the capacitors limits the amount of high-frequency current that can be shunted by these capacitors. Thus, the parasitic inductance limits the frequency range over which the capacitor is effective.

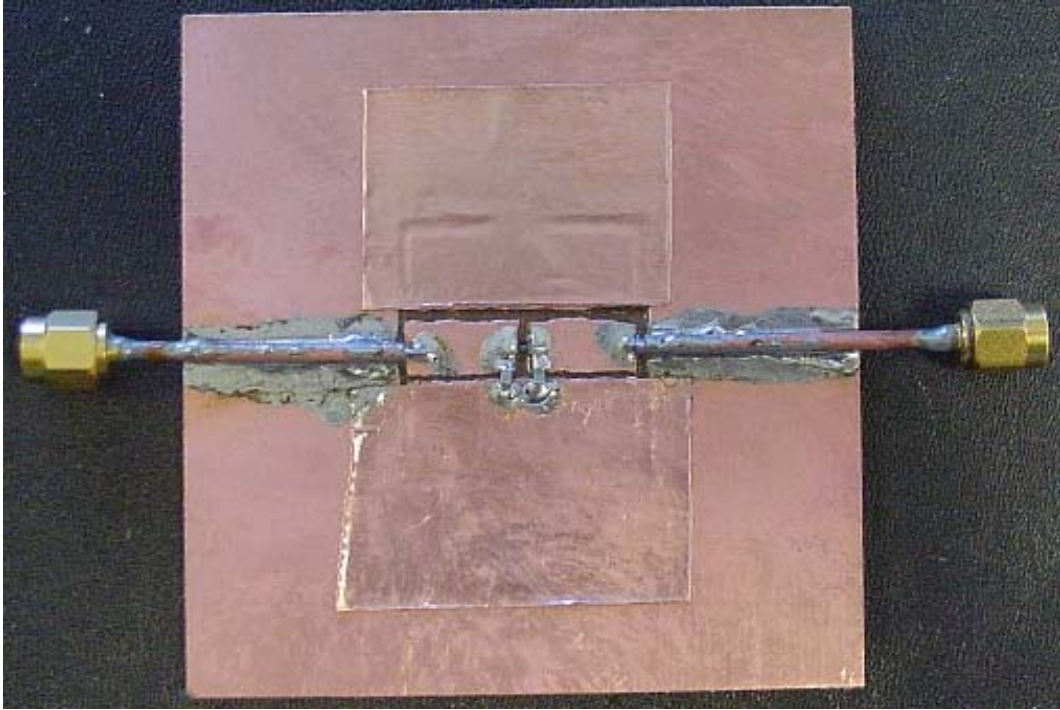
This experiment involves the construction of a low-pass pi-filter that has a cut-off frequency of 100 MHz and is effective to 1 GHz. Figure 1 shows a schematic of the experimental setup. The 50- $\Omega$  ports of the network analyzer will provide the source and load impedances.



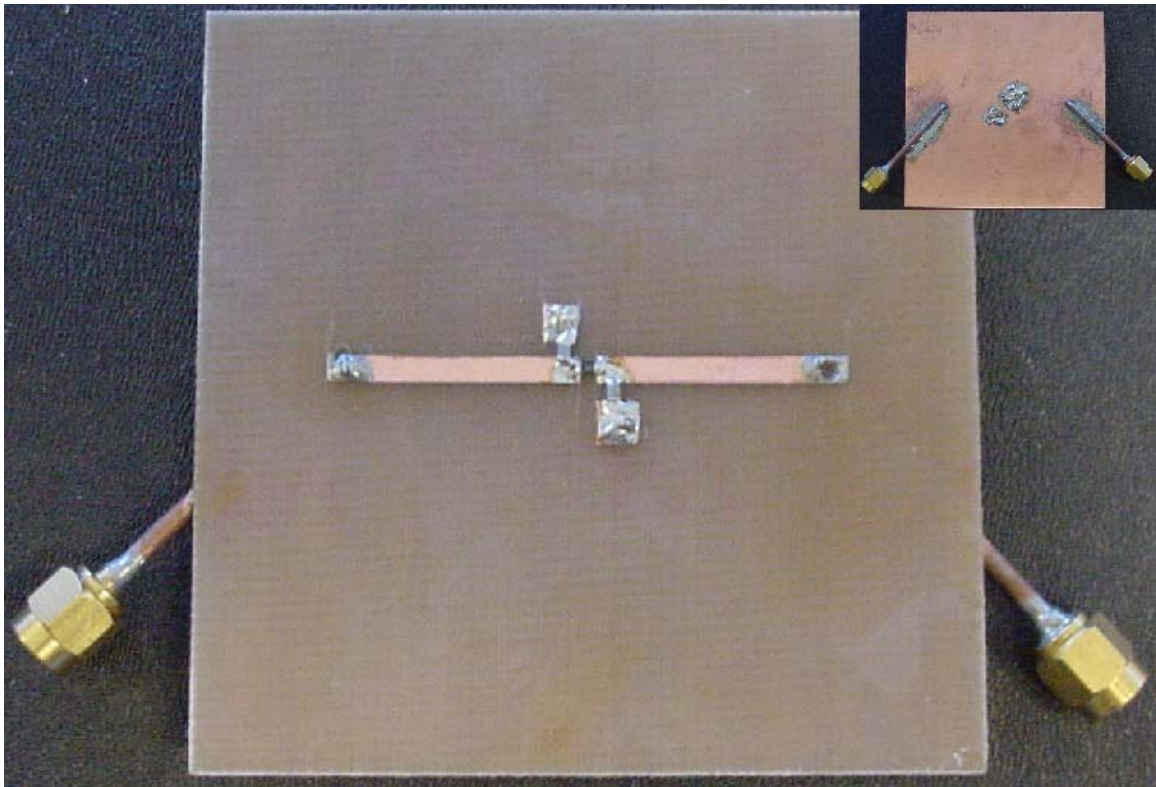
**Figure 1. Schematic of a low-pass pi-filter with the network analyzer connections**

#### 4. Experimental Descriptions

1. Build a single-layer low-pass Pi-filter circuit. Figures 2 and 3 show two unique implementations of the Pi-filter.
  - a. Cut away unwanted copper from one side of the 3" x 3" copper-clad board using a utility knife.
  - b. Solder each of the SMA probes onto the board.
  - c. Mount the SMT resistor and capacitor.
2. Measure the insertion loss with the HP8753D Network Analyzer. The insertion loss for the filters in Figure 2 and 3 is shown in Figure 4.
  - a. Is the response that of a low-pass filter?
  - b. Where are the problems, and what must be done to correct the filter?
  - c. Plot the results.
3. Build an improved filter on the other side of the 3" x 3" copper-clad board.
  - a. Remove the components and probes from the board, and turn the board over.
  - b. Mount the SMA probes on the board.
  - c. Copper-tape may be used to build a two-layer board (suggested) to reduce the effects of the parasitics.
  - d. Mount the components.
4. Measure the insertion loss again with the HP8753D Network Analyzer.
  - a. Now, does the response match that of a low-pass filter?
  - b. Is the cut-off frequency still close to 100 MHz?
  - c. Plot the results.
5. Return to step 3, and try again if necessary.



**Figure 2: One-sided implementation of the Pi-filter**



**Figure 3: Two-sided implementation of the Pi-filter. Note that the current return is carried on the back side of the board.**

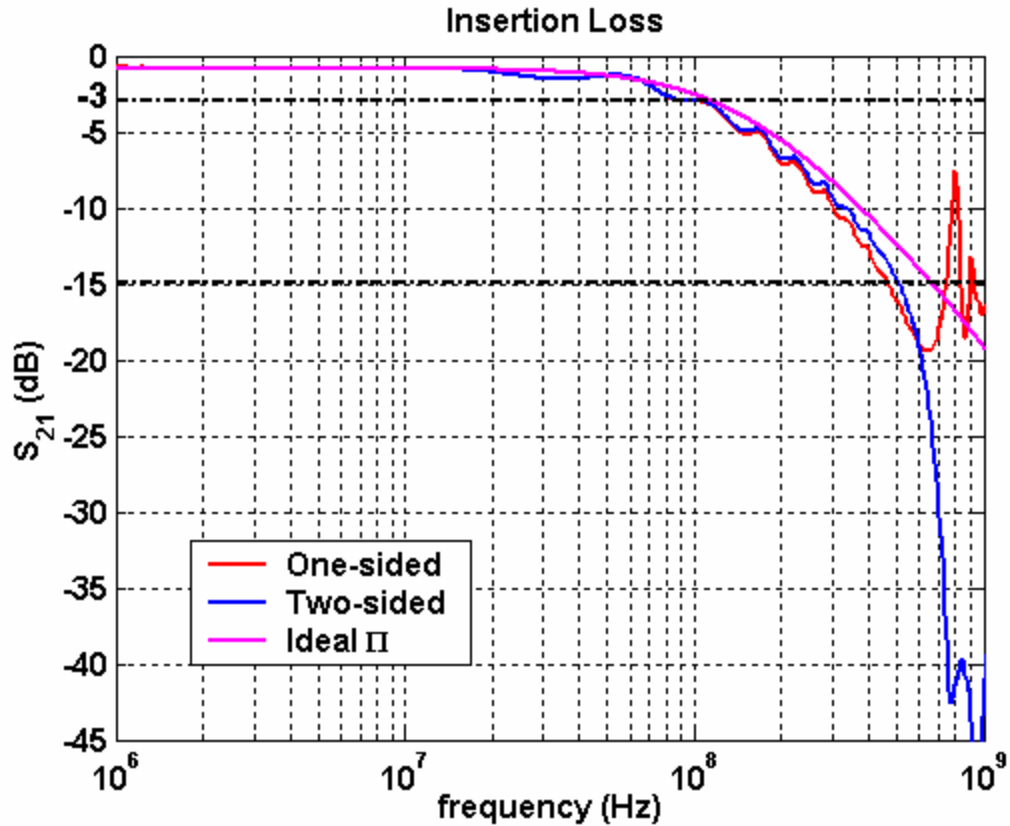


Figure 4: Insertion loss for the two filter designs

### 5. Topics for Discussion

Given the difficulty in constructing a discrete-element filter, what else can be done to reduce high-frequency signals from being conducted on I/O lines? What parasitics may be important at even higher frequencies above 1 GHz?

In Figure 4, the one-sided filter falls off just as the two-sided filter does, but the one-sided filter resonates and ceases to filter effectively for higher frequencies. When viewing the insertion loss up to 3 GHz in Figure 5, the two-sided filter also resonates and loses its effectiveness. Why might the two-sided filter perform better? What could be done to the two-sided filter to make it more effective at higher frequencies?

It is possible to build a one-sided board with better than 15 dB of attenuation up to 3 GHz. What additional measures might be necessary to achieve this performance?

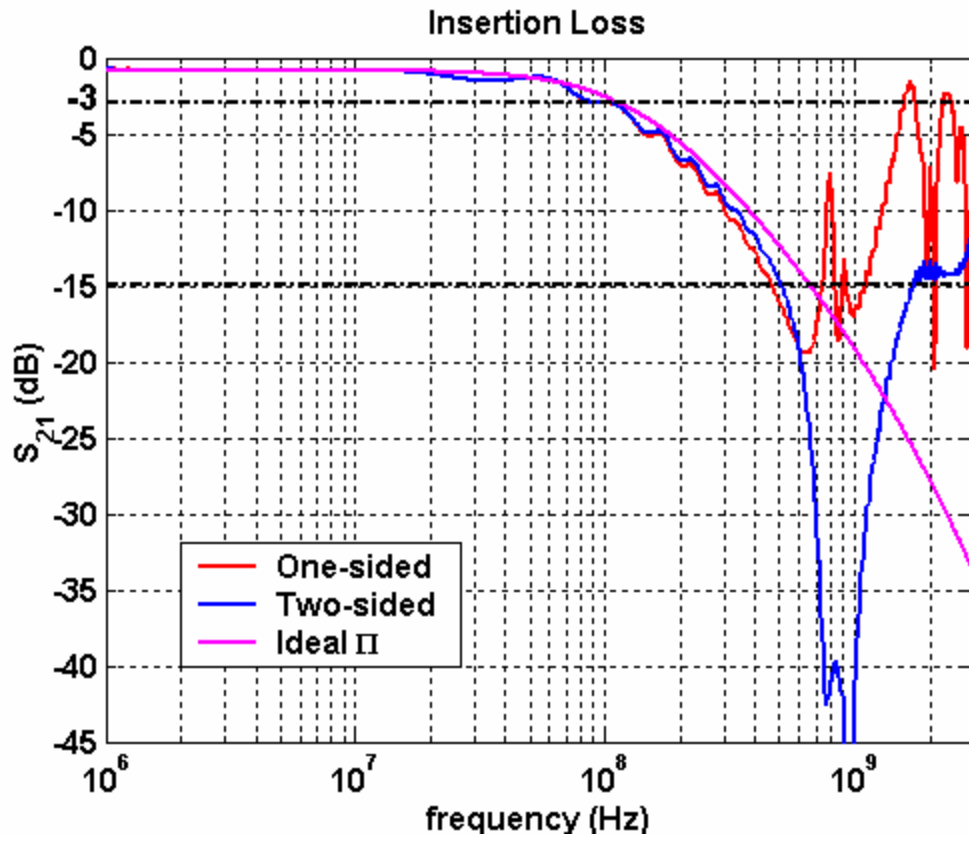


Figure 5: The insertion loss shown from 1 MHz to 3 GHz.