

Reducing the Price-Performance Ratio of 2G Wire

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Abstract—Broad commercial acceptance of HTS wire is expected to occur when the price-performance ratio approaches that of copper ranging from \$30-60/kA-m. The factors which directly influence the price-performance ratio are the electrical performance (I_c) and the cost to produce the wire. The electrical performance, as well as various wire-cost components, are intimately related so that they cannot be treated independently and they often must be traded-off to optimize the price-performance ratio. Some general aspects of the interactions between production rates, volume capacity and producing high ampacity wire are considered in this paper. These points will be illustrated by applying them to AMSC's approach to low-cost high-performance wire manufacturing using a RABiTS™/MOD process on wide strips. Opportunities for further improvement in price-performance reduction are also discussed.

I. INTRODUCTION

The price-performance ratio, defined in units of \$/kA-m, is the generally accepted measure by which the value proposition of HTS wire (or LTS wire for that matter) is evaluated. Achieving a price-performance ratio nearly equivalent to copper wire is particularly important for broad commercial market penetration in applications in which the HTS wire would simply replace copper. Higher price-performance ratios could be justified where the HTS wire offers significant additional functionality compared to copper.

Second generation (2G) wire provides the opportunity to lower the wire price-performance ratio beyond that of first generation (1G) wire and toward, or even below, that of copper, which is \$30-60/kA-m in typical cable applications. There are various 2G wire architectures being developed, but generally they are comprised of a metal substrate on ceramic (simple oxide) buffer layers to provide a textured template for epitaxial growth of the YBCO HTS layer. A thin silver cap layer is deposited on top of the HTS layer for passivation. A thicker metal stabilizing layer is then applied on both sides of the wire to achieve required electrical, thermal and mechanical properties. AMSC has chosen a RABiTS/MOD™ technology for manufacturing 2G wire because of its inherently low materials cost and its compatibility with processing in a wide strip format. The ability to manufacture 2G in a wide strip format and subsequently slit the wide strip into many narrower wires is a key aspect to high volume output and ultimately to low-cost wire. The basic architecture of AMSC's wire contains three thin buffer layers, each 75 nm thick, that are deposited onto a 75 μm Ni-W substrate to form the template [1]. The HTS layer deposited by slot-die coating is nominally 1 μm thick, as is the Ag passivation layer. The structure up to this point is presently processed as a 4-cm

wide strip then slit to several narrower width wires and laminated with metal foils such as copper, brass and stainless steel.

In the remainder of this paper, aspects that influence the price performance ratio are discussed in terms of cost-performance ratio defined here as the total cost to produce wire (in \$) divided by the net capacity (in kA-m).

II. TOTAL COST COMPONENTS

The production costs, aside from factory overhead, can be separated into three categories: raw materials and materials utilization, labor, and equipment capital costs.

Raw material costs depend on the price per unit volume determined by the marketplace and the volume of material in the wire (per meter). The cross-section of the wire is dominated by the substrate and metal stabilizer. The buffer layers are thin and are not a major factor in terms of materials cost. The trifluoroacetate salts (TFA) used to synthesize the MOD precursor are less complex than the chemicals used for CVD processes and ultimately will provide a significant cost-advantage. Although the volume fraction of the Ag passivation layer is small, it is an intrinsically expensive noble metal, but is required for processing compatibility reasons. There is little opportunity for savings in choosing alternative materials at this point for these components; so the focus should be on reducing the volume fraction of the substrate and Ag layer.

The development of a material to reduce the RABiTS substrate thickness must be accompanied by an increase in yield strength in order to maintain the same overall strength (tolerance to load) during processing. AMSC is presently developing a high strength composite substrate to reduce thickness. Naturally, the cost-savings from the reduction in thickness must outweigh any increase in the cost-to-manufacture the composite substrate. Although the Ag layer is on the order of 1 μm, it is deposited by magnetron sputtering, which intrinsically has limitations in making efficient use of the target material. Hence, further work at reducing the amount of Ag will be advantageous. However, it must be done with consideration to preserving the HTS layer when the metal stabilizer is applied, by either a solder-lamination process as used at AMSC or an alternative process such as electro-plating.

Labor costs can be minimized by automating equipment so that the process is not labor intensive and by maximizing the amount of wire produced per production run. AMSC has specified its furnaces so heat treatment processes run unattended after the reels have been loaded. The equipment has been designed to process wide strip up to 10-cm wide by one

kilometer long which would correspond to 20-23 km of wire after slitting to 4-mm width.

Optimizing capital investment on equipment with respect to capacity is critical to minimizing the depreciation costs, which must be amortized against the wire cost. The capacity is a function of the linespeed of the equipment and the number of parallel wires that can be processed through the equipment (the effects of machine maintenance time and set-up time will be discussed in the next section). Linespeed depends on the spatial extent of the processing zone and thus one must trade-off the incremental cost of lengthening the process zone with the enhancement in capacity while considering any additional impact on maintenance. AMSC has standardized production furnaces for heat treatment steps at 10 m length to boost linespeeds. In addition, for slower steps such as texture anneal and HTS decomposition, the furnaces are equipped with three parallel processing chambers for concurrent handling of three wide strips. The increase in capacity provided by the additional process chambers outweighs the incremental capital cost.

III. NET CAPACITY

The net capacity in kA-m can be considered in terms of $I_c * v * T_{op} * Y$, where I_c is the critical current of the strip, v is the linespeed of the slowest process step, T_{op} is the total operation time, and Y is the yield for the entire manufacturing process. These four parameters have the largest impact on the net capacity, and ultimately, on the price-performance ratio. Although yield is very important, it is very process- and equipment-specific and will not be treated here.

Let's consider some of these factors for the HTS layer first. The I_c can be written as $J_c * w * t$ where J_c is the critical current density, w is the width of the strip and t is the thickness of the HTS layer. One desires to grow thick HTS layers with high J_c over a wide width to maximize the I_c per production pass and to do so without sacrificing one of the other parameters. The MOD process for the HTS layer was chosen because the HTS layer can be deposited over large widths. J_c 's for such films are in the 3.5 MA/cm² range and although template texture is sharp, further improvement in template texture to push up J_c should translate into an increase in net capacity (in kA-m) as long as it does not impact the limiting production rate. There is generally a trade-off between thickness and linespeed for a given process zone as determined by the fundamental growth, conversion or deposition rate. In addition, there are process dependent limitations in thickness. Multiple passes/coatings are used to push the thickness up but they do so at the expense of linespeed, effectively reducing it proportionally to the number of passes. As an example, the thickness of the HTS layer for AMSC's MOD coatings for a single manufacturing pass is limited to nominally 1.0 μ m by the formation of cracks accompanying the large volume contraction that occurs during the decomposition step. To overcome this limit, a double-coat process was developed in which the strip is processed through HTS coating and decomposition twice before it is reacted [2]. It is clearly more

advantageous to push the thickness up with a single layer, as it reduces the demand on the decomposition furnace (i.e. has less impact on the effective linespeed) which is already one of the slowest processing steps and because there is no potentially deleterious effect of the interface layer between coatings. Thus, one of the major areas for further opportunity is enhancing the thickness limit imposed at decomposition. We have already demonstrated a significant increase in decomposed thickness beyond that used for our baseline process producing a 0.8 μ m thick HTS layer. This increased thickness will enable higher I_c films to be produced without a significant reduction in linespeed. We expect the effect on T_{op} when increasing thickness to be minimal given our choice of slot die coating followed by decomposition and reaction heat treatments. This impact is much less significant than for example, in a vapor deposition process where coatings are deposited in chambers requiring more preventive maintenance. The point here is that one cannot consider the increases in I_c achieved by thicker HTS coating without its impact on linespeed and operation time.

Buffer layers are predominantly deposited at AMSC and elsewhere by physical vapor deposition. It is well-known that vapor deposition systems require a significant amount of preventive maintenance (PM) and set-up time because of the high vacuum requirements and build-up of material on chamber walls. Development of a liquid phase epitaxial technique would be advantageous as it would obviate the high vacuum environment and require less PM. AMSC is presently working with collaborators at ORNL to develop a MOD-based buffer stack [3]. The development of such a process would require coating and decomposition equipment similar to that presently being used on the production line for the HTS layer. We have found the processing times to be very low (i.e. high linespeeds should be achievable) and expect there to be significant savings in capital expense for future capacity expansion.

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