

## Activities of the FLUXONICS Society

F.H. Uhlmann and T. Ortlepp

Ilmenau University of Technology, Institute of Information Technology  
P.O. Box 100 565, D-98684 Ilmenau, Germany  
[thomas.ortlepp@tu-ilmenau.de](mailto:thomas.ortlepp@tu-ilmenau.de)

**Abstract** – We offer a brief overview of activities of the FLUXONICS Society, from its inception to the present status. Its overall goal is to stimulate the development of digital superconducting electronics in Europe. Its main activities are: (1) professional education through RSFQ Workshops, (2) development and maintenance of RSFQ cell library, (3) technical forecasting via a roadmap, and (4) linkage of and to European centers for superconducting low-temperature electronics, and the operation of FLUXONICS Foundry.

Manuscript received January 11, 2008; accepted January 17, 2008. Reference No. RN4; Category 4.

Keywords: Digital electronics, foundry, high speed processing, , Josephson junction, roadmap, single flux quantum.

### I. INTRODUCTION

The origins of FLUXONICS go back to the now terminated European Network for Superconductivity (SCENET), which was supported by European Commission until July 2006. As an initiative of the SCENET working group “Superconducting Electronics”, the non-profit Society FLUXONICS e.V. was officially founded on May 31, 2001, with the aim to provide a dynamic platform coordinating European activities in Superconducting Electronics (SE) [1], and especially rapid digital single flux quantum (RSFQ) electronics [2]. Since that time, the activities of the Society developed gradually, and assumed an important nurturing role since the termination of SCENET. Today, the main activities are: (1) professional education through biannual (now annual) RSFQ Workshops, (2) development and maintenance of RSFQ cell library, (3) technical forecasting via a periodically updated roadmap, (4) linkage of and to European fabrication and testing centers for low-temperature superconducting electronics. As a major outcome of the FLUXONICS efforts, an European circuit foundry for SE was established [3], a cell library was developed and made available [4], and the first European roadmap was drawn up for this field [5]. The FLUXONICS Foundry offers complex low temperature superconducting circuit fabrication, has ISO 9001 certification, and successfully performed numerous production runs.

Members of FLUXONICS e.V. are University of Twente (UT) in the Netherlands, Institute of Photonic Technology (IPHT), Ilmenau University of Technology (TUIL), Physikalisch Technische Bundesanstalt (PTB) and University of Karlsruhe (UniKarl) in Germany, University of Chalmers (UChal) in Sweden, University of Savoie (USavoie) and CEA Grenoble in France, National Research Center (CNR) in Italy, and University of Cambridge (UCam) in United Kingdom.

The overall goal of the Society is to stimulate the development of digital superconducting electronics technology in Europe to attain performance beyond the possibilities of semiconductor circuit technologies.



Fig. 1. Locations of FLUXONICS members in Europe symbolized by their logos.

## II. THE RSFQ WORKSHOP

The acronym RSFQ (rapid single flux quantum) was coined by Likharev, Semenov and Mukhanov, who first proposed this particular embodiment of SFQ [2]. Under the leadership of F.H. Uhlmann, the FLUXONICS RSFQ design workshop was established in 2001 at the Ilmenau University of Technology, Germany, shortly after the foundation of FLUXONICS. Until 2007, the workshop has been held every two years. The 4<sup>th</sup> workshop took place on September 23<sup>th</sup> to 25<sup>th</sup>, 2007, in Ilmenau, Germany (see Forum [Highlight H18](#)). Each workshop included two parts: (1) training courses for integrated SE design and testing, and (2) individual contributions by each participant to special research topics.

The steadily increasing number of participants clearly shows the growing interest in design and simulation of superconducting digital electronics. The workshop assists joint efforts of European academic and industrial groups in the field by providing an educational opportunity for graduate students and engineering professionals.

The next workshop will be held June 29<sup>th</sup> to July 2<sup>nd</sup>, 2008, as usual in Ilmenau, Germany, thus switching to an annual cycle. The program of the 5<sup>th</sup> workshop will include the following topics:

- Lectures on superconductor electronics
- Introduction to digital circuit design
- Advanced aspects of RSFQ circuit design
- Application of active and passive phase shifting elements in RSFQ circuits
- High data-rate superconductor-to-semiconductor interface
- RSFQ circuits with reduced critical current density.

The workshop activity aims at strengthening the vital link between research and development groups and supporting education for all groups active in the field of RSFQ circuit design. We focus on training and knowledge dissemination to make SE technologies ready to benefit other technologies on the world markets and to bridge the gap between SE and other areas of electronics. Our objective is also to boost investigation activities in the field of digital SE. We believe that, in areas where it can be especially effective, this technology has a high potential for solving some bottlenecks in Moore's law already identified by the International Technology Roadmap for Semiconductors (ITRS) [6]. The attributes of digital SE are high speed, quantum accuracy and size-independent very low power dissipation. The workshop should inspire industrial interest and prepare interested industries for the

application of RSFQ as one of future electronic generations beyond the possibilities of current semiconductor circuit technologies.

### III. FLUXONICS Foundry

#### A. The Principle of Collaborative Foundry

The FLUXONICS Foundry is a collaborative effort, schematically illustrated in Fig. 2, to use the strength of each partner to form a complete European foundry for superconductor electronics. The objective is to develop, fabricate and test miscellaneous RSFQ circuits using the dedicated cell library created and maintained by the “RSFQ design group” of Ilmenau (TUIL). The fabrication activities are based on the technological process of the Institute of Photonic Technology (IPHT) located in Jena, Germany. Chips fabricated in Jena are tested at the Microwave and Characterization Laboratory of the University of Savoie, France.

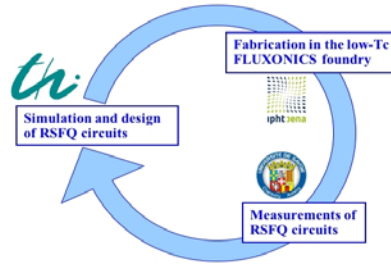


Fig. 2 Design, fabrication and test cycle of the FLUXONICS Foundry.

#### B. The Cell Library

At the present time a wide range of CAD tools are available to design semiconductor integrated circuits which incorporate many millions of transistors. However straightforward utilization of the semiconductor CAD tools for the design of RSFQ integrated circuits is difficult due to the following reasons:

- (1) Transient voltage pulses represent the data in RSFQ circuits.
- (2) Gate interaction is considerable, so that the propagation delay and the bias supply margin are strongly affected by neighbouring cells.
- (3) Josephson transmission lines required for the cell interconnection occupy large areas on the chip and cause large propagation delays. While microstriplines are possible to use for long interconnections, they are costly for short interconnections as they need additional impedance matching circuits.

Reason (2) makes the cell-based design approach difficult, and (3) prohibits to use the conventional automated placing and routing tools. We cannot utilize the semiconductor logic synthesis tools as they are for the RSFQ circuit systems, because circuit styles and the figures of merit for the optimization differ too much. Nevertheless, the cell-based design methodology employing simple one- or two-bit operations is the most promising technique for designing complex RSFQ circuits. The challenge in this field is to develop adequate design tools for the high speed SE as discussed in [7].

The FLUXONICS Foundry provides a circuit design kit, design support and a library of simple logic cells maintained at TUIL. The active element for circuit designs is the Josephson junction; [4] contains a design kit for a set of junctions with different parameters based on the design rule description of the foundry.

We were able to integrate our library elements *without further reoptimization* into small-scale circuits, and demonstrated the mature level of the library elements and of the cell-based design approach [8]. The further extension of the library, specific testing of reliability and yield, and the compilation of larger circuits are currently in progress. The University of Chalmers has developed its own specific cell library for the implementation of a complex digital signal processor for telecommunication purposes [9]. Other RSFQ cell libraries have been published by Stony Brook University, USA [10], by the National Institute of Advanced Industrial Science and Technology (AIST) in Japan [11], and (the most advanced) by the Superconductivity Research Laboratory (SRL) of the International Superconductivity Technology Center (ISTEC) in Japan [12].

### C. Fabrication

The FLUXONICS Foundry is based on a 1 kA/cm<sup>2</sup> Nb/Al-AlO<sub>x</sub>/Nb Josephson junction process at the Quantum Detection Department of the IPHT Jena. This 4 inch wafer production is ISO-9001:2000 certified and provides also a lower critical current density (200 A/cm<sup>2</sup>) which fulfils requirements for SQUID and radiation detector applications. The design rules *RSFQID* are available online [13].

The Foundry is the core element for the professional fabrication of digital SE in Europe. As already mentioned, the quality and reliability of this process has been proven in numerous fabrication runs within the last 7 years [8]. Future plans for technology improvements will replace the current standard contact lithography (2 μm linewidth) by a projection photolithography based on a 5:1 GCA i-line waferstepper (0.5 μm). This will make possible the fabrication of Josephson junctions with higher critical current densities. The process improvement is currently in progress. It should reduce the overlap between different layers from 2.5 μm down to 1 μm and the Josephson junction areas from 12.5 μm<sup>2</sup> down to below 1 μm<sup>2</sup>. The intended planarization technology (CMP) will also provide more than three Nb layers. An automatic test environment for the process characterisation is planned to improve the process monitoring and to reduce cycle times.

Similar capabilities for the production of low-temperature RSFQ circuits exist at Physikalisch Technische Bundesanstalt (PTB) in Braunschweig, Germany and at the Technical Research Centre of Finland (VTT). Besides the advanced low-temperature Nb-based process, other FLUXONICS members are investigating new materials and novel fabrication techniques. The promising combination of both low- and high-temperature superconductors is studied at the University of Twente to demonstrate the new technique of applying the d-wave symmetry HTS materials in RSFQ circuits [14]. The CEA Grenoble is developing a niobium nitride (NbN) multilayer process for RSFQ applications operating at temperature above 10 K [15]. The implementation of a ferromagnetic barrier material (SFS) for intrinsic π-Josephson junctions is studied at the University of Cambridge, University of Birmingham and University of Karlsruhe.

### D. Circuit Testing

Extensive tests of all circuit elements are performed to provide a base for the next revision of our cell library. In addition to testing the logic functionality of implemented digital devices, we developed a fully automatic test environment for advanced circuit analysis based on multiple bit patterns and long data streams to evaluate the bit error rate. The advanced circuit analysis is needed to qualify these with regard to the most serious issues in the design of complex RSFQ circuits: (1) current distribution and related magnetic fields; (2) flux trapping into the active circuit structures, and (3) magnetic and microwave shielding against the background of data links at microwave speed. Our work aims at the improvement of the current setup towards a higher immunity against environmental noise and a better reliability of the entire superconducting electronic system.

Most of the tests to date are performed in liquid helium cryostats. However, significant progress has been made recently in the field of small cryogenic coolers

(microcoolers) for low temperatures. Therefore, the current interest within FLUXONICS is turning to the implementation of SE with such cryocoolers. Recent progress in this field will be reviewed at the first internal Microcooling Workshop of “S-Pulse”, April 7<sup>th</sup> and 8<sup>th</sup>, 2008, at Twente University\*.

#### IV. THE ROADMAP

Superconducting analog to digital converters [16], network switches [17] and microprocessor prototypes [18] are the first demonstrated digital systems based on RSFQ technology. These applications of SE operate at very high speed with a typical clock frequency of about 20 GHz and very low power consumption. Three general issues are today the most important show stoppers for the industrial application of SE. One system design challenge is the data interface from RSFQ to CMOS electronics. The data rate can be reduced by using serial-to-parallel converters, as for the ADC system developed by Hypres Inc. [19, 16] and by the Advanced Research Laboratory of Hitachi Ltd. [20], but this increases the system complexity significantly. The second main issue is the device density on chip, which is currently limited to about 20.000 Josephson junctions. This limit is caused by three different reasons: (1) the density of defect junctions even for the most advanced process in Japan is about one out of 20.000 [21], (2) a chip of this size consumes about one ampere supply current; the related magnetic field penetrates the circuit and causes a shift of the operational margins (larger currents cause even malfunction), (3) the feature size of Josephson junctions and interconnects is today above 1 $\mu$ m, but physical limits become serious soon below this value. The third main issue is the memory bottleneck, since no dense RSFQ memory is available. The interfacing of conventional CMOS memory is possible in general [22], but it limits the clock speed significantly to values of about 1 GHz. Only a massive parallel interface as proposed for the DSP system of the University of Chalmers could provide a higher data rate.

Within the FLUXONICS network, we keep track on all the European and international developments in the field to provide a scientific and technological assesment of progress in SE. The results by 2005 were collected and published in the SCENET Roadmap for Superconducting Electronics [5]. The next actualization of this document should lead to a new roadmap in early 2009.

#### V. FUTURE PERSPECTIVES

The recently launched European FP7 project “S-PULSE” (see Forum Announcement [A24](#)) will support and extend the FLUXONICS activities presented above. The overall goal is to prepare digital SE technologies for the technology generation beyond the CMOS scaling limits. To exploit the potential of SE for the future information and communication society, it is important to strengthen the technical and economical impact of superconducting technologies in Europe. The “S-PULSE” should help supporting joint efforts of European academic and industrial groups in the superconducting technologies field. Through the exchange of knowledge and ideas, systematic education, *etc.*, it should strengthen the vital link between research and development on the one hand and the industrial perspective on the other hand, thus bringing together realistic industrial expectations and visionary extrapolations of the current status of technology. This should improve the image of SE, win public interest, and increase chances for practical applications of SE technology where these could be especially effective in eliminating the bottlenecks already identified by ITRS. The RSFQ technology does not offer a universal solution of all problems of CMOS electronics. For example, it doesn’t readily offer very large scale integration. However, it has a high

---

\* This internal Workshop will be by invitations only. Those interested may contact Prof. Marcel ter Brake: [h.j.m.terbrake@utwente.nl](mailto:h.j.m.terbrake@utwente.nl).

potential for solving some of the problems through its high speed, quantum accuracy and size-independent very low power dissipation. No other thin-film technology can handle multigigahertz clock-frequencies with a low-cost metal process and a moderate feature size.

Within the project, we will continue to focus on training and dissemination activities, and on the development of an elaborate short- and long-term roadmap and definition of research strategy towards the assessment for applications possibly impacting on the future of electronics. In order to define the research strategy, we propose to study the ultimate limits for SE in terms of minimum feature size and identify the challenges to reach these limits. Current research in this field will benefit significantly from a clear definition of technological challenges and limits. For the time being, the interest of related industries is still low, but a particular objective of the “S- PULSE” project is to bridge the gap between SE and other areas of electronics.

Also within the project, architecture issues in general circuit design will be addressed, taking into account the increasing complexity, the need for fault tolerance and the information propagation time in ultra-high speed systems. The knowledge of downscaling limits and performance for high-speed routing and computing based on superconducting electronics will enable the community to identify the new qualities of SE, and hopefully promote further funding of technological innovation in the field of electronics. Its objective is to support the development of the most promising superconducting technologies in a coherent and compatible way contributing to the future in high-speed digital data processing.

The most promising areas where our approach should take advantage of its performance edge, in conjunction with integrating hitherto “competing” technologies (superconductor *versus* semiconductor), include hybrid circuits for high-rate digital data processing in ground- and space-based communication systems, software defined radio, ultra high-speed signal processing, measuring equipment for non-destructive testing, medical applications, precision measurements (arbitrary waveform generation), new computing principles, and sensitive detectors (with mixers and local oscillators included). These developments will be synchronized and coordinated by joining the expertise of several complementary domains: superconducting high-speed electronics, high-speed semiconductor circuits (InP and CMOS), microwave systems, packaging and cryogenics. We expect S-PULSE to structure the R&D resources and skills in the area of superconductor technologies existing in Europe.

## REFERENCES

- [1] <http://www.fluxonics.org>
- [2] K. K. Likharev et al., “RSFQ Logic/Memory Family: A New Josephson-Junction Technology for Sub-Terahertz-Clock-Frequency Digital Systems”, *IEEE Trans. Appl. Superconductivity* **1**, no. 13-27 (1991).
- [3] <http://www.fluxonics-foundry.de>
- [4] [http://www4.tu-ilmeneau.de/EI/ATE/kryo/cell\\_library/index.htm](http://www4.tu-ilmeneau.de/EI/ATE/kryo/cell_library/index.htm)
- [5] M. TerBrake et al., “SCENET Roadmap for Superconductor Digital Electronics”, *Physica C* **439**, 1-42, 2006.
- [6] ITRS, [http://www.itrs.net/Links/2004Update/2004\\_05\\_ERD.pdf](http://www.itrs.net/Links/2004Update/2004_05_ERD.pdf)
- [7] K. Gaj et al., “Toward a systematic design methodology for large multigigahertz rapid single flux quantum circuits”, *IEEE Trans. Appl. Superconductivity* **9**, no. 3, 4591-4606 (1999).
- [8] J. Kunert et al., “Design, Fabrication, and Tests of RSFQ Circuits based on the FLUXONICS Foundry”, 8<sup>th</sup> European Conference on Applied Superconductivity (EUCAS), Brussels, September 16<sup>th</sup> – 20<sup>th</sup> 2007 (unpublished).
- [9] I. Kataeva et al., “Scalable Matrix Multiplication With Hybrid CMOS-RSFQ Digital Signal Processor”, *IEEE Trans. Appl. Superconductivity* **17**, no. 2, 486-489 (2007).
- [10] P. Bunyk et al. “RSFQ cell library”, Technical Report 15, SUNY at Stony Brook, <http://pavel.physics.sunysb.edu/RSFQ/publication.html>, May 1999.
- [11] M. Maezawa et al., “Design and fabrication of RSFQ cell library for middle-scale applications”, *Physica C* **412-414**, 1591-1596 (2004).

- [12] S. Yorozu *et al.* "A single flux quantum standard logic cell library", *Physica C* **378-381**, 1471-1474 (2002).
- [13] <http://www.ipht-jena.de>
- [14] T. Ortlepp *et al.*, "Flip-Flopping Fractional Flux Quanta", *Science* **312**, 1495-1497 (June 9, 2006).
- [15] E. Baggetta *et al.*, "New design and implementation of a fast modulator in NbN technology", *IEEE Trans. Appl. Superconductivity*, **15**, no. 2, 453-456 (2005).
- [16] D. Gupta *et al.*, "Digital Channelizing Radio Frequency Receiver", *IEEE Trans. Appl. Superconductivity* **17**, no. 2, 430-437 (2007).
- [17] Y. Hashimoto *et al.*, "Implementation and Experimental Evaluation of a Cryocooled System Prototype for High-throughput SFQ Digital Applications", *IEEE Trans. Appl. Superconductivity*, **17**, no. 2, 546-551 (2007).
- [18] Y. Yamanashi *et al.*, "Design and Implementation of a Pipelined Bit-Serial SFQ Microprocessor, CORE1 $\beta$ ", *IEEE Trans. Appl. Superconductivity* **17**, no. 2, 474-477 (2007).
- [19] Design rules of the Hypres Inc. available online at <http://www.hypres.com>
- [20] F. Futura and K. Saitoh, "A Study for an Improved Design of Front-End Circuit of Superconducting Analog-to-Digital Converter", *IEEE Trans. Appl. Superconductivity* **15**, no. 2, 445-448 (2005).
- [21] H. Terai *et al.*, "Diagnostic Test of Large-Scale SFQ Shift Register", *IEEE Trans. Appl. Superconductivity* **17**, no. 2, 422-425 (2007).
- [22] Q. Liu *et al.*, "Latency and Power Measurements on a 64-kb Hybrid Josephson-CMOS Memory", *IEEE Trans. Appl. Superconductivity* **17**, no. 2, 526-529 (2007).