PCB Power Decoupling Myths Debunked

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Conventional Wisdom

- Need a variety of capacitance values to maintain low impedance over frequency range
- Many capacitors of one value is better than many values
- Place capacitors close to ICs as possible
- Location does not matter
- Spread capacitors over entire board
Power Plane Noise Control

“Ground Bounce”
What is Capacitance?

Capacitance is the ability of a structure to hold charge (electrons) for a given voltage.

\[ C = \frac{Q}{V} \]

\[ Q = CV \]

Note: Capacitance has no frequency dependence!

Amount of charge stored is dependant on the size of the capacitance (and voltage).
High Frequency Capacitors

• Myth or Fact?

It’s really the inductance that matters!
Capacitance and Inductance

- **Capacitance** → amount of charge stored
- **Inductance** → speed that the charge can be delivered from capacitor
Decoupling Capacitor Mounting

• Keep as to planes as close to capacitor pads as possible
0603 Size Cap Typical Mounting

*Note: Minimum distance is 10 mils but more typical distance is 20 mils.
0402 Size Cap Typical Mounting

*Note: Minimum distance is 10 mils but more typical distance is 20 mils.
# Connection Inductance for Typical Capacitor Configurations

Configurations with 10 mils from Capacitor Pad to Via Pad

<table>
<thead>
<tr>
<th>Distance into board to planes (mils)</th>
<th>0805 typical (148 mils between via barrels)</th>
<th>0603 typical (128 mils between via barrels)</th>
<th>0402 typical (106 mils between via barrels)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1.2 nH</td>
<td>1.1 nH</td>
<td>0.9 nH</td>
</tr>
<tr>
<td>20</td>
<td>1.8 nH</td>
<td>1.6 nH</td>
<td>1.3 nH</td>
</tr>
<tr>
<td>30</td>
<td>2.2 nH</td>
<td>1.9 nH</td>
<td>1.6 nH</td>
</tr>
<tr>
<td>40</td>
<td>2.5 nH</td>
<td>2.2 nH</td>
<td>1.9 nH</td>
</tr>
<tr>
<td>50</td>
<td>2.8 nH</td>
<td>2.5 nH</td>
<td>2.1 nH</td>
</tr>
<tr>
<td>60</td>
<td>3.1 nH</td>
<td>2.7 nH</td>
<td>2.3 nH</td>
</tr>
<tr>
<td>70</td>
<td>3.4 nH</td>
<td>3.0 nH</td>
<td>2.6 nH</td>
</tr>
<tr>
<td>80</td>
<td>3.6 nH</td>
<td>3.2 nH</td>
<td>2.8 nH</td>
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<tr>
<td>90</td>
<td>3.9 nH</td>
<td>3.5 nH</td>
<td>3.0 nH</td>
</tr>
<tr>
<td>100</td>
<td>4.2 nH</td>
<td>3.7 nH</td>
<td>3.2 nH</td>
</tr>
</tbody>
</table>
## Connection Inductance for Typical Capacitor Configurations with 50 mils from Capacitor Pad to Via Pad

<table>
<thead>
<tr>
<th>Distance into board to planes (mils)</th>
<th>0805 (208 mils between via barrels)</th>
<th>0603 (188 mils between via barrels)</th>
<th>0402 (166 mils between via barrels)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1.7 nH</td>
<td>1.6 nH</td>
<td>1.4 nH</td>
</tr>
<tr>
<td>20</td>
<td>2.5 nH</td>
<td>2.3 nH</td>
<td>2.0 nH</td>
</tr>
<tr>
<td>30</td>
<td>3.0 nH</td>
<td>2.8 nH</td>
<td>2.5 nH</td>
</tr>
<tr>
<td>40</td>
<td>3.5 nH</td>
<td>3.2 nH</td>
<td>2.8 nH</td>
</tr>
<tr>
<td>50</td>
<td>3.9 nH</td>
<td>3.5 nH</td>
<td>3.1 nH</td>
</tr>
<tr>
<td>60</td>
<td>4.2 nH</td>
<td>3.9 nH</td>
<td>3.5 nH</td>
</tr>
<tr>
<td>70</td>
<td>4.5 nH</td>
<td>4.2 nH</td>
<td>3.7 nH</td>
</tr>
<tr>
<td>80</td>
<td>4.9 nH</td>
<td>4.5 nH</td>
<td>4.0 nH</td>
</tr>
<tr>
<td>90</td>
<td>5.2 nH</td>
<td>4.7 nH</td>
<td>4.3 nH</td>
</tr>
<tr>
<td>100</td>
<td>5.5 nH</td>
<td>5.0 nH</td>
<td>4.6 nH</td>
</tr>
</tbody>
</table>
Via Configuration Can Change Inductance

The “Good”

The “Bad”

The “Ugly”

Really “Ugly”
Comparison of Decoupling Capacitor Via Separation Distance Effects

0.1 uF Capacitor

<table>
<thead>
<tr>
<th>Via separation, mils</th>
<th>Inductance, nH</th>
<th>Impedance @1 GHz, Ohms</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0.06</td>
<td>0.41</td>
</tr>
<tr>
<td>40</td>
<td>0.21</td>
<td>1.3</td>
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<tr>
<td>60</td>
<td>0.36</td>
<td>2.33</td>
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<tr>
<td>80</td>
<td>0.5</td>
<td>3.1</td>
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<tr>
<td>100</td>
<td>0.64</td>
<td>4.0</td>
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<tr>
<td>150</td>
<td>1.0</td>
<td>6.23</td>
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<tr>
<td>200</td>
<td>1.4</td>
<td>8.5</td>
</tr>
<tr>
<td>300</td>
<td>2.1</td>
<td>12.7</td>
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<tr>
<td>400</td>
<td>2.75</td>
<td>17.3</td>
</tr>
<tr>
<td>500</td>
<td>3.5</td>
<td>21.7</td>
</tr>
</tbody>
</table>
Example #1
Low Cap Connection Inductance
Example #2
Hi Cap Connection Inductance

IC
Cap

PCB

PWR
GND
Example #3
Lower Cap Connection Inductance

IC
PWR
GND
Cap
PCB
Example #4
High Cap Connection Inductance

PCB
IC
Cap
PWR
GND
Capacitor Connection Inductance Ratio

For local decoupling need $L3/L2 < 3$

<table>
<thead>
<tr>
<th>Power/GND plane spacing, (mils)</th>
<th>via diameter, (mils)</th>
<th>$L2$ (nH)</th>
<th>62mil brd centered plane spacing, mils</th>
<th>0603 SMT L3’ (nH)</th>
<th>L3/L2 w/extra 100 mil trace length</th>
<th>L3/L2 w/extra 200 mil trace length</th>
<th>L3/L2 w/extra 300 mil trace length</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>10</td>
<td>0.32</td>
<td>10</td>
<td>1.66</td>
<td>6.75</td>
<td>9.13</td>
<td>11.50</td>
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<tr>
<td>10</td>
<td>13</td>
<td>0.304</td>
<td>35</td>
<td>0.92</td>
<td>1.29</td>
<td>1.98</td>
<td>2.67</td>
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<tr>
<td>10</td>
<td>25</td>
<td>0.27</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>35</td>
<td>10</td>
<td>1.1</td>
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<tr>
<td>35</td>
<td>25</td>
<td>0.95</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Decoupling Must be Analyzed in Different Ways for Different Functions

- EMC
  - Resonance big concern
  - Requires STEADY-STATE analysis
    - Frequency Domain
  - Transfer function analysis
    - Eliminate noise along edge of board due to ASIC/IC located far away
Decoupling Must be Analyzed in Different Ways for Different Functions

• Provide Charge to ASIC/IC
  – Requires time-limited analysis
    • Charge must get to the IC *during the time it is needed*
  – Charge will NOT travel from far corners of the board fast enough
    – Local decoupling capacitors dominate
Decoupling Capacitor Mounting

- Keep as to planes as close to capacitor pads as possible
Current in IC During Logic Transitions (CMOS)

Current in IC During Logic Transitions (CMOS)

IC load

Vcc

switch

Vdc

IC driver

Vcc

charge

Z0, vp

GND

logic 0-1

shoot-thru current

logic 1-0

 Shoot-thru current

GND

Drivers with shoot-through current: IC load

Vcc

logic 0-1

Shoot-thru current

logic 1-0

Discharge, IC load
Typical PCB Power Delivery
Equivalent Circuit for Power Current Delivery to IC

- Connector and wiring
- Capacitor leads
- Via interconnect
- Distance inductance
- PCB wiring
- IC load
- DC/DC converter
- Electrolytic capacitors
- SMT capacitors
- V_{CC}/GND plane

- \( L_{ps} \)
- \( L_{bulk} \)
- \( L_{via} \)
- \( C_{bulk} \)
- \( C_{SMT} \)
- \( C_{planes} \)
Power Bus Charging Hierarchy

100’s uF  0.01-100’s uF  pF’s-100 nF
SLOW       POKEY       QUICK       FASTEST

HUGE  BIG  SMALL  TINY
L_{ps}  L_{bulk}  L_{via}  L_{planes}  L_{trace}
Traditional Analysis #1

• Use impedance of capacitors in parallel

No Effect of Distance Between Capacitors and IC Included!
Traditional Impedance Calculation
for Four Decoupling Capacitor Values

Impedance (ohms)

Frequency (Hz)

.1uF
.01uF
.001uF
.0001uF
All in Parallel

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Traditional Analysis #2

• Calculate loop area – Traditional loop Inductance formulas
  – Which loop area? Which size conductor

Over Estimates L and Ignores Distributed Capacitance
More Accurate Model Includes Distributed Capacitance
Distributed Capacitance Schematic

\[ L = \text{Loop } L + \text{ESL}, \text{ but Loop } L \text{ dominates} \]
Effect of Distributed Capacitance

- Can NOT be calculated/estimated using traditional capacitance equation – need to use full-wave technique
- Displacement current amplitude changes with position and distance from the source
Sample Parameters for Comparison to Measurements

- Dielectric thickness = 35 mils
- Dielectric constant = 4.5, Loss tan = 0.02
- Copper conductivity = 5.8 e7 S/m
Impedance at Port #1
Single 0.01 uF Capacitor at Various Distances (35mil Dielectric)
Z11 Phase Comparison as Capacitor distance Varies for 35 mils FR4
ESL = 0.5nH

Frequency (Hz) vs. Phase (rad) for different Capacitor distances:
- 100 mils
- 200 mils
- 300 mils
- 400 mils
- 1000 mils
- 2000 mils

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Impedance at Port #1
Single 0.01 uF Capacitor at Various Distances (10mil Dielectric)

Frequency (Hz)
Impedance (dBohms)

-50 -40 -30 -20 -10 0 10 20
1.0E+07 1.0E+08 1.0E+09 1.0E+10

no caps
300 mils
500 mils
700 mils
1000 mils

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Effect of Capacitor Value??

- Need enough charge to supply need
- Depends on connection inductance
Charge Depletion

- IC draws charge from planes
- Capacitors will re-charge planes
  - Location \textit{does} matter!
Model for Plane Recharge Investigations

Port 2 represents IC current draw

Decoupling Capacitor:
C = 1μF
ESR = 30mOhm
ESL = 0.5nH

DC voltage used to charge the power plane

Port 2 represents IC current draw
Charge Between Planes vs. Charge Drawn by IC

Board total charge : $C \times V = 3.5\text{nF} \times 3.3\text{V} = 11\text{nC}$

Pulse charge 5A peak : $I \times dt/2 = (1\text{ns} \times 5\text{A})/2 = 2.5\text{nC}$
Charge Depletion vs. capacitor distance

![Graph showing voltage over time for different capacitor distances.](image)
Charge Depletion for Capacitor @ 400 mils for various connection Inductance
Noise Voltage is INDEPENDENT of Amount of Capacitance!

As long as there is ‘enough’ charge

Dist=400 mils
ESR=30mOhms
ESL=0.5nH
Capacitor Locations and Orientation

• Many myths about decoupling capacitor design
• Proximity between capacitors has been shown to impact capacitors’ performance
• Wish to quantify these various effects, not just show which is best
• Current (not voltage) important for decoupling capacitor analysis
What Happens if a 2nd Decoupling Capacitor is placed near the First Capacitor?

Via #1

Observation Point

distance

500 mils

Via #2 Moved in arc around Observation point while maintaining 500 mil distance to observation point
**Second Via Around a circle**

![Diagram of second via around a circle](image)

- $d_1 = R$
- $d_2 = 2R \sin \frac{\theta}{2}$

\[
\frac{\mu d}{4\pi} \ln\left(\frac{(R+r)^2(d_1+r)^2}{r^3(d_2+r)}\right) - \frac{\mu d}{4\pi} \ln\left(\frac{d_1+r}{R+r}\right) = \frac{\mu d}{4\pi} \ln\left(\frac{(R+r)^d}{(2R \sin(\theta / 2)+r)r^3}\right)
\]

- $R$: distance between Port 1 and Port 2 in mil
- $r$: radius for all ports in mil
- $d$: thickness of dielectric layer in mil
- $d1$: distance between Port 3 and Port 1 in mil
- $d2$: distance between Port 2 and Port 3 in mil
- $\theta$: angle as shown in the figure in degree

*Courtesy of Jingook Kim, Jun Fan, Jim Drewniak*

Missouri University of Science and Technology
Effective Inductance for Various Distances to Decoupling Capacitor
With Second Capacitor (Via) Equal Distance Around Circle
Plane Separation = 35 mil -- Via Diameter = 20 mil
Effective Inductance for Various Distances to Decoupling Capacitor
With Second Capacitor (Via) Equal Distance Around Circle
Plane Separation = 5 mil – Via Diameter = 20 mil
Understanding Inductance Effects and Proximity

1 via

2 via with degree 30°

2 via with degree 90°

2 via with degree 180°
Current Density - simulation

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DUT for Experimental Validation (Single Plane pair)

G-S probing port

Short Vias

\[ \theta = 0^\circ, 30^\circ, 180^\circ \]

G-S probing port

Shorting via

1 shorting

2 shorting with 30°

2 shorting with 180°
Experimental Validation (Single Plane Pair)

- Even in the case with two shorting vias at opposite sides ($\theta=180^\circ$), the inductance value is 68.8% of that with one shorting via.
- As two shorting vias get closer together, mutual inductance between two shorting vias increases.

Equation

$$
\frac{\mu d}{4\pi} \ln \left( \frac{(R + r)^4}{(2R \sin(\theta/2) + r)r^3} \right)
$$
Observations

• Added via (capacitor) does not lower effective inductance to 50%
  – 70-75% of original single via case

• Thicker dielectric results in higher inductance
Multiple Capacitors
**Via Spacing**

![Diagram showing via spacing with dimensions and distances labeled.]

<table>
<thead>
<tr>
<th>Distance to Planes (mils)</th>
<th>40 mil Spacing (nH)</th>
<th>0402 SMT (nH)</th>
<th>0603 SMT (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0.3</td>
<td>0.9</td>
<td>1.1</td>
</tr>
<tr>
<td>20</td>
<td>0.5</td>
<td>1.3</td>
<td>1.6</td>
</tr>
<tr>
<td>30</td>
<td>0.75</td>
<td>1.6</td>
<td>1.9</td>
</tr>
<tr>
<td>40</td>
<td>0.95</td>
<td>1.9</td>
<td>2.2</td>
</tr>
</tbody>
</table>

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Possible Configurations

- Dense, non-alternating
- Dense, alternating
- Spread, non-alternating
- Spread, alternating
Effective Inductance for 16 Decoupling Capacitors for Dense and Spread Configurations and Plane Pair Depth

- Dense Non-Alternating
- Dense Alternating
- Spread Non-Alternating
- Spread Alternating

Distance into PCB (mils)

Effective Inductance (pH)

40 mil via spacing
Number of Capacitors

- 1 cap
- 2 caps
- 4 caps
- 8 caps
- 16 decaps
Effective Inductance vs. Number of Capacitors and Plane Pair Depth

Effective Inductance (pH) vs. Distance into PCB (mils) for different numbers of capacitors:
- 1 Capacitor
- 2 Capacitors
- 4 Capacitors
- 8 Capacitors
- 16 Capacitors

40 mil via spacing

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Inductance vs. Plane Width

• Current tends to spread to minimize the impedance
• What is the effect of narrow power/ground planes?
• Using PowerPEEC in quasi-static inductance extraction mode
• Plane widths of 10”, 5”, 2” and 1”
• Distance between planes = 10 mils
Geometry

Solid Plane

‘Capacitor’ Port

‘IC’ Port (shorting via)

10 inches

12 inches

Top View

‘IC’ Port (shorting via)

‘Capacitor’ Port

Side View

10 mils
Table 1  Inductance as a Function of Plane Width

<table>
<thead>
<tr>
<th>Plane Width (inches)</th>
<th>Inductance (pH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>545</td>
</tr>
<tr>
<td>5</td>
<td>709</td>
</tr>
<tr>
<td>2</td>
<td>1352</td>
</tr>
<tr>
<td>1</td>
<td>2574</td>
</tr>
</tbody>
</table>
Effect of distance between Capacitor and IC

- Initially used 10” now use 2” and 1”
- Vary plane width as before
Table 2  Inductance as a Function of Plane Width

<table>
<thead>
<tr>
<th>Plane Width (inches)</th>
<th>Inductance (pH) (Distance=10&quot;)</th>
<th>Inductance (pH) (Distance=2&quot;)</th>
<th>Inductance (pH) (Distance=1&quot;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>545</td>
<td>173</td>
<td>154</td>
</tr>
<tr>
<td>5</td>
<td>709</td>
<td>178</td>
<td>156</td>
</tr>
<tr>
<td>2</td>
<td>1352</td>
<td>355</td>
<td>163</td>
</tr>
<tr>
<td>1</td>
<td>2574</td>
<td>658</td>
<td>240</td>
</tr>
</tbody>
</table>
Current Density

2" wide

5" wide

10" wide
Current Spread Comparison
Planes 5” Width

Distance = 10”

Distance = 1”
Really Ugly
From Actual PCB
Conclusions

- Inductance increases rapidly as plane width decreases
- Impact of plane width not as severe when capacitor and IC are close
- Should avoid all long thin power/ground structures
Summary

- Capacitance values should be as large as possible within the package size.
- In most cases, IC takes charge from between the plates, capacitors replenish that charge.
- Capacitors are better able to provide charge when spread out.
- If placed near each other, capacitors should alternate power/ground pins.
  - *Worst configuration* is when capacitors are close together and all pins in the same direction.
- When plane pair is deep in PCB stackup, effective inductance is higher.
Conventional Wisdom

- Need a variety of capacitance values to maintain low impedance over frequency range
- Many capacitors of one value is better than many values
- Place capacitors close to ICs as possible
- Location does not matter
- Spread capacitors over entire board
Backup
Modeling Technique

• Difficult to model many layer PCB with full wave models

• Multi-Via Transition Tool (MVTT)
  – Breaks multiple layers into individual via transitions
  – Cavity resonance technique to find impedance between planes
  – Capacitance calculation for via-to-plane effects
  – Concatenate S-parameters from all individual elements
Breaking the Problem

One via between a power plane: 2-port network
Via Configurations

Signal Via  |  GND Via
---|---
PWR Plane  |  PWR Plane

Signal Via  |  GND Via
---|---
GND Plane  |  PWR Plane

Signal Via  |  GND Via
---|---
GND Plane  |  GND Plane

S Top Port  |  S Bottom Port
G Top Port  |  G Bottom Port

Zpp

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