Embedded Capacitance
the Next Step in PWB Design

Collaboration that works...

...to create value

capture new markets

and expand your enterprise.

Presented by:
Richard Charbonneau & Charles Grasso

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Part I
Standard Practice for Selecting Decoupling Capacitors

an interactive discussion period

hosted by: Charles Grasso

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Decoupling Rules of Thumb* engineering dogma

use smallest chip you can

place as close to Vcc pins as possible

don't use Z5U

use 1 decoupler per Vcc pin

add cap close to ground pin

use .01uF

separate power

use 1 decoupler per pin

place decoupler under IC

don't use film caps

doesn't matter where cap is

.001uF work best

.1uF is preferred

X7R preferred

connect directly to Vcc and gnd

de-rate decouplers by factor of 2

ten-to-one rule

use redundant vias

tantalum is closest ideal

widen traces to decouplers

always use solid Vcc and ground plane

use 4 decouplers per IC

your rule here

always follow manufactures guidelines

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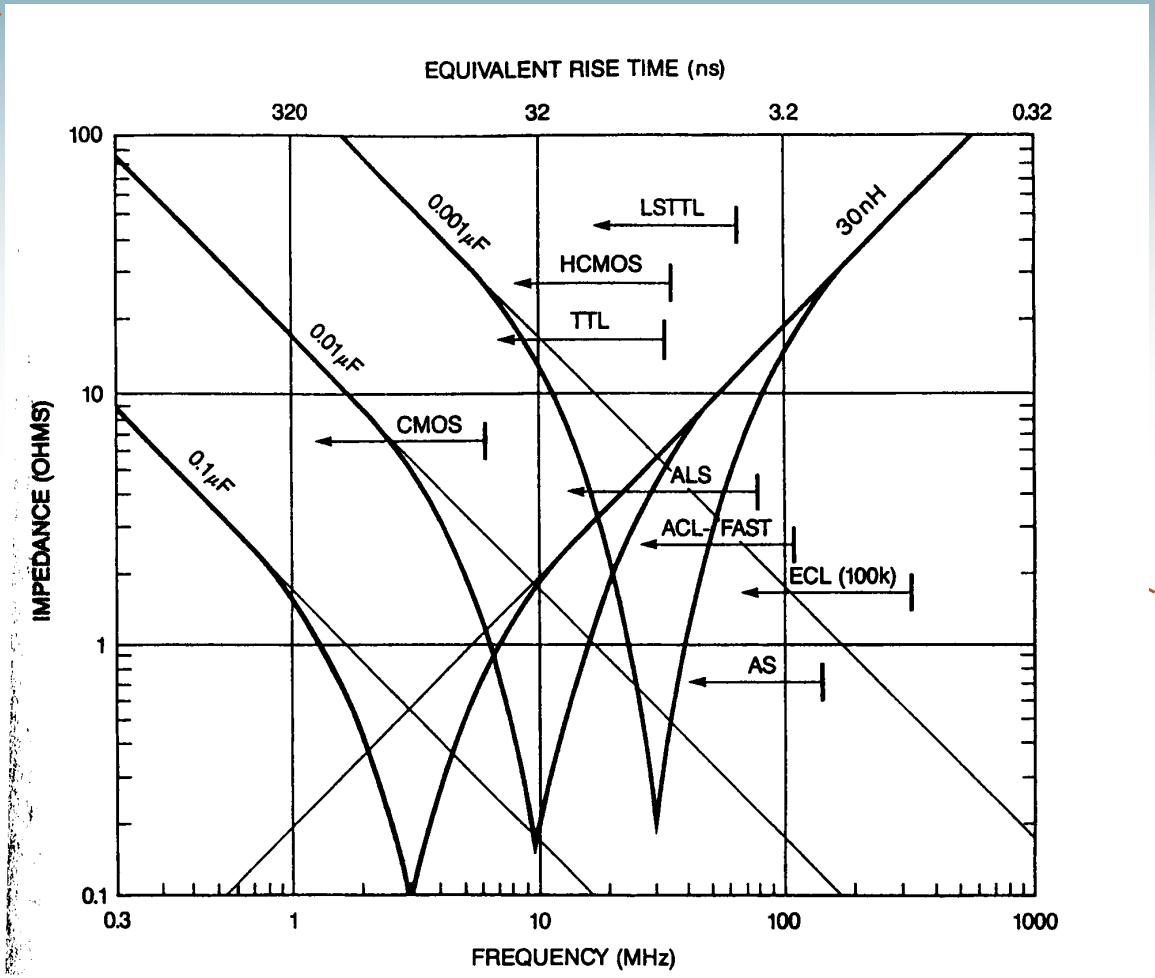
Capacitor Impedance vs. Frequency



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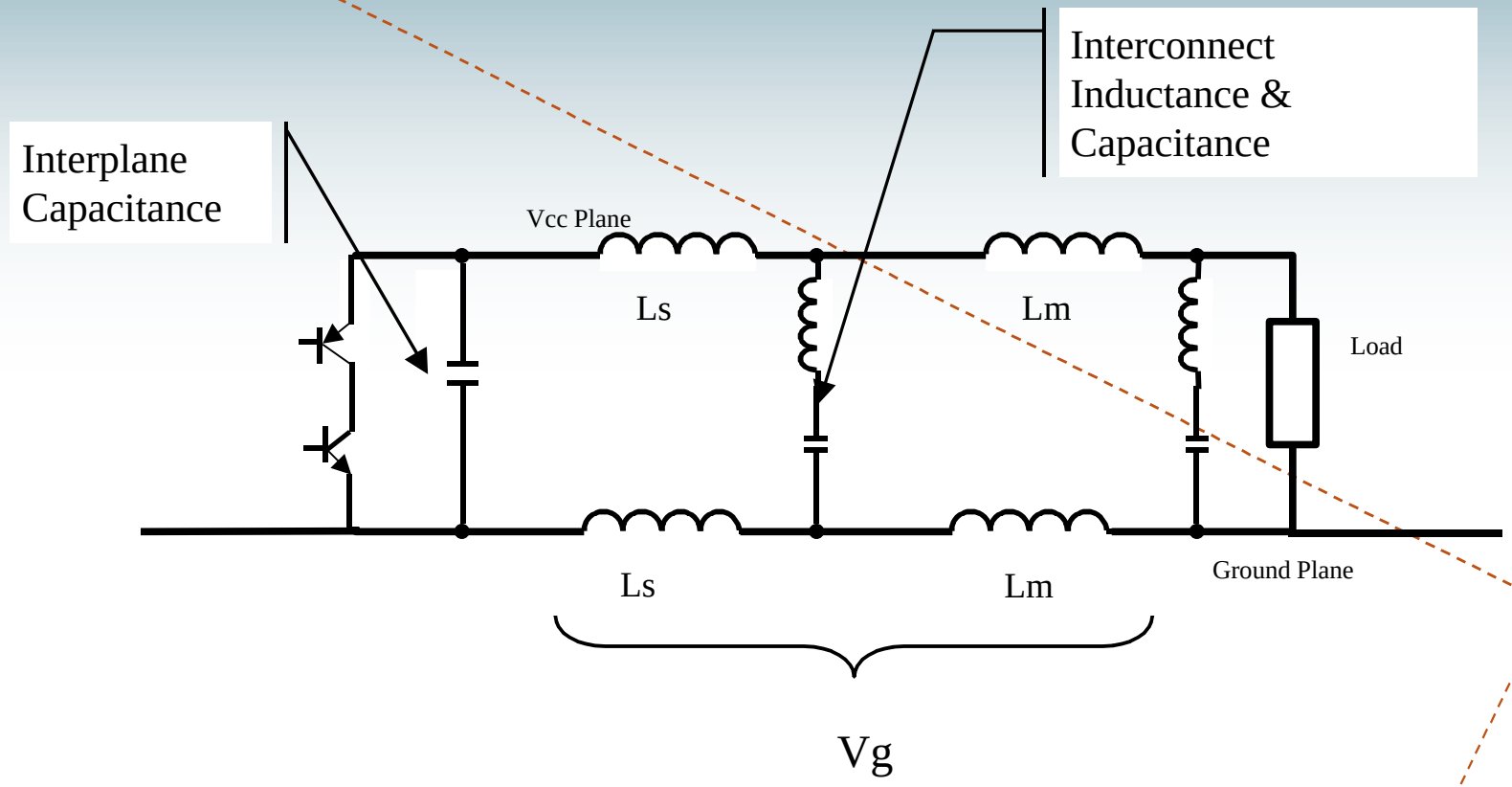
The Physics of Power Bus Noise



Part II
An Overview of the NCMS Embedded Decoupling Capacitance Project

discussion of materials properties

presented by: R. Charbonneau

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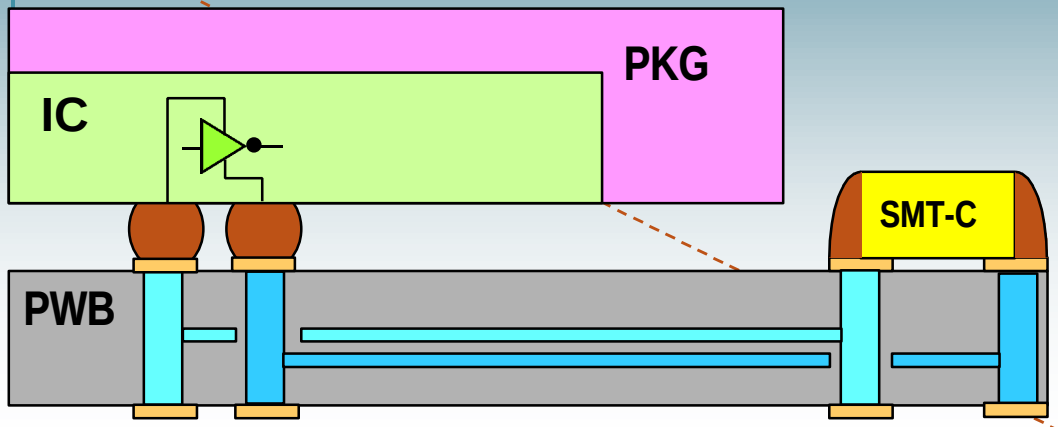
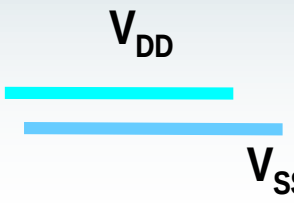
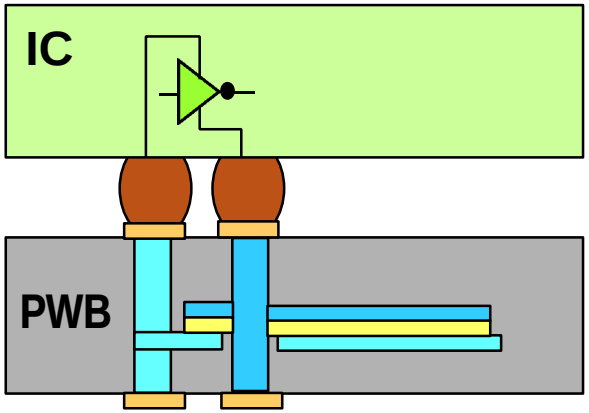
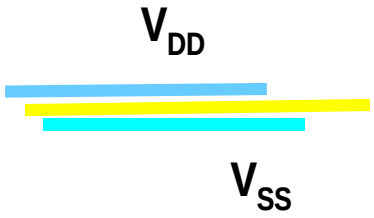


Discrete SMT Decoupling





Integrated Decoupling



Embedded Capacitance Layer

Source: 3M

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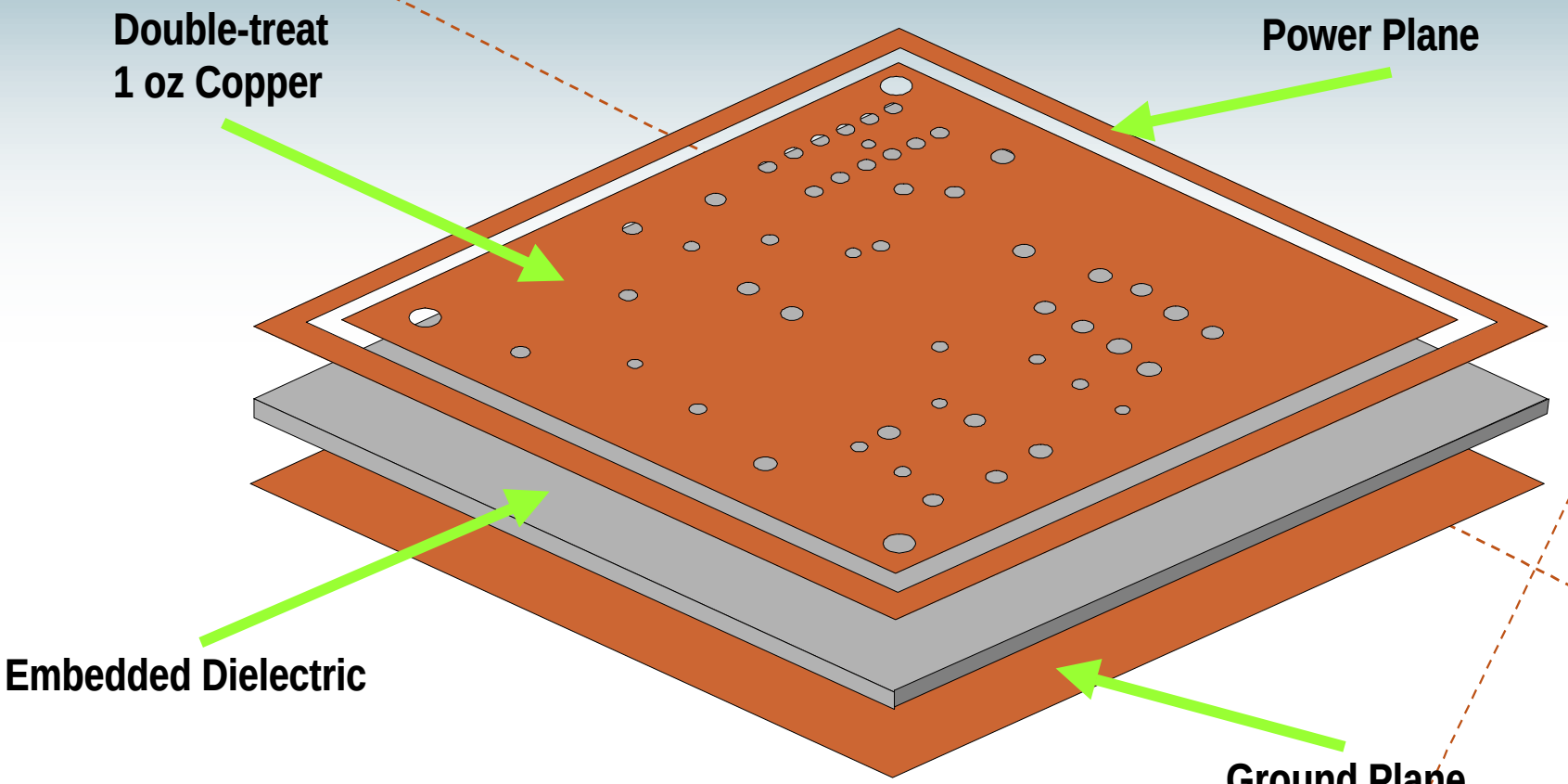
Why Embedded Capacitance ?

- **Increased packaging density**
  - ➔Frees up valuable real estate occupied by discretes.
  - ➔Potential for reducing size and number of layers.
- **Lower inductance**
  - ➔Improved electrical performance.
  - ➔Reduces power bus noise and electromagnetic interference.
- **Quality and Reliability improvement**
  - ➔Reduces the number of capacitors.
  - ➔Reduces the number of solder joints.

Embedded Capacitance the Next Step in PWB Design



Source: Hadco

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HADCO BC 2000 tm

Objective and Technical Approach

Initial Development Drivers

- Reduce assembled PCB cost.
- Save space to add new parts.
- Faster throughput at higher yields.

Primary Drivers Today

- Superior EMI performance at high frequency.
- Improved high frequency edge rate and pulse shape.

Status

- Patented product-HADCO
- Polyclad one of two U.S. lincenses
- Product has been in production since 1995

Technology

Very thin (0.0020” + 0.0002”) epoxy glass laminate clad with reverse laminated double treat copper foil used to form a capacitive layer.

Point of Contact Information

Bill Varnell
Polyclad Laminates, Inc.
45 Tannery Street
Franklin, NH 03235

Tel: (603) 934-5642
Fax: (603) 934-1243

bvarnell@polyclad-usa.com

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HADCO EmCap ™

Objective and Technical Approach

- Target Products
  - Any Digital Board with Discrete Bypass Capacitors (the larger the number of capacitors the greater this could improve overall system cost)
- Products that should NOT be Targeted
  - Analog Boards (individual capacitors cannot be created with this material)

Status

- HADCO Patent # 5,162,977
- Material Supplier-Polyclad
- 18” x 24” Panel Size
- Moving towards increased volumes of EmCap
- Developing modeling methods for EmCap

Technology

Standard FR4 filled epoxy

$BaTiO_X$ ceramic powder

Laminate coated material - unreinforced

Dielectric constant is 35-90*

Thickness 4 mils

Capacitance values 2-5nf/in^2

*not reproducible

Point of Contact Information

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Salem, NH 03079

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Fax: (603) 896-3303

tderego@hadco.com

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NCMS Embedded Decoupling Project

Steering Team:
StorageTek*
Delphi Electronics
Raytheon Hughes
Tobyhanna Army Depot
NCMS

Contracted Services:
NIST Gathersburg
Penn State University
University of Missouri-Rolla

Materials Suppliers:
Polyclad
Dupont
3M
Allied Signal

Board Fabricators:
HADCO
Merix
Raytheon Systems
Litton ACD

*project leader

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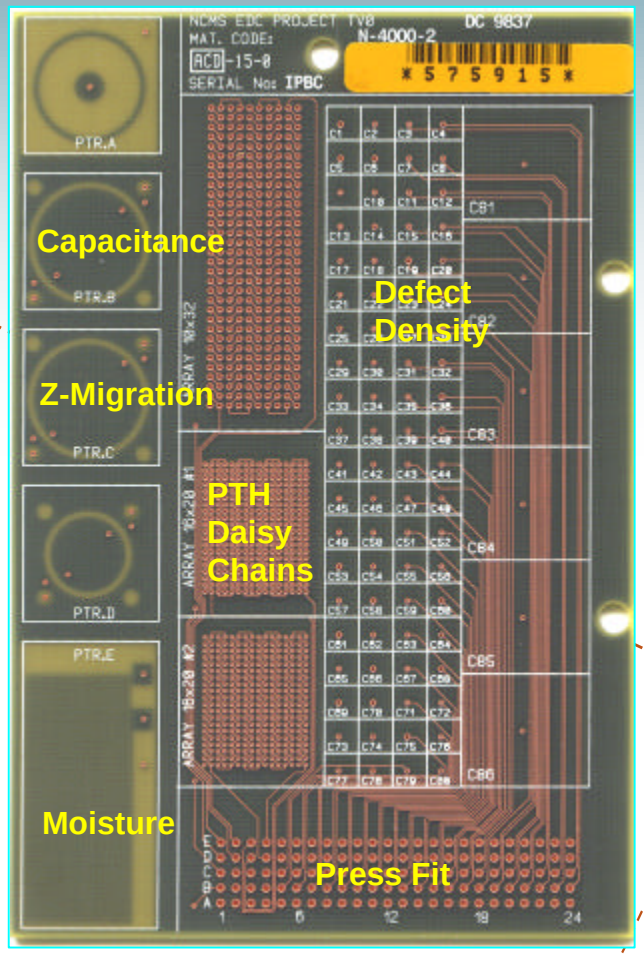
Embedded Capacitance the Next Step in PWB Design

Material Characterization

- Capacitance vs. Temperature
- Loss Tangent vs. Temperature
- Moisture and Z-Migration
- Pulse Discharge Equivalent Capacitance
- Polarization and Electroresistive Strain vs. Voltage
- Leakage Current
- Breakdown Voltage
- Flex Modulas (3 point bend test)
- Thermal Coefficient of Expansion



Test Vehicle 0

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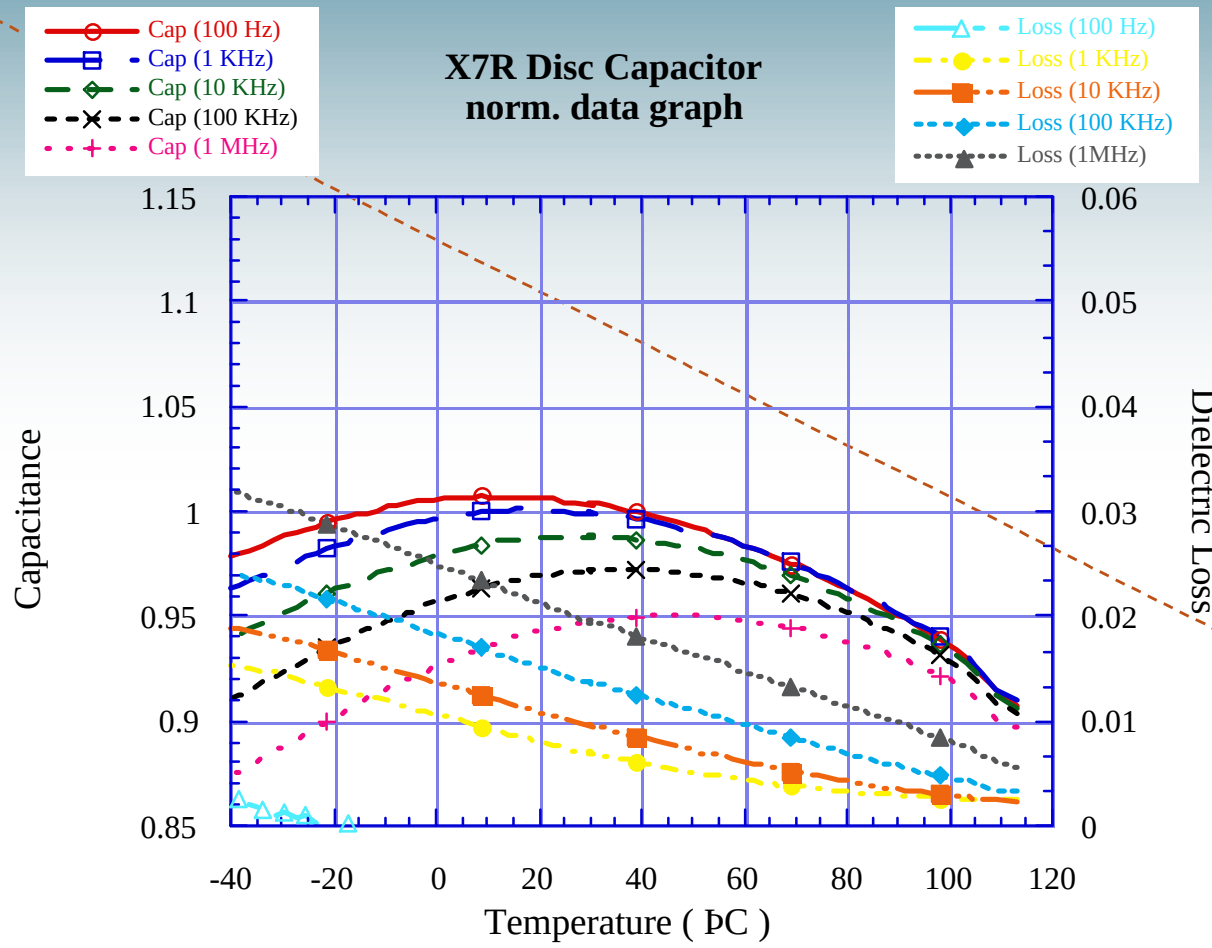

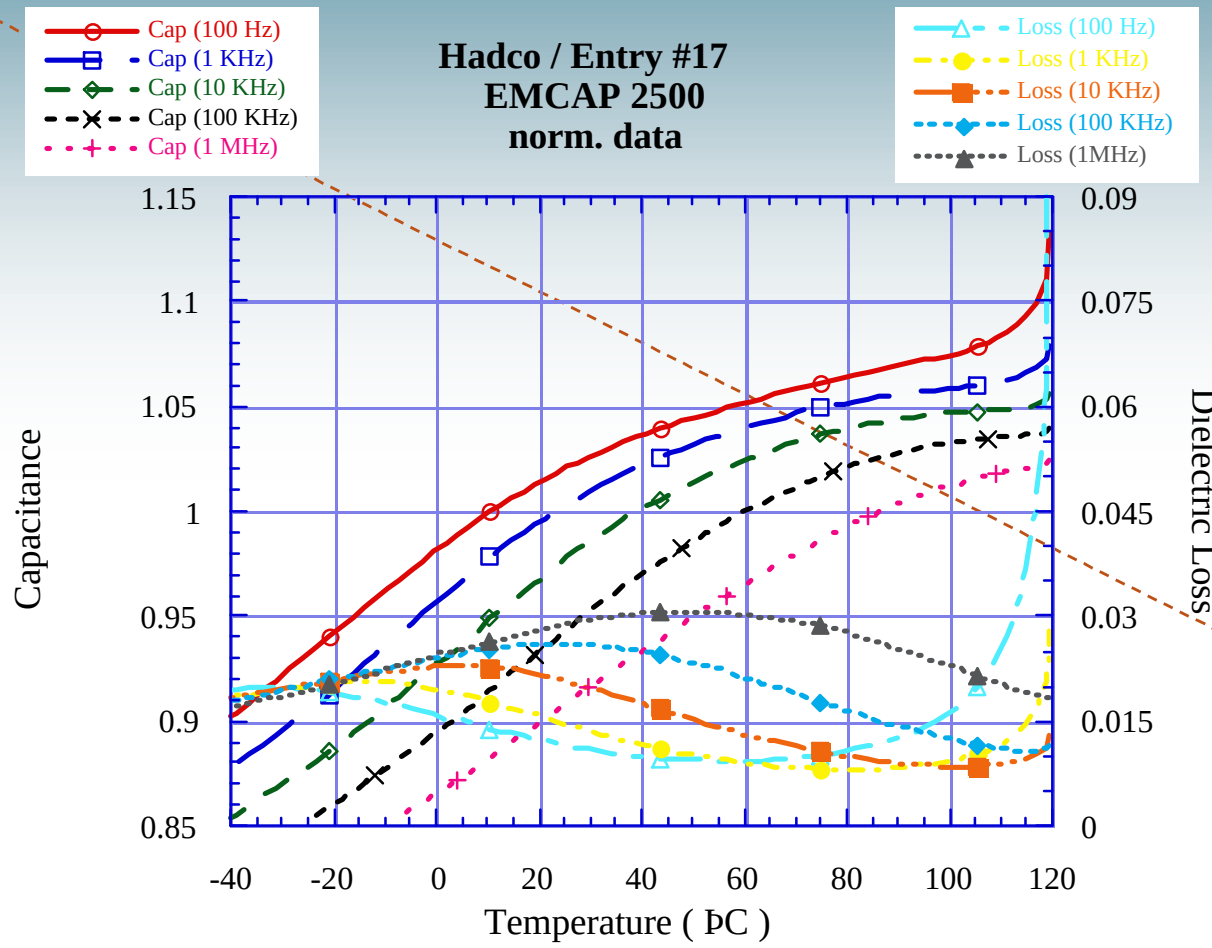

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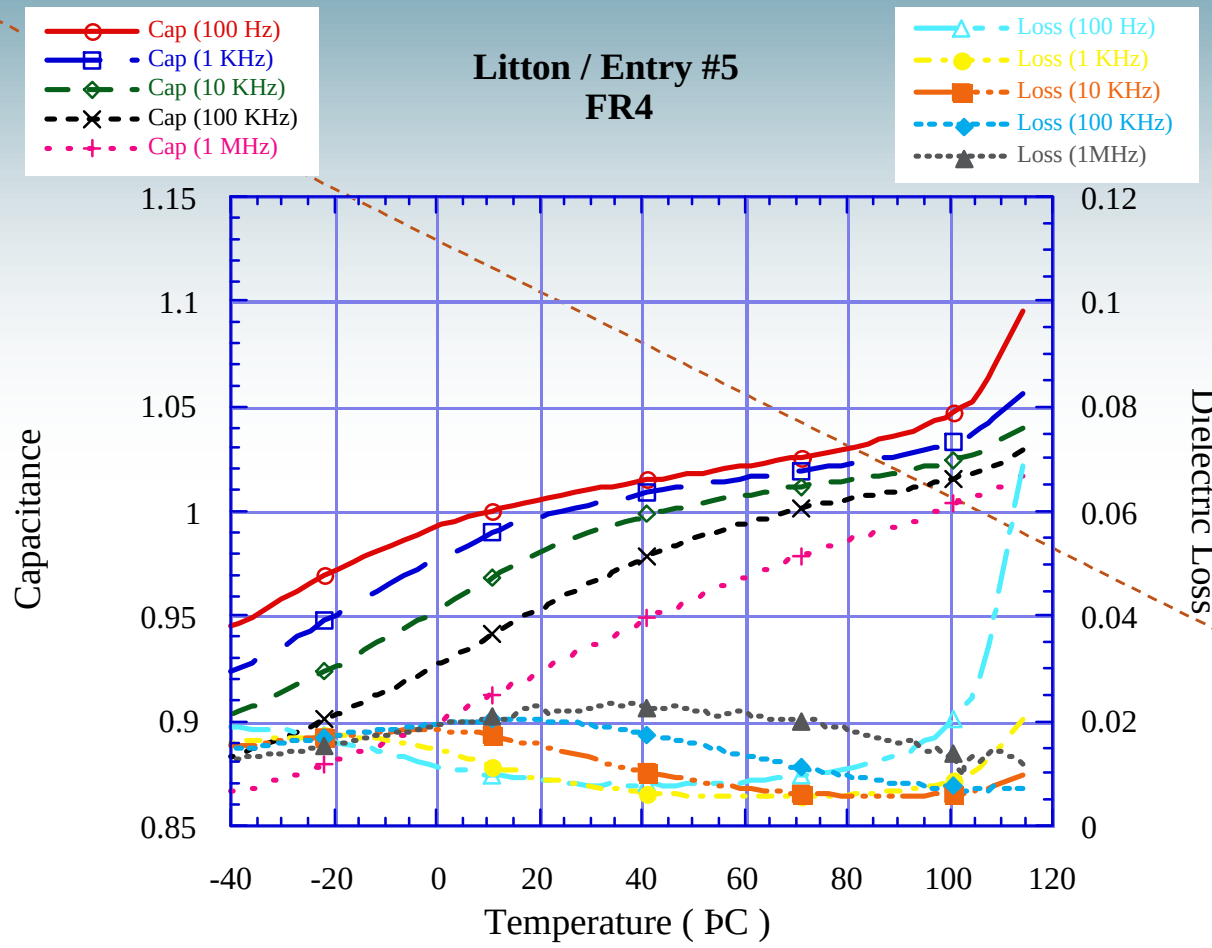

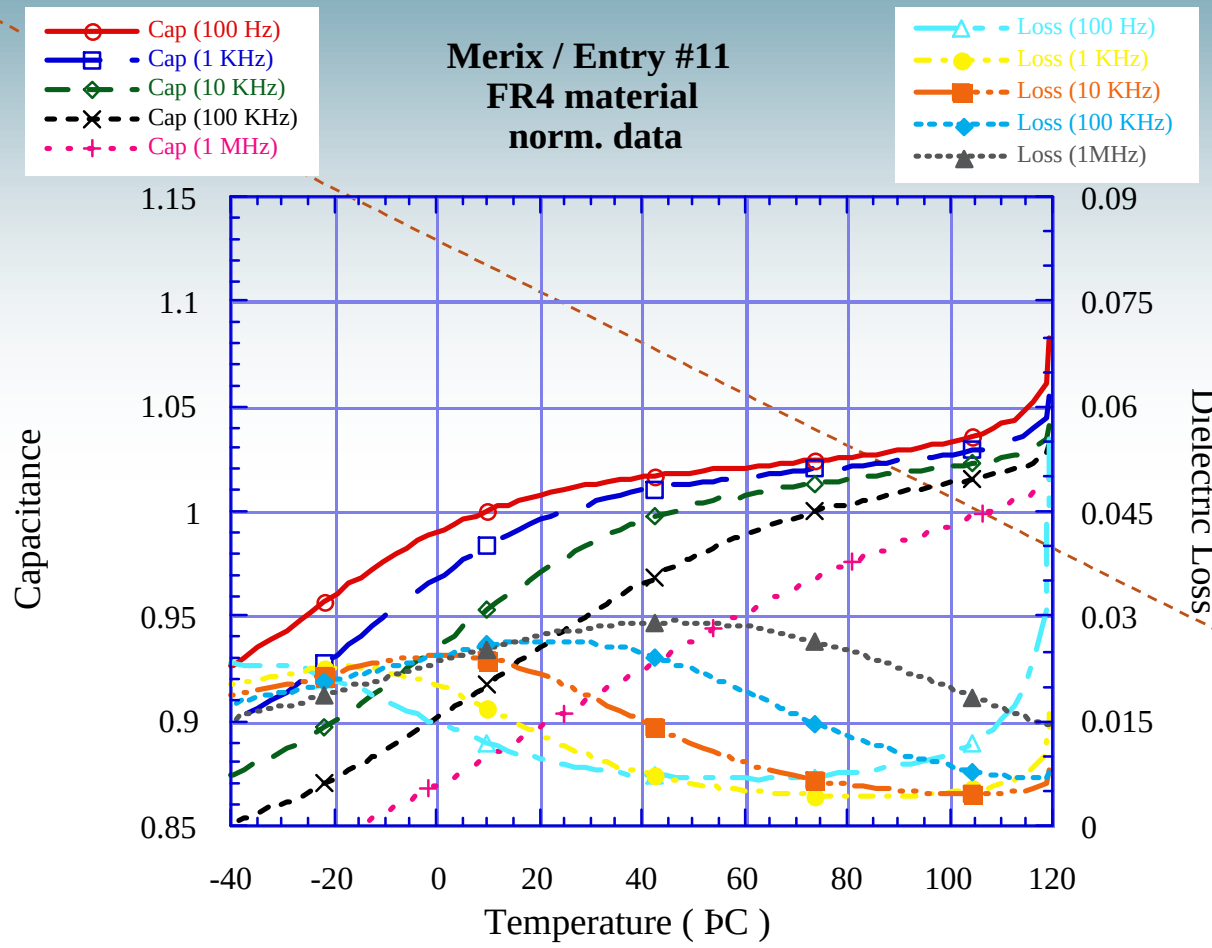

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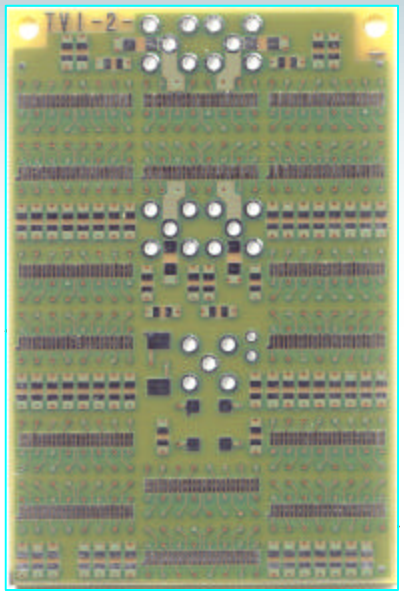
Embedded Capacitance the Next Step in PWB Design

Electrical Performance Measurements

- Power/Ground Plane Resonance*
  - Measure impedance vs. frequency of equivalent circuit
- Power Supply Ripple*
  - Measure differential voltage across Vcc and ground
- Electro Magnetic Interference**
  - Measure radiated field strength at 10 meters
- Power Supply Current*
  - Measure simultaneous switching currents



Test Vehicle 1

* University of Missouri
** Storage Technology Corporation

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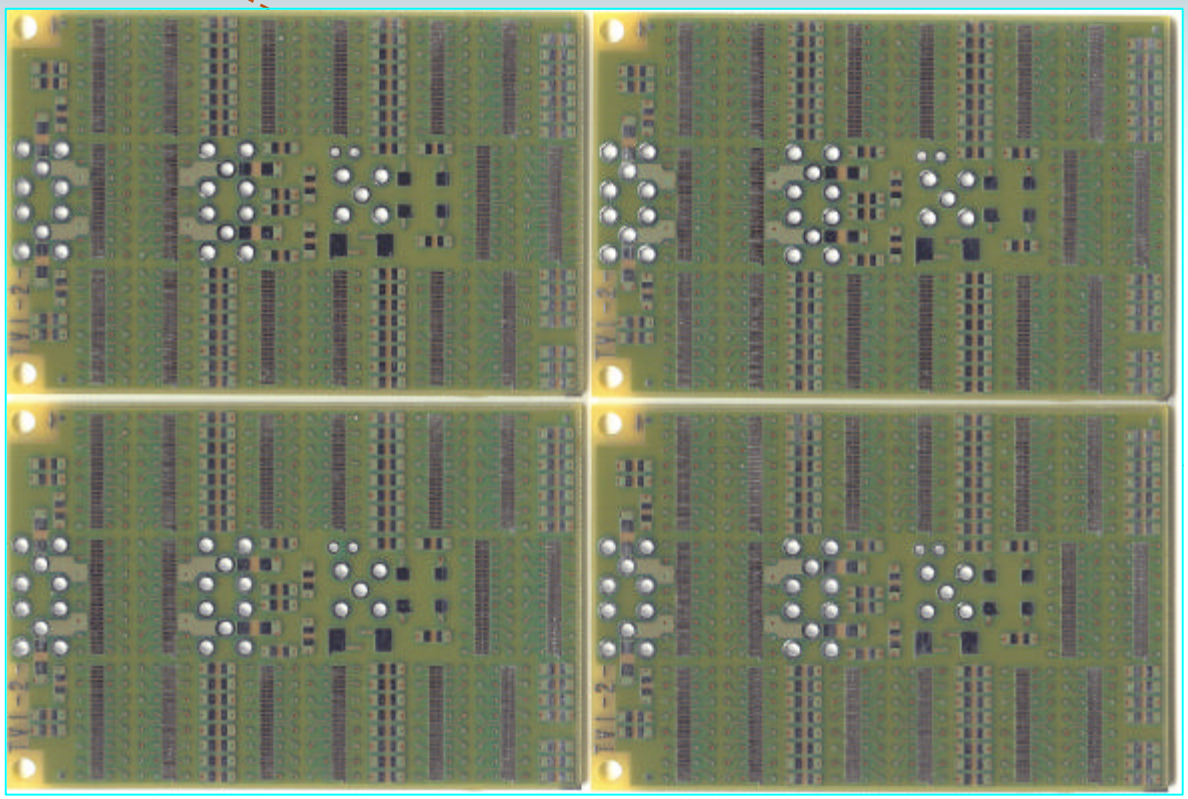
Embedded Capacitance the Next Step in PWB Design

TV1 4-up Panel



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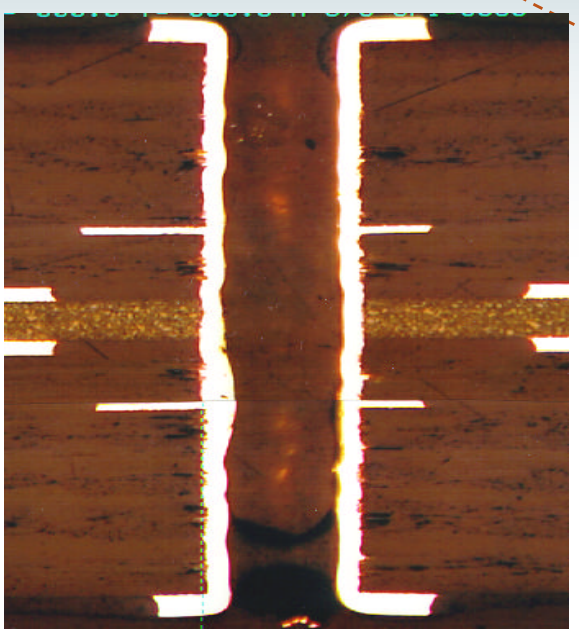
PWB Cross Sections



HADCO EmCap ™ (6 layer)

HADCO EmCap ™ (7 layer)

Source: Merix

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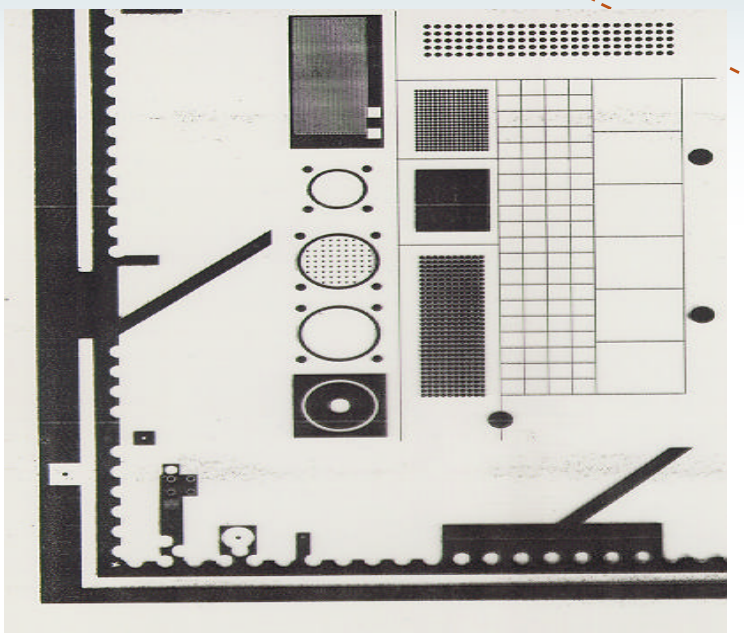
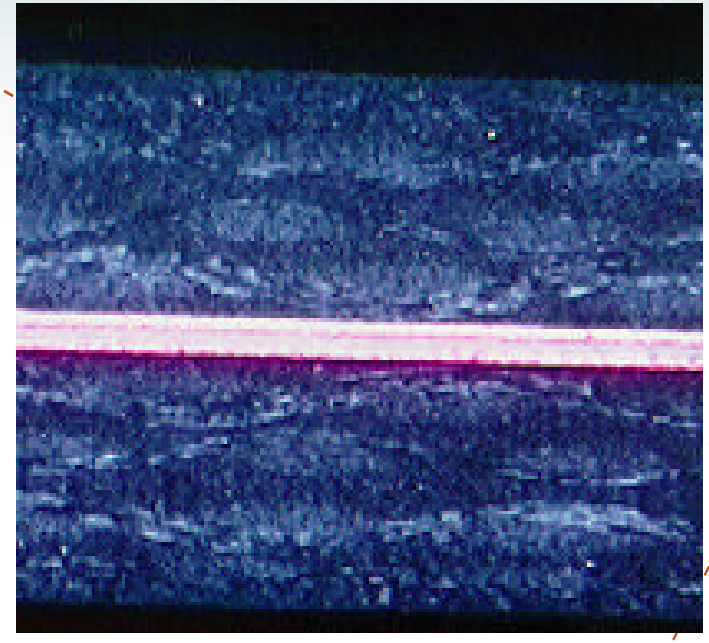
PWB Fabrication & Lessons Learned



Artwork Border Changes



Exposed Copper on Card Edge

Source: Merix

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NCMS Embedded Decoupling Project Status:

Critical Success Factor	3Q98	4Q98	1Q99	2Q99	3Q99	4Q99
Project Agreement						
TV0 Design & Layout						
Materials Characterization						
TV1 Design & Layout						
Modeling						
TV0 Reliability Testing						
Document Results						

- Program test vehicles have been designed and the reliability test boards have been fabricated. Reliability testing began in 2Q99 and is expected to be completed by 4Q99.
- Assembly of the electrical test boards is complete. The electrical testing and model development is scheduled for completion by Nov 1999.
- We expect the Project Report will be available in Feb 2000.

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Embedded Capacitance the Next Step in PWB Design

Next 90 days:

- 2-day project meeting in St. Paul, MN on Oct. 23 and 24.
- Continue accelerated reliability testing at Delphi Delco.
- Begin high frequency testing at NIST, Gathersburg.
- Begin EMI testing at StorageTek and power bus modeling at UM-Rolla.

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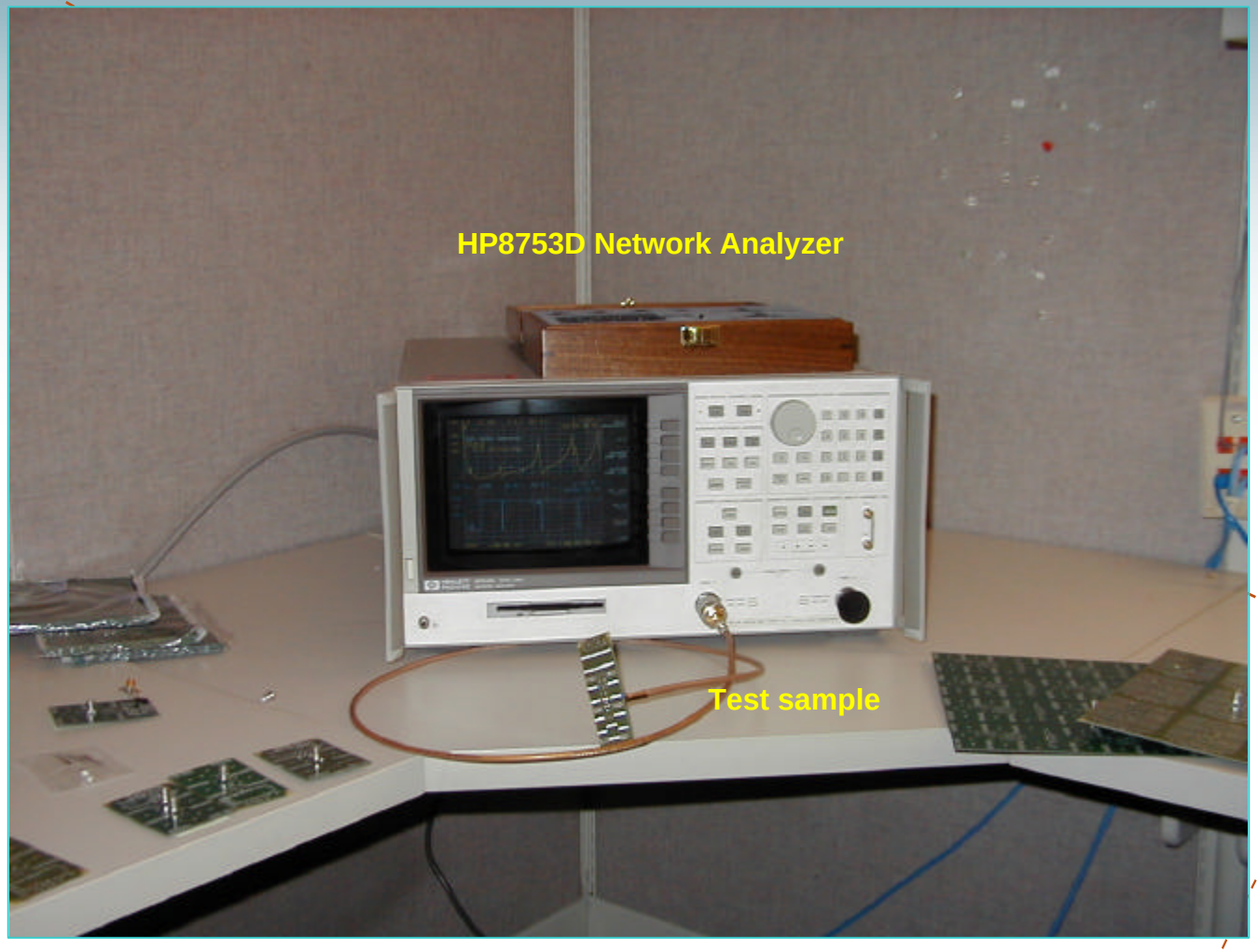
Part III
Swept Frequency Response of Power and Ground Planes

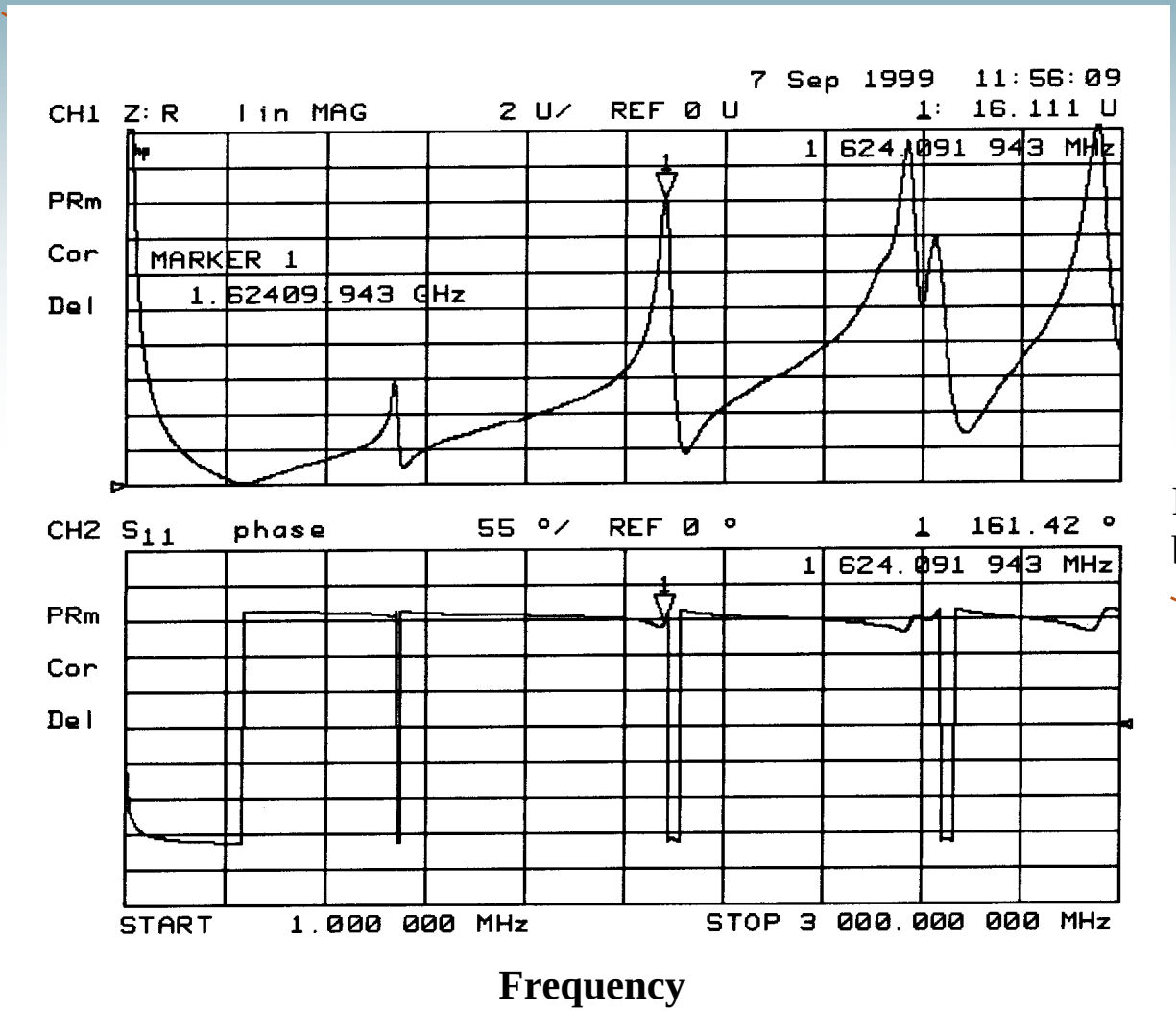
measured data

presented by: Charles Grasso

Test Set-up



Swept Frequency Data - 1up FR4 (Allied Signal 406)



Fabricated by: Merix

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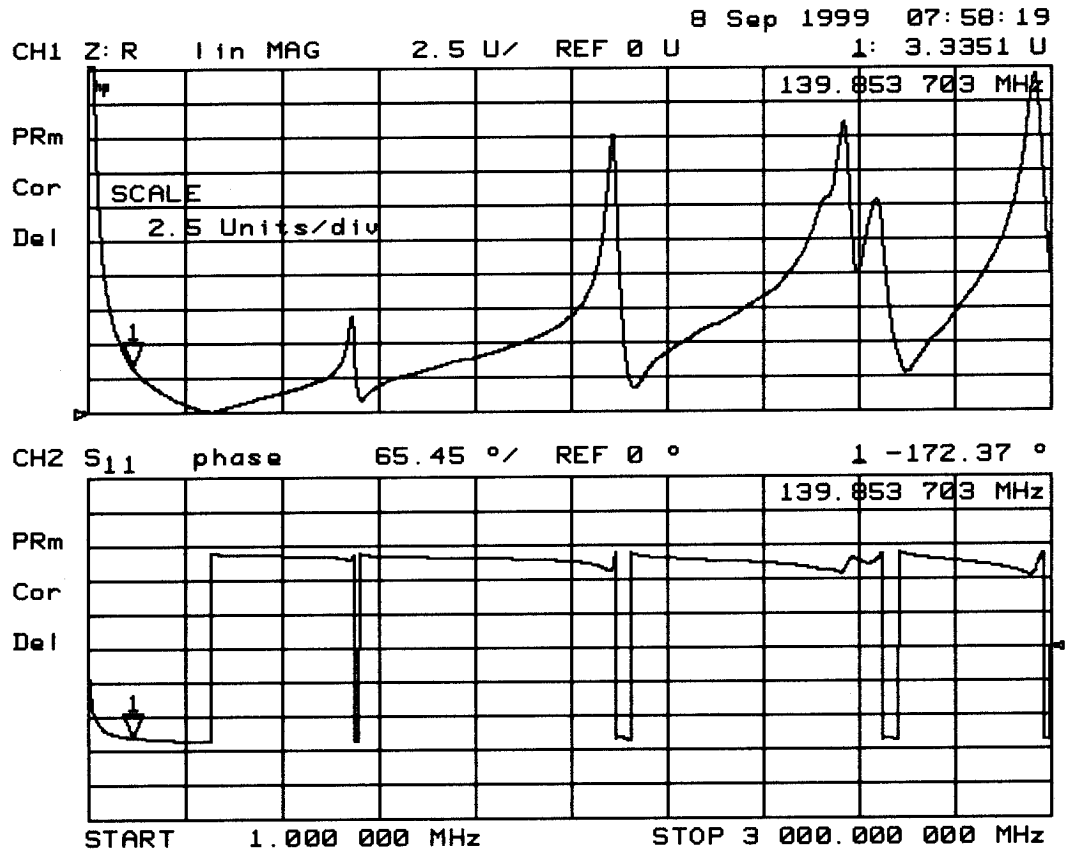
Swept Frequency Data - 1up FR4 (Allied Signal 406)



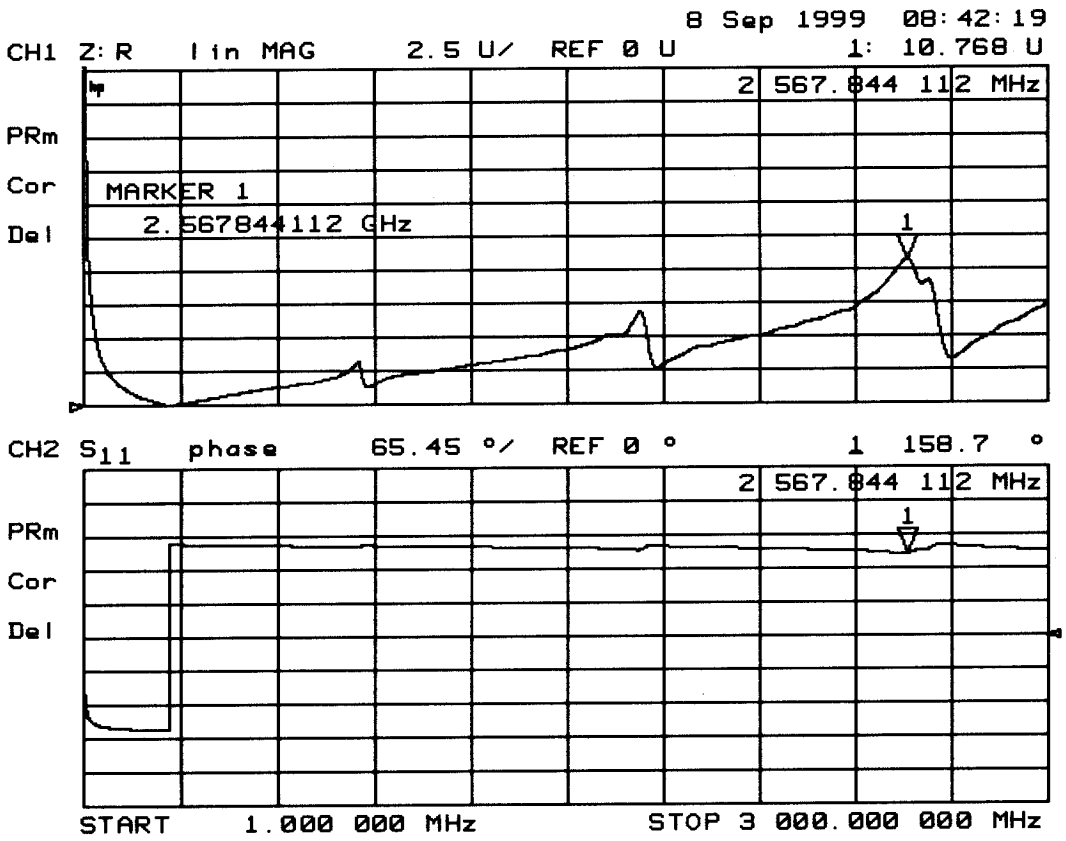
Impedance

Phase

Frequency

Fabricated by:
3M subcontractor

Swept Frequency Data - 1up FR4 (Nelco 4000-6)



Impedance

Phase

Frequency

Fabricated by: Litton

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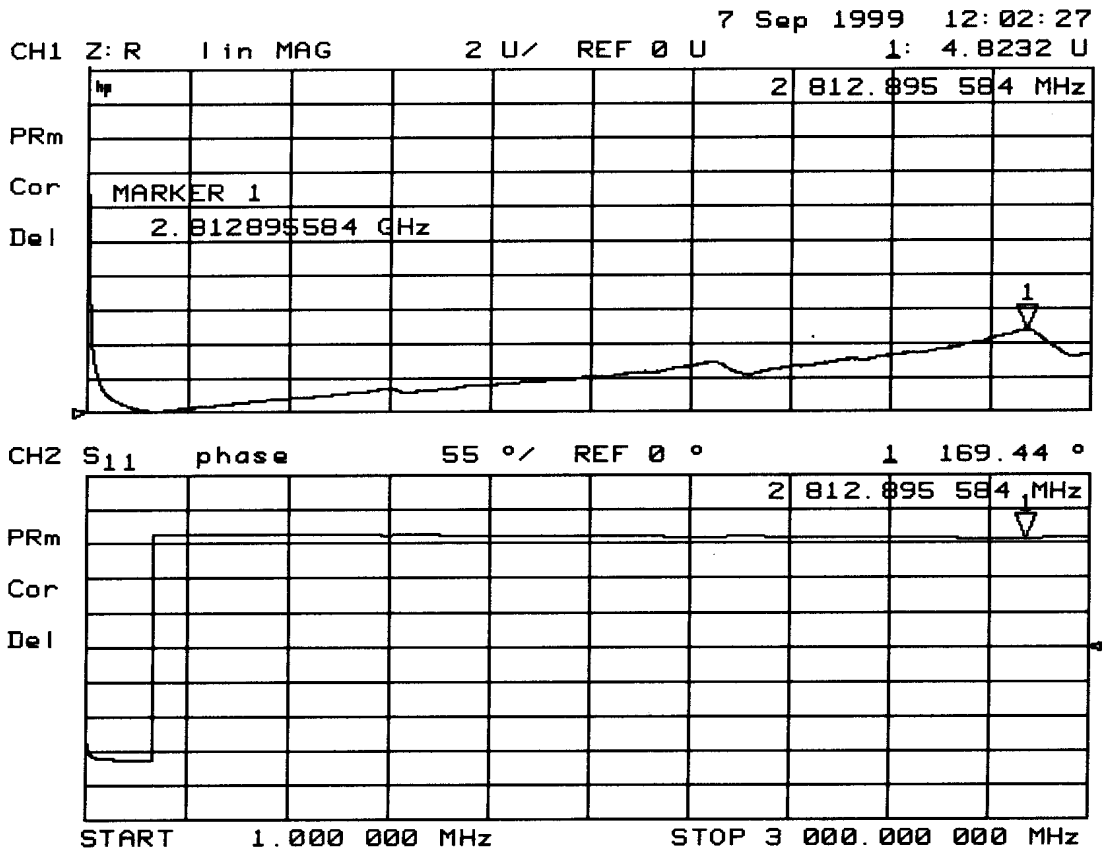
Swept Frequency Data - 1up BC2000 tm (PolyClad)



Impedance

Phase

Frequency

Fabricated by: Hadco

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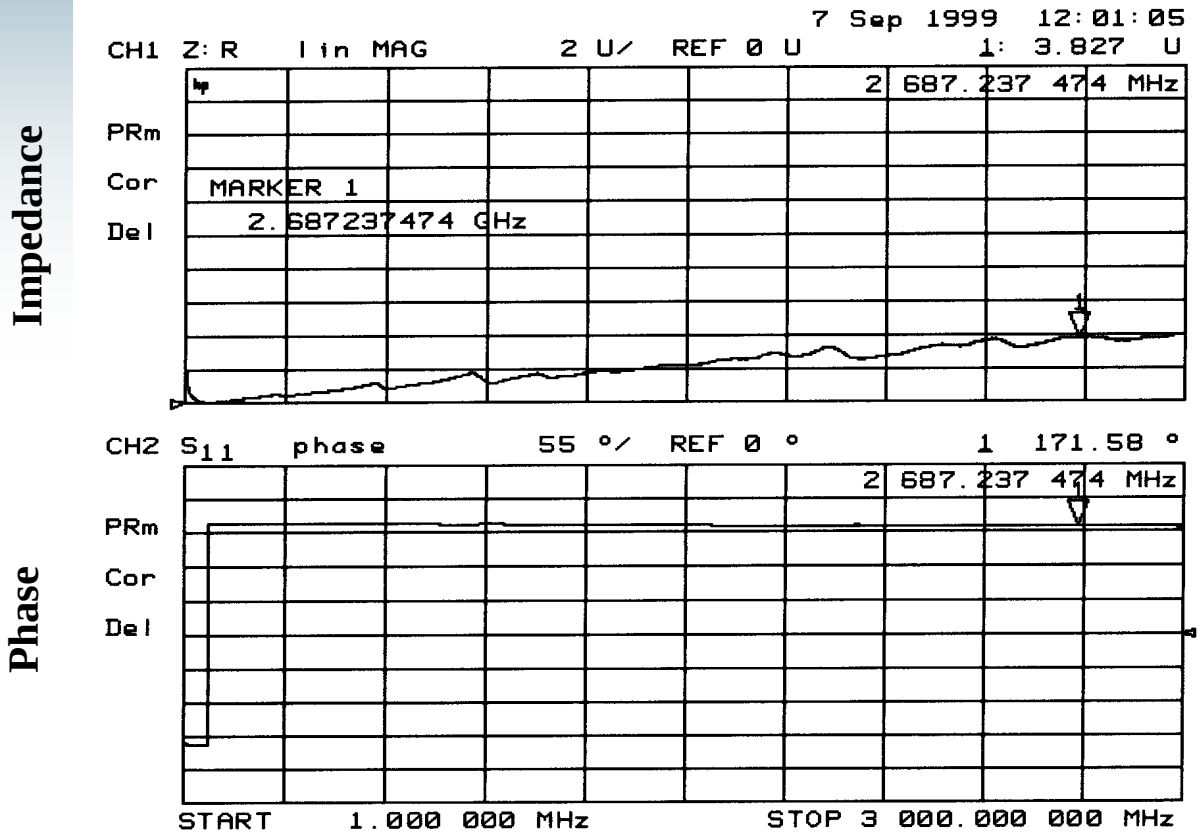
Swept Frequency Data - 1up EmCap ™ (PolyClad)



Fabricated by: Hadco

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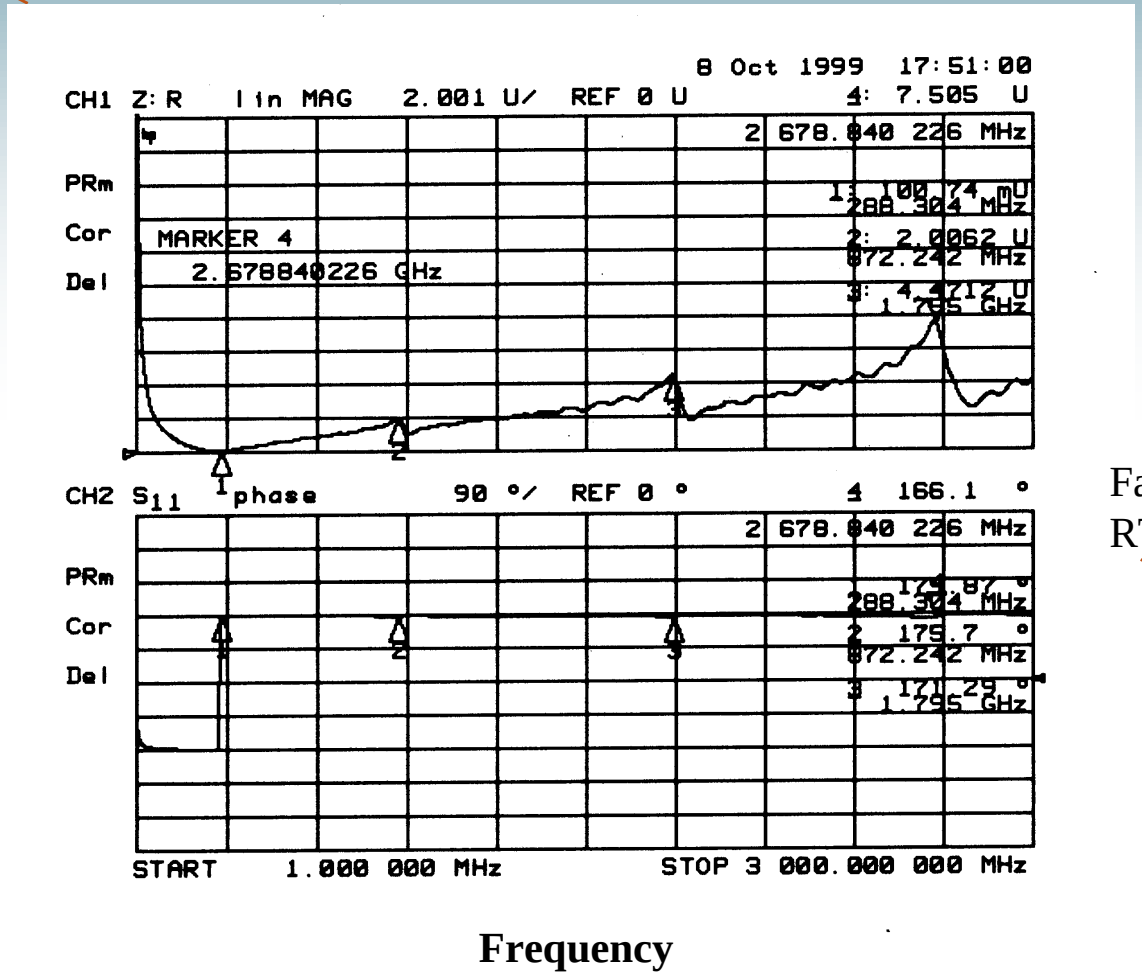
Swept Frequency Data - 1up FR4 (Polyclad Tetra II)



Impedance

Phase

Frequency

Fabricated by:
RTIS

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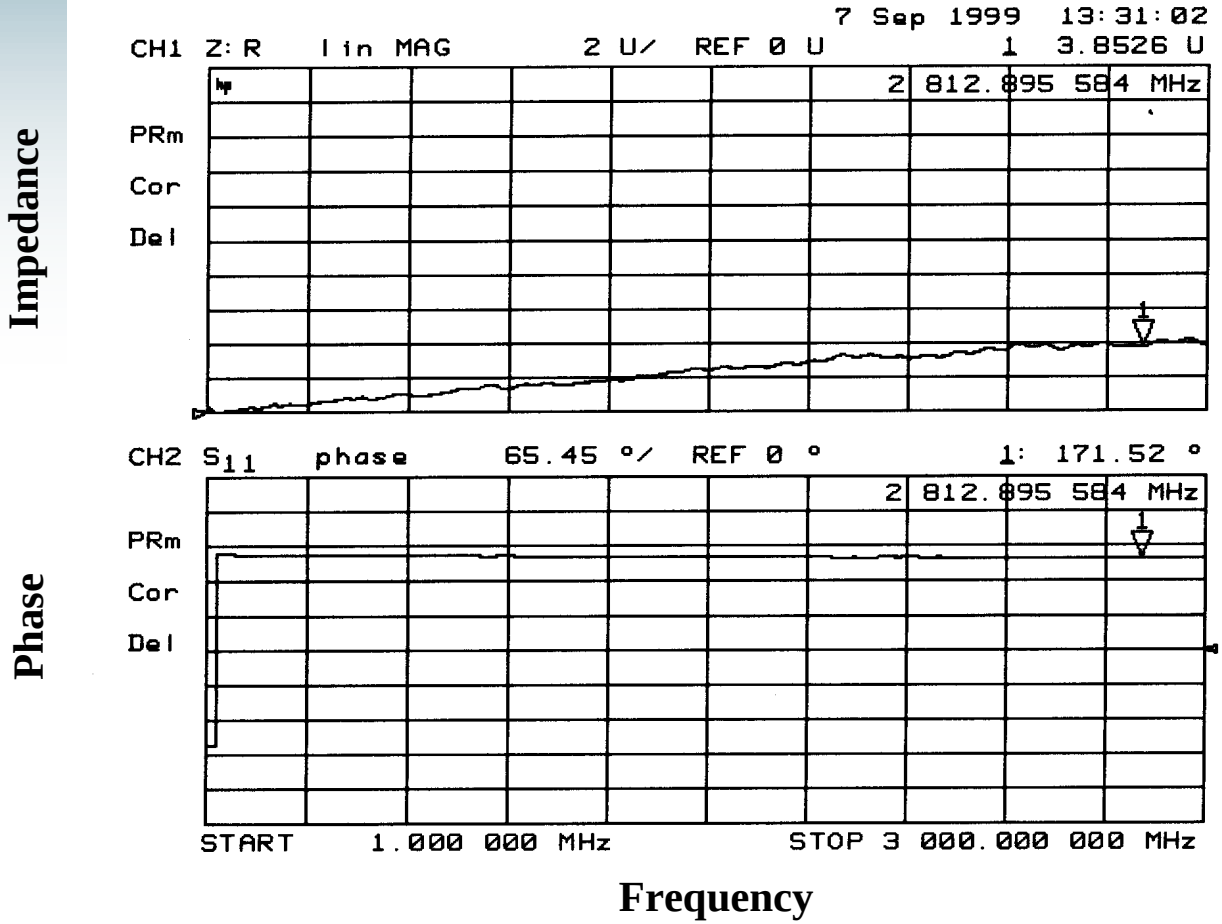
Swept Frequency Data - 4up EmCap ™ (PolyClad)



Fabricated by: Hadco

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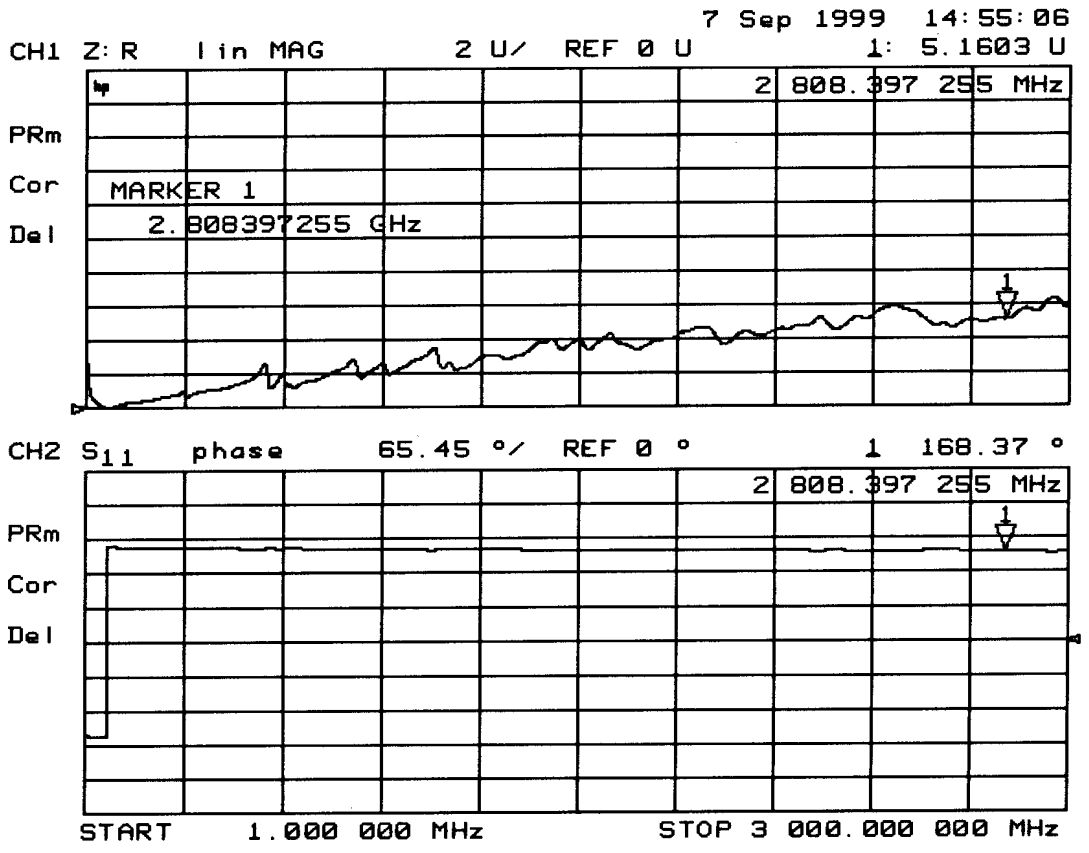
Swept Frequency Data - 12up FR4 (Nelco 4000-6)



Impedance

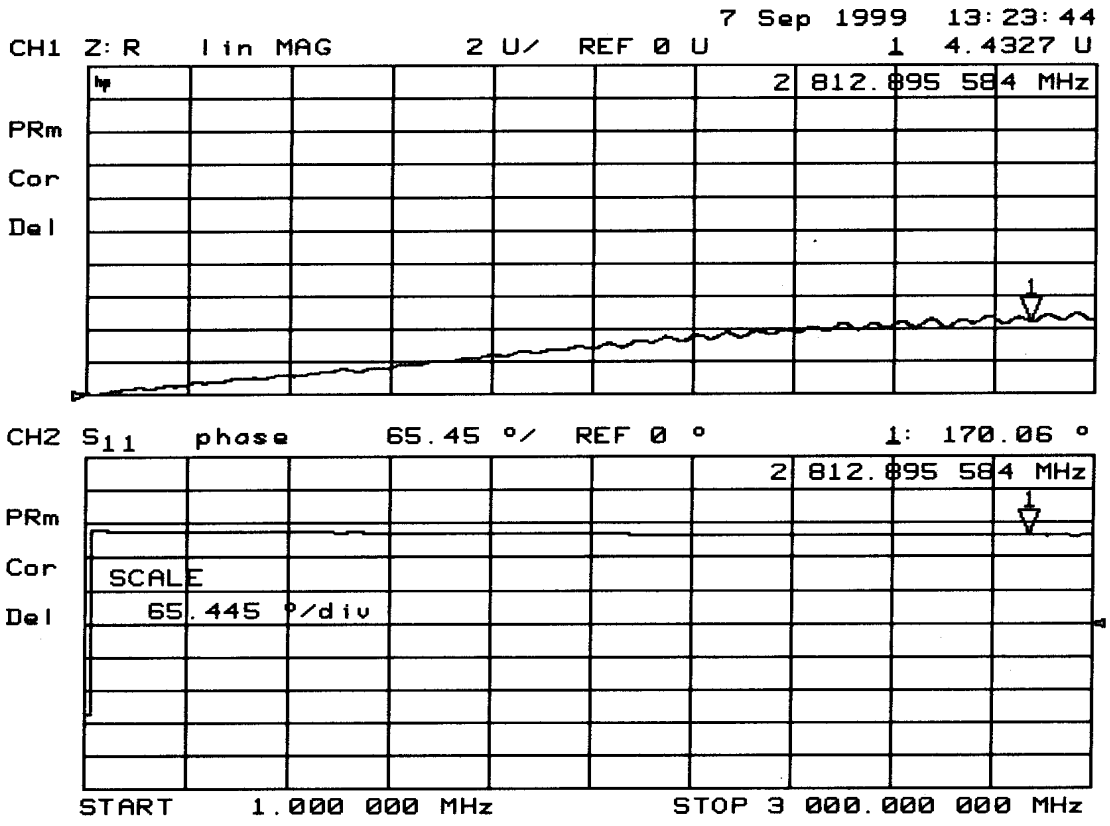
Phase

Frequency

Fabricated by: Litton

ncms Collaboration that works.

Swept Frequency Data - 12up EmCap ™ (PolyClad)



Impedance

Phase

Frequency

Fabricated by: Hadco

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Conclusions

- Higher dielectric constant embedded capacitance materials
  - ➔ Damp out the resonant peaks present in FR4 materials.
  - ➔ Results indicate a lower Z over a wide frequency range possibly reducing power bus noise.
  - ➔ Represent certain handling issues in board fabrication.

- Swept frequency responses
  - ➔ FR4 materials exhibited significant resonant peaks.
  - ➔ Results varied between different FR4 epoxy materials.
  - ➔ Results are essentially the same for 1up, 4up and 12up configurations with embedded capacitance.