

Signal Integrity Design versus Radiated Emission Control

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Outline

- Design Objectives (What?)
- Key Concepts (Why?)
- Design Considerations (How?)
 - EMI ☺ / SI ☺ **(EMI > si , SI > emi)**
 - EMI ☺ / SI ☹
 - EMI ☹ / SI ☹
 - SI ☺ / EMI ☹
- Summary

Design Objectives

Signal Integrity (SI)	Radiated Emission (EMI)
Make it work reliably <ul style="list-style-type: none"> ■ signal quality ■ timing ■ crosstalk ■ power/ground noise ■ ... 	Make it pass EMI tests <ul style="list-style-type: none"> ■ shielding ■ grounding ■ filtering ■ noise suppression ■ noise isolation ■ ...

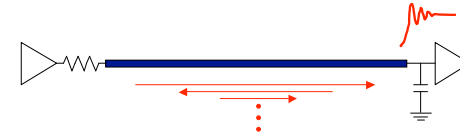
Key Concepts

SI	EMI
Time Domain	Frequency Domain
$V_S(t)$	$I_S(f) \square E(f)$
All High-Speed Signals	Clocks & I/O's
Low-Order Harmonics	High-Order Harmonics
Differential Mode Signal	Common Mode Noise
Noise: mV, mA	Noise: $\square V$, $\square A$

Key SI Concepts

- Transmission Line Effects
- Crosstalk
- Ground Bounce / Power Noise (SSN/SSO/□I)
- Current Return Path

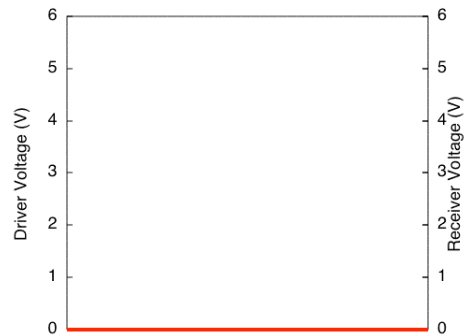
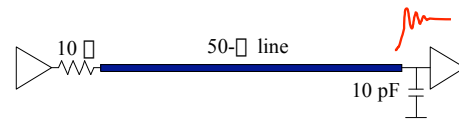
SI: Transmission Line Effects



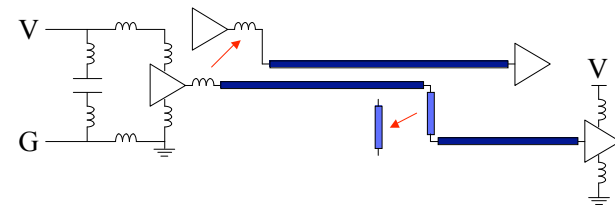
- Impedance (Z_0) and Propagation Velocity (v)

$$Z_0 = \sqrt{\frac{L}{C}} \quad v = \frac{1}{\sqrt{LC}}$$

- Delay = Length / Propagation Velocity
- Discontinuities □ Reflection □ Ringing

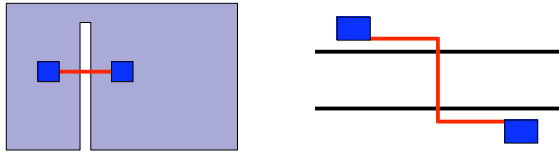


SI: Noise Mechanisms



- Crosstalk
 - Trace, cable, connector, package, via, RPD, ...
- Ground Bounce / Power Noise (SSN/SSO/□I)
 - Mechanism: $L \, di/dt$
 - Input reference, supply V, signal quality, crosstalk

SI: Current Return Path



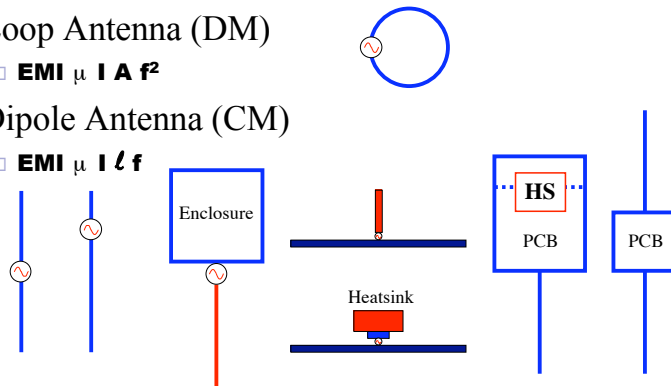
- Current flows in loops (in pairs!).
- Return current takes the least Z path.
- Discontinuities □ Reflection & Crosstalk!

Key EMI Concepts

- All SI concepts plus the following:
- Noise Source □ Coupling □ Antenna
- Shielding, Grounding, Filtering, Noise Suppression, Noise Isolation, ...
- Antenna
- Ground Inductance
- Current Return Path (again!)

EMI: Antenna

- Loop Antenna (DM)
 - $EMI \propto I A f^2$
- Dipole Antenna (CM)
 - $EMI \propto I \ell f$



EMI: An Interesting Question

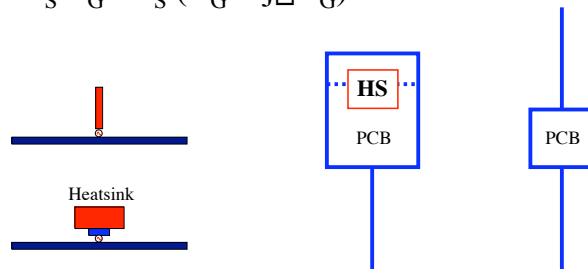
- Microstrip
- Coplanar Strips



- Which one radiates more?
 - $Z_{0M} = Z_{0C} = R_T$
 - $\ell_M = \ell_C$
 - $H > S$

EMI: Ground Drop

- Ground Drop is a main source of CM radiation!
- $V_G = I_S Z_G = I_S (R_G + j\omega L_G)$



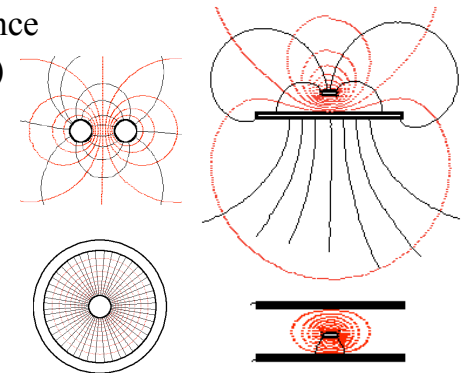
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EMI: Ground Inductance

- $L_G \neq$ self inductance
- Pairs (S, P, V, W)
 - $L_{GP} = L/2$
- Microstrip
 - $L_{GM} \ll L$
- Stripline
 - $L_{GS} \ll L_{GM}$
- Coaxial
 - $L_{GC} \approx 0$



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EMI: DM vs. CM Radiation

- DM Radiation

$$E_{DM} \propto I_S(f) \ell H f^2$$

- CM Radiation

$$E_{CM} \propto I_{CM}(f) f$$

$$\propto V_G(f) f$$

$$\propto I_G(f) \ell L_G f$$

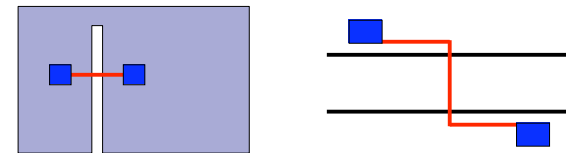
$$\propto I_S(f) \ell \omega^2 f^2 / W \quad (L_G \propto H/W)$$

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EMI: Current Return Path



- Discontinuities $\propto L_G \propto V_G \propto$ EMI
- Discontinuities $\propto V_{PP} \propto$ EMI

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Design Considerations

- EMI ☺ / SI ☺
 - EMI > si
 - SI > emi
 - There are exceptions. It depends on:
 - Shielding
 - Spread Spectrum Clocking
 - ...
- EMI ☺ / SI ☺
- EMI ☺ / SI ☹
- SI ☺ / EMI ☹

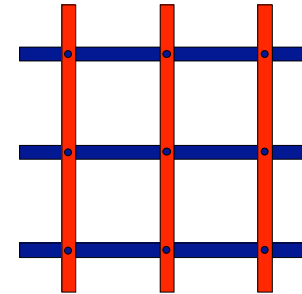
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E☺/S☺: Ground Planes/Grids

- EMI & Crosstalk > Signal Quality
- SI
 - Impedance control
 - Reduce crosstalk
- EMI
 - All the above
 - Reduce A
 - Reduce L_G □ V_G



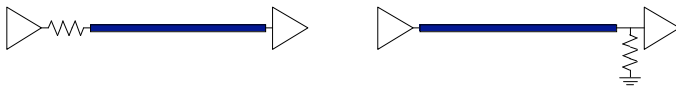
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E☺/S☺: Terminations

- Reflection □ Ringing □ High-Order Harmonics
- Source T. better than End T. for EMI (> 4 dB!)

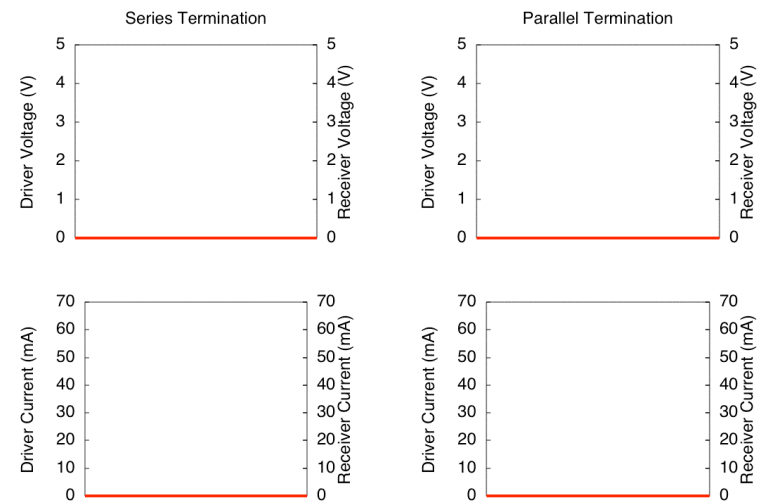


- Diode termination can increase EMI! (E☹)
 - Clean Voltage Waveform ≠ Clean Current Waveform
- DM and CM terminations
- Clocks & HS I/O's: EMI > si

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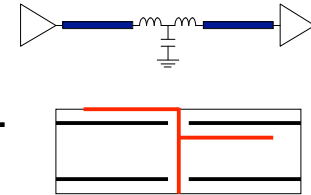
E☺/S☺: Impedance Matching

- Reflections do not only occur at both ends.
- Transmission line transitions:
 - **Microstrip** □ **Stripline**
 - **PCB Trace** □ **Cable**
 - **Motherboard** □ **Daughter Card**
- DM and CM matching
- High-speed connector Z_0
- Clocks & HS I/O's: EMI > si

E☺/S☺: Stubs & Vias

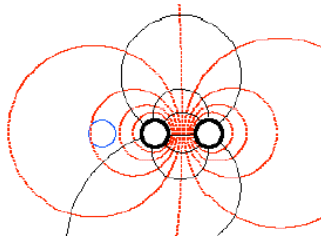
- Excess L or C □ Reflection □ Ringing
- Vias w/o switching RP's are less of a problem.
- Design "matched" discontinuities!

- $L/C = Z_0^2$
- **Reduce trace width.**
- **Increase via clearance.**
- **Use blind and buried vias.**
- **Back-drill vias.**



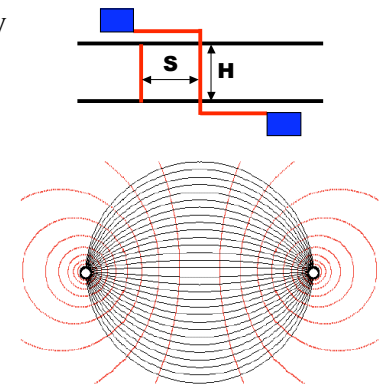
E☺/S☺: Crosstalk

- Trace-to-trace crosstalk
 - **Maintain spacing.**
 - **Minimize parallel length.**
- Pin-to-pin crosstalk
 - **Design proper pinout.**
- Via-to-via crosstalk
 - **Provide adjacent return via when switching RP's.**
- Clocks □ I/O's: EMI > si
- Others: SI > emi

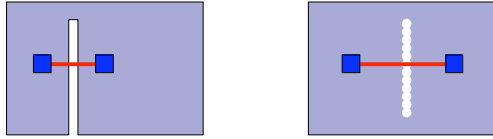


E☺/S☺: Return Vias

- Crosstalk > Signal Quality
- $L_{Via} \square 2.8 \text{ nH}$
 - $D = 10 \text{ mil}$
 - $S = 1 \text{ in}$
 - $H = 50 \text{ mil}$
- $M_{Trace} \square 2.5 \text{ nH}$
 - $Z_0 = 65 \square$
 - $W = S = 5 \text{ mil}$
 - $L = 1 \text{ in}$
- Many-to-many coupling!
- Plane edge reflections!



E☺/S☺: Traces Crossing Slots



- EMI (L_G) > Crosstalk (M) > Signal Quality (L_{ex})
- Traces crossing split planes
 - Add decoupling capacitors.
 - Add stitching capacitors.
 - Avoid them in the first place.
- Avoid unnecessary ground cuts & isolations.

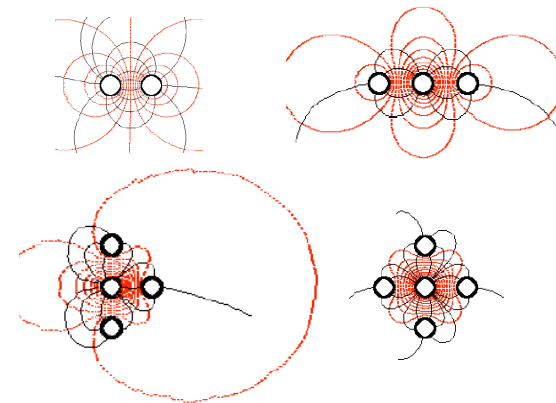
E☺/S☺: Ground Bounce & SSN

- Mechanism: $L \frac{dI}{dt}$
- SI: (V_{Ref} , V_{Supply} , Signal Quality, Xtalk)
 - Minimize package L & M.
 - Use slew rate control.
 - Reduce shoot through current.
 - Use differential signaling.
- EMI (I/O noise)
 - Provide dedicated I/O power and ground.
 - Design proper pinout.

E☺/S☺: Connector & IC Pinouts

- For connectors and IC's with Heatsink
 - EMI > Crosstalk > Signal Quality
- Provide adjacent Ground pins to Power.
- Provide adjacent Return pins to Clocks, High-Speed and I/O Signals.
- Isolate I/O and susceptible pins from noisy pins.
- It is desirable to provide additional adjacent Return pins to Clocks to reduce L_G !

E☺/S☺: More Return Pins



E😊/S😊: Stackup & Placement

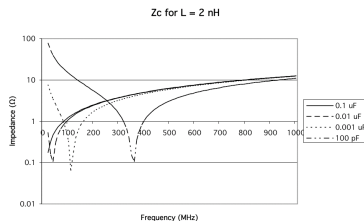
- PCB Stackup for EMI
 - All SI considerations plus the following:
 - Use Ground Planes or Ground Grids.
 - 2 or more Ground Layers □ Ground Stitching
 - Provide solid Ground Plane underneath Noisy IC's.
- Component Placement for EMI
 - All SI considerations plus the following:
 - Place I/O connectors on one side of the PCB.
 - Place High-Speed IC's away from I/O & PCB edges.

E😊/S😊: Differential Signaling

- Improve noise immunity. (SI)
- Reduce ground bounce. (SI)
- Reduce ground drop $V_G = L_G dI_G/dt$. (EMI)
- Current mode differential signaling eliminates shoot through current. (SI & EMI)
- Minimize differential skew and maintain balance.
- HS Differential I/O's: EMI > si

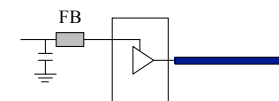
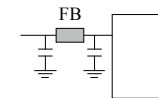
E😊/S😊: Power Decoupling

- Minimize Inductance
 - Proper layout
 - On-package capacitors
 - On-die capacitance
- Use single value C's
 - Avoid anti-resonance!
- Power plane resonance
 - Thin dielectric lowers Q due to skin loss!
 - Use lossy capacitors!
 - Power isolation!



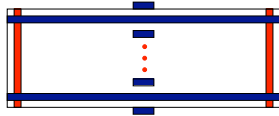
E😊/S😊😊😊😊: Power Isolation

- SI: Isolate Power for Susceptible Circuits
- EMI: Isolate Clock & I/O Power
- Typical Implementation
 - Ferrite bead
 - Use routing layer!
 - Don't overdo it!
 - Affect signal if it references to power plane! (S⊗)
- Backdoor termination!?!
 - Starve the driver. (S⊗)



$E\odot/S\ominus$:

- Splitting clock frequencies
 - **Avoid overlapping harmonics.**
- Shielding
 - **Ground stitching**
- Grounding
 - **Grounding heatsinks**
 - **Terminate to eliminate PCB-chassis resonance!**



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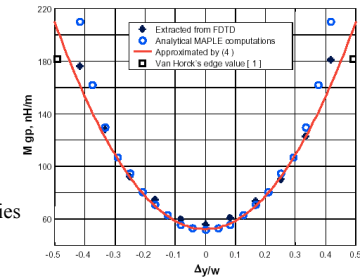
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$E\odot/S\ominus$: Clocks away from Edges

- Minimize board edge fringing fields.
- Minimize $L_G \square V_G!$

M. Koledintseva et al.,
“External Parasitic Inductance in
Microstrip and Stripline Geometries
of Finite Size”, Proc. 2002 IEEE
EMC Symposium, pp. 244-248.



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$E\odot/S\ominus$:

- Filtering: I/O's and Clocks
 - **Minimize impact on signal quality.**
- Spread Spectrum Clocking
 - **Minimize PLL tracking skew.**
- Burying Clocks ($S\ominus\ominus$)
 - **Minimize DM and CM radiation.**
- Skin & Dielectric Losses
 - **Signal Loss and Dispersion**
 - **Pre-emphasis ($E\otimes$) vs. Equalization ($E\odot$)**

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$S\odot/E\ominus$:

- Ground Isolation
 - **Because of noise concerns**
 - Make sure high-speed signals do not cross ground cuts.
- Timing Driven
 - **Long clock routes**
 - Bury them.
 - **Surface clock routes**
 - Use guard traces to reduce L_G and DM radiation!

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Summary

- Design Concepts
 - **Transmission Line Effects**
 - **Noise Mechanisms**
 - **Current Return Path**
 - **Antenna**
 - **Ground Inductance**
- Compare and contrast SI & EMI considerations.
- Design rules may change but underlying concepts will remain.