Power Distribution Network Design for High-Speed Printed Circuit Boards

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Outline

• Overview of PDN design in multi-layer PCBs
• Interconnect Inductance
• Individual Capacitor Values
• Capacitor Location
• Power/Ground Plane Pair
• Summary
PDN in a Multi-Layer PCB

- DC/DC converter (Power source)
- SMT capacitors
- GND
- VCC
- IC load
- Electrolytic capacitor
- IC driver
- Electrolytic capacitor
- PCB trace
- P-MOS
- N-MOS
- IC driver
- IC load
- VCC
- VDC
- GND
- Switch
- PCB trace
- Z_0, V_p
- CL
Device Switching

Shoot-through current only

Shoot-through + load charging current

Current Supply and Power Bus Noise

I am Mr. Charge!
PDN Design Objectives

1. Ensure charge supply for logic transitions
   - Enough capacitance to store charge
   - Enough charge readily available for short transitions

2. Minimize noise voltage distribution on the $V_{CC}$/GND plane pair
   - Low power bus impedance over frequency
   - Noise decoupling
   - Noise isolation
PDN Design Issues in PCB

- Capacitor interconnects;
- Individual capacitor values and packaging forms;
- Number of capacitors needed;
- Capacitor placement;
- PCB stack-up;
- Power/ground plane pair geometry;
- Segmentation and isolation
PDN Charging/Discharging Hierarchy

The planes can be regarded as a $C$ only @ low frequencies.
PDN Impedance Profile

- Frequency [GHz]
- $Z_{21}$ [dBΩ]

- Power plane distributed behavior
- Global decoupling
- Local decoupling
- Bulk cap
Outline

Interconnect Inductance
- shall be minimized in any situation
Effect of Inductance

Inductance – impedes the flow of current (charge) to the load that will charge it to achieve a logic 1

\[ Z = R + j \omega L + \frac{1}{j \omega C} \]

\[ f_{res} = \frac{1}{2\pi \sqrt{LC}} \]

\[ i(t \geq 0) = V_s \sqrt{\frac{C}{L}} \sin\left(\frac{t}{\sqrt{LC}}\right) \]
Minimizing Interconnect Inductance

SMT Decoupling Capacitor

ESL

Loop 1 $\rightarrow$ $L_{\text{via}}$

Loop 2 $\rightarrow$ $L_{\text{above}}$

SMT Capacitor

Via

Capacitor Pads

The “Good”

The “Better”

The “Best”

Really “Ugly”

The “Ugly”

The “Bad”
Individual Capacitor Values

- multiple values or maximum value? May not matter

\[ f_{res} = \frac{1}{2\pi \sqrt{LC}} \]
Two Common SMT Decoupling Strategies

- **Use an array of capacitor values:**
  - This may be the best known approach and is very popular in the signal integrity design community (SI-LIST).
  - Rationale: to maintain a flat impedance profile below a target impedance over a wide frequency range
  - Typically a logarithmically spaced (10, 22, 47, 100, 220, 470nF, etc.) array of 3 values per decade.

- **Use the largest capacitor value in the package size**
  - This is less well-known, but a popular approach in the EMI design community
  - Rationale: to keep impedance as low as possible, less emphasis on a target impedance and a flat profile
Different Approaches : Comparison

- **Approach A**: values of decoupling capacitors logarithmically spaced, i.e. 3 values per decade: 10, 22, 47, 100, etc.

- **Approach B**: largest values of decoupling available in two package sizes, i.e., 0603 and 0402

- **Approach B1**: largest values of decoupling available in one package size, i.e., 0402.

**Both approaches can meet the design specs relative to the target impedance**
Outline

Capacitor Location
- could be important due to PCB geometry
Background

- Does capacitor location matter?
- How close is close?
- What if capacitors can’t be placed close enough to the IC pwr/gnd pins?
- Is it worth sacrificing routing or using costly new technology in order to get capacitors closer?
- Need a way to facilitate engineering judgment
Location Affects Interconnect Inductance

Interconnect inductance is reduced when the cap is moved closer to the IC
⇒ The capacitor becomes more effective

\[ Z = R + j \omega L + \frac{1}{j \omega C} \]

\[ f_{res} = \frac{1}{2\pi \sqrt{LC}} \]

\[ i(t \geq 0) = V_s \sqrt{\frac{C}{L}} \sin\left(\frac{t}{\sqrt{LC}}\right) \]
Local Decoupling Effect – Frequency-Domain

Equivalent circuit at high frequencies

\[ Z_{21} = \frac{V_2}{I_N} \]
\[ Z'_{21} = \frac{V_2}{I_1} \]
\[ Z'_{11} = \frac{V_1}{I_1} \]

\[ \frac{Z_{21}}{Z'_{21}} = \frac{I_1}{I_N} = \frac{j\omega(L_2 + L_3 - M)}{j\omega(L_2 + L_3) + Z'_{11}} \approx \frac{(1-k) + \frac{L_2}{L_2}}{1 + \frac{L_3}{L_2}} \]
Local Decoupling Effect – Frequency-Domain

- Increasing series resonant frequency of decoupling capacitor
- Reducing impedance uniformly in a frequency-independent manner (approximately) for frequencies higher than the series resonant frequency
Local Decoupling Effect – Time-Domain

Equivalent circuit at early time $(t ≈ 0)$

\[ M \frac{di_1(t)}{dt} \approx (L_2 + L_3 - M) \frac{di_2(t)}{dt} \]

\[ i_1(t) = \frac{L_2 + L_3 - M}{L_2 + L_3} i_N(t) \]

\[ (1 - k) + \frac{L_3}{L_2} \approx \frac{L_3}{1 + \frac{L_3}{L_2}} i_N(t) \]
Local Decoupling Effect – Time Domain

Reducing initial noise voltage generated in the power bus due to logic transitions.
Local Decoupling Effect – Charge Delivery

![Diagram](image)

- \( \varepsilon_r = 4.5 \)
- \( \mu_r = 1.0 \)
- \( s = 5.8 \times 10^7 \)
- \( \tan \delta = 0.02 \)

\[ C_{dec} = 1 \mu F \]
\[ L_3 = \{ 0.5, 1.0, 2.0, 3.0 \} nH \]
\[ R_{dec} = 30 \Omega \]
\[ X = \{ 50, 400, 5000 \} \text{ mils} \]

35 mil (0.889mm) thick

10 mil (0.254 mm) thick
Estimating Local Decoupling Effect

Closed-form expressions derived from the radial transmission-line theory:

\[ L_2 = \frac{\mu_0 d}{2\pi} \left[ \ln \left( \frac{R_{\text{equiv}}}{r} \right) - 0.75 \right] \]

\[ k \approx \frac{\ln \left( \frac{R_{\text{equiv}}}{s + r} \right) - 0.75}{\ln \left( \frac{R_{\text{equiv}}}{r} \right) - 0.75} \]

\[ \Delta |Z_{21}| (dB) \approx 20 \log_{10} \left[ (1 - k) + \frac{L_3}{L_2} \right] \]

accounting for fringing effect

\( d \) – PWR/GND plane pair spacing
\( r \) – via radius
\( R_{\text{equiv}} \) – equivalent radius of power bus
\( s \) – spacing between two vias

For a rectangular power bus, \( R_{\text{equiv}} \approx \frac{a + b}{4} \)

assumption: vias are located close to the center of the planes

Estimating Local Decoupling Effect

\[ L_3' = L_{\text{via}} + L_{\text{trace}} \]

where \( L_{\text{via}} = 2 \left( L_{ps} - M_{ps} \right) \)

and \( L_{\text{trace}} = L_t - M_t \)

\[
M_{ps} = \frac{\mu_0}{2\pi} h_s \left\{ \ln \left[ \frac{h_s}{l} + \sqrt{1 + \left( \frac{h_s}{l} \right)^2} \right] + \frac{l}{h_s} - \sqrt{1 + \left( \frac{l}{h_s} \right)^2} \right\}
\]

\[
L_{ps} = \frac{\mu_0}{2\pi} h_s \left\{ \ln \left[ \frac{h_s}{r} + \sqrt{1 + \left( \frac{h_s}{r} \right)^2} \right] + \frac{r}{h_s} - \sqrt{1 + \left( \frac{r}{h_s} \right)^2} \right\}
\]

\[
L_t = \frac{2 \times 10^{-7}}{3w^2} \left[ 3w^2 \ln \left( \frac{l + \sqrt{l^2 + w^2}}{w} \right) + 3l^2 \ln \left( \frac{w + \sqrt{w^2 + l^2}}{l} \right) \right]
\]

\[
- \frac{2}{3} \left( w^2 - 2p^2 + l^2 \right) \sqrt{w^2 + p^2 + l^2}
\]

\[
+ l \left( w^2 - p^2 \right) \ln \left( \frac{l + \sqrt{l^2 + w^2 + p^2}}{-l + \sqrt{l^2 + w^2 + p^2}} \right)
\]

\[
+ \frac{2}{3} \left( w^2 - 2p^2 \right) \sqrt{w^2 + p^2}
\]

\[
+ l^2 w \ln \left( \frac{w + \sqrt{w^2 + p^2 + l^2}}{-w + \sqrt{w^2 + p^2 + l^2}} \right)
\]

\[
- 4wp \cdot \tan^{-1} \left( \frac{wl}{p\sqrt{w^2 + p^2 + l^2}} \right)
\]

\[
+ \frac{2}{3} \left( l^2 - 2p^2 \right) \sqrt{l^2 + p^2}
\]

\[
+ p^2 l \ln \left( \frac{l + \sqrt{l^2 + p^2}}{-l + \sqrt{l^2 + p^2}} \right) + \frac{4p^3}{3}
\]

\( l \): separation between two via;

\( h_s \): height of the capacitor from the nearest power or ground plane;

\( w \): width of the trace connecting two vias, or width of the capacitor package if no trace;

\( r \): radius of the via; and \( p = 2h_s \).

Validated with CEMPIE

Design Implications

**Dos**

**Don’ts**

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Design Implications

The ratio of $L_3/L_2$

- A good indicator of the ability of a power bus to support local decoupling
- The lower, the better
- Can be greatly increased by even very short trace length from via to pad

<table>
<thead>
<tr>
<th>PWR/GND pair thickness</th>
<th>$L_3'$ (nH)</th>
<th>$L_3/L_2$ with no trace</th>
<th>$L_3/L_2$ w/extra 100 mil trace length</th>
<th>$L_3/L_2$ w/extra 200 mil trace length</th>
<th>$L_3/L_2$ w/extra 300 mil trace length</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 mils</td>
<td>1.66</td>
<td><strong>6.75</strong></td>
<td>9.13</td>
<td><strong>11.50</strong></td>
<td>13.88</td>
</tr>
<tr>
<td>35 mils</td>
<td>0.92</td>
<td><strong>1.29</strong></td>
<td>1.98</td>
<td><strong>2.67</strong></td>
<td>3.36</td>
</tr>
</tbody>
</table>

Tabulated values for
- Centered power bus in a 62 mil PCB stack-up
- 10 mil via diameter
- 0603 SMT capacitor package
Design Implications

The placement of de-cap (obverse or reverse), can be highly dependent on the position of power bus in PCB stack-up.

<table>
<thead>
<tr>
<th>SMT de-cap Placement</th>
<th>$L_3'$ (nH)</th>
<th>$L_3/L_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Obverse</td>
<td>0.45</td>
<td>2.96875</td>
</tr>
<tr>
<td>Reverse</td>
<td>2.56</td>
<td>9.5625</td>
</tr>
</tbody>
</table>

Always LEAST above-plane inductance!
Power/Ground Plane Pair

- thin is always better
Impedance of the Power/Ground Plane Pair

Based on the cavity method:

\[ Z_{ij}(\omega) = \frac{1}{j\omega C_{\text{plane}}} + j\omega \mu d \]

\[ \sum_{m=0}^{M} \sum_{n=0}^{N} \left( \varepsilon_{m}^{2} \varepsilon_{n}^{2} \right) (k_{nm}^{2} - k_{m}^{2}) \frac{f(x_i, y_i, x_j, y_j)}{ab} p(L_{xi}, L_{xj}, L_{yi}, L_{yj}) + j\omega L_{ij}^{HM} \]

\[ Z_{ij}(\omega) \propto d \]

Power Bus Thickness Effects on Decoupling

Frequency domain: impedance
Power Bus Thickness Effects on Decoupling

Time domain: port voltages

Port 1 current

Port 1 (3 in, 2 in)

Port 2 (7 in, 4 in)

Port 1

Port 2

b = 10 in

d

a = 12 in

Current (A)

Time (ns)

Port 1 voltage (mV)

Time (ns)

Port 2 voltage (mV)

Time (ns)

Port 1 voltage (mV)

Time (ns)

Port 2 voltage (mV)

Time (ns)

d = 1 mil

d = 5 mils

d = 10 mils

d = 40 mils

Current (A)

Time (ns)

Port 1 voltage (mV)

Time (ns)

Port 2 voltage (mV)

Time (ns)
Power Bus Thickness Effects on Decoupling

35 mil (0.889mm) thick

10 mil (0.254 mm) thick
## Effect of Typical Laminates on Decoupling

<table>
<thead>
<tr>
<th>Dk</th>
<th>Loss Tangent</th>
<th>Thickness, d</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.4</td>
<td>0.02</td>
<td>4, 10, 35 mils</td>
<td>better quality fiberglass/epoxy resin material</td>
</tr>
<tr>
<td>4</td>
<td>0.02</td>
<td>2 mils</td>
<td>patented thin FR4 core, widely used.</td>
</tr>
<tr>
<td>16</td>
<td>0.006</td>
<td>16 microns (0.63 mils)</td>
<td>ultra-thin material commercially available</td>
</tr>
<tr>
<td>20</td>
<td>0.015</td>
<td>0.2 mils</td>
<td>ultra-thin material from [7, 8].</td>
</tr>
</tbody>
</table>

Embedded capacitance (thin laminate) has superior electrical performance
Summary

- **Interconnect inductance shall be minimized in any situation:** inductance limits the effectiveness of decoupling.

- **Individual capacitor values may not matter:** using an array of capacitor values or the largest value in a package size meets design specifications.

- **Capacitor location could be important due to PCB geometry:** thin power bus structures (< 10 mils) usually result in a larger \( \frac{L_3}{L_2} \) value; thus capacitor location is relatively unimportant. Thick power bus structures usually result in a smaller \( \frac{L_3}{L_2} \) value, and capacitor placement can be an important design factor.

- **Thin power/ground plane pair is always better:** low impedance and high charge availability.