Thermal Stability of Barrier Layers for Copper Metallization

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Abstract— **Sheet resistance measurements were performed on four different barrier schemes, to test the thermal stability of parylene and TiN as barrier layers for copper metallization. The samples used in this study, were stacked Cu/TiN/parylene/Si structures annealed at 200°C for 2 hours. The samples had two different thicknesses of TiN (110nm and 220nm), two different thicknesses of parylene (650nm and 1050nm) with 500nm of copper on them. Results show that the thick TiN had no significant change in sheet resistance whereas the thin TiN samples showed instable values of sheet resistance. Scannning Electron Microscopy (SEM) was used to observe the surface morphology.**

I. Introduction

THE current advances in integrated circuit technology emphasize increasing device speeds and reducing device sizes. This need for increased device speed and functionality while minimizing die size can be achieved with three dimensional (3D) packaging technologies. One approach to 3D stacking of electronic devices is achieved using through-wafer interconnects (TWIs), where vias provide electrical connection between the stacked chip levels.

Interconnection performance is critical in determining the overall package performance. This is because the interconnect signal delay, or RC time delay, has become more significant than the gate delay [1]. Therefore materials with low electrical resistance are desired to reduce the RC delay. During the past decades, aluminum was widely used as the interconnect material. Now, copper has received much attention as the new interconnect material in ultra large scale integrated (ULSI) devices. This increasing interest is due to copper's high electrical conductivity and electromigration resistance. This superior resistance to electromigration has allowed metal lines to be thinner using copper, leading to lower power consumption.

However, there are some well known disadvantages of using copper. Copper has a tendency to "bleed" into silicon and can diffuse quickly in a wafer even at room temperature. It can diffuse in 15 hours through a standard 4 in. p-type boron doped 10 Ω cm Si. Copper thus diffuses and introduces deep electronic levels into the silicon band gap which results in the reduction of minority carrier lifetime. This ultimately leads to degradation of device performance. The fast diffusivity of copper in silicon is due to its small ionic radius, weak interaction with the silicon lattice and the interstitial location of copper in silicon.

To prevent the deterioration of devices, a diffusion barrier is necessary between any copper metallization and the silicon substrate. Among many materials used as diffusion barriers, titanium nitride (TiN) is attractive due to its thermal stability. But one still needs to find the stability of the diffusion barrier at the temperature of interest and if possible know the maximum annealing temperatures and durations which the metallization layer can withstand without the die being compromised. Copper, the fastest metal diffuser in silicon can contaminate a portion of, or the entire die, even with a small penetration spot due to a defect in the barrier layer. Thus it is critical that the diffusion barrier layer deposited is homogenous through out the wafer. It has been shown [2] that changes in sheet resistance of copper films deposited on barrier structures indicates a failure of the barrier.

II. Experimental Procedures

This work examined samples consisting of stacked Cu/TiN/parylene/Si structures, as shown in Fig. 1, with varying thicknesses of TiN and parylene.

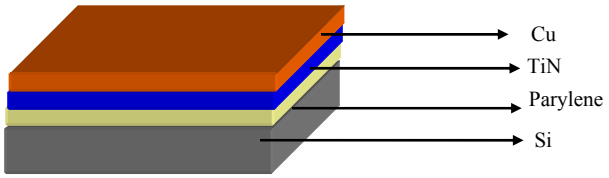

Fig. 1. Stacked structure of the sample.

Parylene is used as an electrical insulating layer to minimize current leakage from copper through-wafer interconnects. This work will examine the efficacy of parylene and TiN barrier layers. The samples are 2 x 2 cm^2 with two different thicknesses of TiN and parylene with a copper thickness of 500nm. Four different barrier schemes were explored as described in table 1.

TABLE I
BARRIER SCHEMES

Sample No.	Parylene Thickness (nm)	TiN Thickness (nm)	Copper Thickness (nm)
# 1	650	220	500
# 2	650	110	110
# 3	1050	220	500
# 4	1050	110	500

III. RESULTS AND CONCLUSION

The sheet resistance of Cu/TiN/parylene/Si structures was determined under a N_2 ambient for 2 hours at room temperature and at 250°C. The measured sheet resistance is dominated by copper and an abrupt increase indicates the instability of the barrier layers. There was no significant change in sheet resistance for the thick TiN diffusion barriers. However, thin TiN samples showed sheet resistance instability. Figures 2 and 3 compare the sheet resistance at room temperature and at 250°C for the thick TiN, figures 4 & 5 show the data for the thin TiN. Scanning electron microscopy was used to examine surface morphology before and after annealing. EDS analysis will be performed on areas that show surface irregularities after annealing.

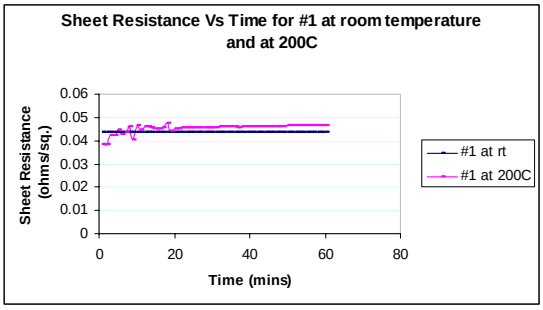

Fig. 2. Sheet Resistance of Cu with 650nm/220nm thickness of parylene/TiN

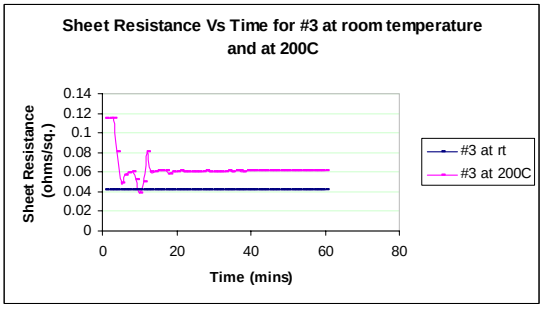

Fig. 3. Sheet Resistance of Cu with 1050nm/220nm thickness of parylene/TiN

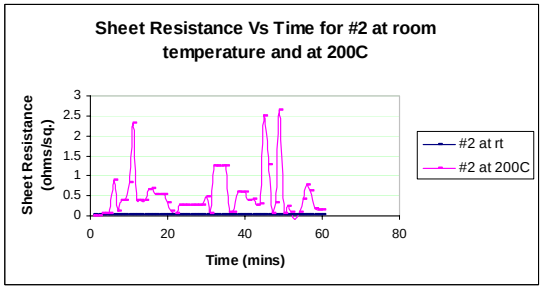

Fig. 4. Sheet Resistance of Cu with 650nm/110nm thickness of parylene/TiN

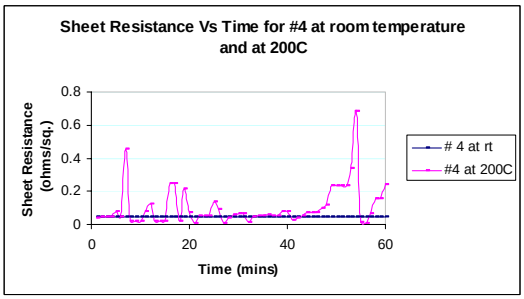

Fig. 5. Sheet Resistance of Cu with 1050nm/110nm thickness of parylene/TiN.

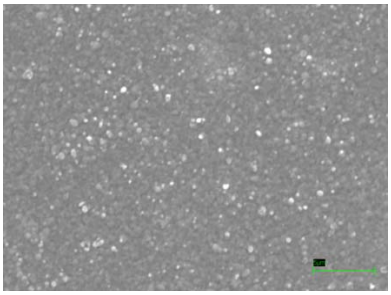

Fig. 6. SEM photograph of the surface of 650nm/110nm parylene/TiN at room temperature

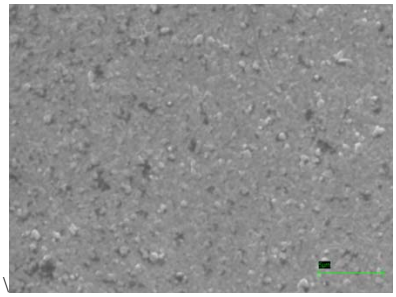

Fig. 7. SEM photograph of the surface of 650nm/110nm parylene/TiN after annealing at 200°C.

REFERENCES

[1] Baozhen Li, Timothy D Sullivan, Tom C lee, and Dinesh Badani, "Reliability challenges for copper interconnects," *Microelectronics Reliability*., vol. 44, pp. 365–380, 2004.

[2] Sa-Kyun Rha, Seung Yun Lee, Won-Jun Lee, Yong-Sup Hwang and Chong-Ook Park, "Charateization of tiN barriers against Cu diffusion by capacitance-volatge measurement" J. Vac. Sci. Technol. B 16(4), pp.2019-2025, Jul/Aug 1998.