Reliability of a Semiconductor Power Switch in a Power Electronics Converter

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Today’s Topics for Discussion

- Current methodology used to design power converters
- Current approach used to assess semiconductor power switch reliability in a power converter
- **Case study:** Lessons learned from extensive field-reliability investigation of high-density power supplies
- Silicon vs. Wide Bandgap (WBG) power devices – Future of WBG power devices
- **Moving forward:** How to design power converters with “built-in” field-reliability
Current reliability assessment methods are only good to evaluate infant mortality.
“Field-reliability” of a power converter is among the least understood topics today!

We are not able to design power converters with “built-in” field-reliability!
What is Needed?

Information vs. Power Processor

Information Age

- MTBF > 100,000 hrs.
- "End-of-Life" = 17 years
- Increased switching speed at reduced power consumption

Energy Age

- MTBF > 1,000,000 hrs.
- "End-of-Life" = 125 years
- Increased energy efficiency with smaller profile

Cost

- Increased efficiency at reduced cost

"End-of-Life" = 125 years
Trends in Power Conversion

- Increased current density, higher switching frequency, and higher $T_{j\text{max}}$
- Higher system integration
- Increased power density
- Increased cooling density

Smaller converter, lower cost and higher efficiency
Today’s Power Converter Design Approach

Current sourced by the load (drive motor) under specified field operating conditions determines heat generated within chips.

Power Chip in an OEM – $T_{j\text{max}}$ to $T_a$

Miniaturization demands high-frequency power conversion and system integration
Today’s Semiconductor Power Switch Reliability Assessment Approach

• High-Temperature Reverse Bias (HTRB) Test
• High-Temperature Gate Bias (HTGB) Test
• Temperature Humidity Bias (THB) Test
• Thermal Cycling (-40°C to 125°C)
• Power Supply Operating Life Test
The HTRB Test

- Test performed to accelerate failure mechanisms

- Typical stress conditions are:
  - $T_a = 125^\circ C$ to $150^\circ C$
  - $V_{dc} \geq V_{BR}$

- Test duration ~ 1000 hours

- Failure rate ($\lambda$) is estimated by considering the dependence on temperature (T), relative humidity (RH) and electric field (E)

$$\lambda = A e^{\frac{\phi}{kT}} e^{\frac{B}{RH}} e^{CE}$$
EPC eGaN® FET Reliability - Example

Figure 1A: Weibull Plots for \( R_{\text{DS(on)}} \) Failure (150°C)

Figure 1B: Time to Failure vs. \( V_{\text{DS}} \) (150°C)

\[ R(t) = R_0 \left( \alpha + \beta \ln[t] \right) \]

Reliability of High-End Computer Server Power Supplies – a Case Study
Failures of Computer Supplies

- IBM eServer 900
- 30% volume taken by PS
- 10% volume by cooling

ROAD BLOCK!

Power loss in components and packaging!

10 kW Power Supply
50 kHz to 75 kHz = 50% reduction in size

P. Singh et.al., *IBM J. Res. & Dev.*, Nov. 2002
At UI-Chicago (1995-2004)

Founded and directed world’s first industry-university-government consortium to improve power supply reliability (1998-2004)

Fig. 1. Zinc whiskers are typically 1 μ in diameter and 0.5-2 mm in length.

Fig. 2. A magnified view of an arc between the drain and source solder pads of a MOSFET. In this example of field arcing, the arc damage was difficult to detect with the unaided eye.

**Power Supply Arcing**

**Fig. 3.** Paschen’s law.

**Partial Vacuum Test** – identifies location of failure

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Power Supply Arcing

Zinc Whisker Spray Test – identifies minimum spacing between features

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**Fig. 6.** Pressure at arc for TO220 and TO247 MOSFETs as a function of drain-to-source dc voltage.

**Fig. 7.** Coupon experiment solder pad features spaced 0.5 mm apart. Note the alignment of zinc whiskers with the electric field.

**TABLE II**

<table>
<thead>
<tr>
<th>Solder pads gap</th>
<th>Arc voltage without zinc whiskers</th>
<th>Arc voltage with zinc whiskers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5 mm</td>
<td>~3000 V</td>
<td>~1800 V</td>
</tr>
<tr>
<td>1.0 mm</td>
<td>~4000 V</td>
<td>No arc up to 5000 V</td>
</tr>
<tr>
<td>1.5 mm</td>
<td>No arc up to 5000 V</td>
<td>No arc up to 5000 V</td>
</tr>
</tbody>
</table>

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Safe Operating Area (SOA) Degradation

Zero voltage transition (ZVT) boost converter

High turn-off $dv/dt$ and avalanche stress on $Q_2$

Degradation of transfer curve of $Q_2$ with time

Degradation of SOA of $Q_2$ with time

N. Keskar, M. Trivedi and K. Shenai, IEEE IAS Digest, pp. 1098-1102, 1999
Silicon MOSFET Failures due to Dynamic Avalanching

Accelerated HTRB Stress Test

Power MOSFET Failure: Effect of Die Size

SEB Failure Rates of 1000V Silicon Power MOSFETs

<table>
<thead>
<tr>
<th>%/WK FAILS</th>
<th>70</th>
<th>75</th>
<th>80</th>
<th>85</th>
<th>90</th>
<th>95</th>
<th>100</th>
<th>ACTIVE AREA</th>
<th>DIE SIZE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000 APT - 4</td>
<td>0.0006</td>
<td>0.0041</td>
<td>0.028</td>
<td>0.197</td>
<td>1.146</td>
<td>2.70</td>
<td>3.93</td>
<td>0.16</td>
<td>4</td>
</tr>
<tr>
<td>1000 APT - 5</td>
<td>0.0011</td>
<td>0.0079</td>
<td>0.054</td>
<td>0.379</td>
<td>2.210</td>
<td>5.21</td>
<td>7.58</td>
<td>0.32</td>
<td>5</td>
</tr>
<tr>
<td>1000 APT - 6</td>
<td>0.0016</td>
<td>0.0117</td>
<td>0.080</td>
<td>0.562</td>
<td>3.277</td>
<td>7.73</td>
<td>11.24</td>
<td>0.47</td>
<td>6</td>
</tr>
<tr>
<td>1000 APT - 7</td>
<td>0.0035</td>
<td>0.0250</td>
<td>0.170</td>
<td>1.200</td>
<td>7.000</td>
<td>16.50</td>
<td>24.00</td>
<td>1.00</td>
<td>7</td>
</tr>
</tbody>
</table>

EXTRAPOLATED DATA - RATIO BY ACTIVE AREA

Actual measured data down to 83% of rated voltage
No data for lower stresses due to very low failure rates

Low-level leakage results in significant device de-rating.

Field-Failures of Power MOSFETs in Power Supplies

Residual material defects in silicon caused field-failures of power MOSFETs in high-end server power supplies

Silicon IGBT Failures During Short-Circuit and Inductive Switching Conditions – Simultaneous High-Voltage and High-Current Situation
Short Circuit Failure in Silicon IGBTs

Failure after 18 $\mu$s

Silicon IGBT Failure Under Clamped Inductive Stress

Physics of “Hot Spot” Formation

Poynting vector \( S = E \times H \)

Dipole radiation pattern

Energy conservation law

\[
\frac{\delta u}{\delta t} = -\nabla (S) - J \cdot E
\]

\( u = \frac{1}{2} (E.D + B.H) \)

Electric field strength (color)
Poynting vector (arrows)

Si vs. WBG Power Devices – Future of WBG Power Devices
System-Level Benefits of WBG Power Devices

- Shenai’s Figure of Merit -
  \[ Q_{F2} = \lambda \sigma_A E_M \]
  2400x improvement

- Silicon Power Switch
  - Volumetric: 50,000 cm³
  - Weight: 18 kg

- WBG Power Switch
  - Volumetric: 4,500 cm³
  - Weight: 0.2 kg

WBG Power Switch for

- Increased energy savings
- Reduced system cost
- Robust & reliable system


At the system level, the objective should be to increase power and cooling densities.
Smaller Chip : Lower Cost
## Si vs. WBG Material Properties

<table>
<thead>
<tr>
<th>Electrical Property</th>
<th>Si</th>
<th>SiC (4H)</th>
<th>SiC (6H)</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Gap Energy (eV)</td>
<td>1.12</td>
<td>3.28</td>
<td>2.96</td>
<td>5.5</td>
</tr>
<tr>
<td>Critical Electrical Field (MV/cm)</td>
<td>0.29</td>
<td>[2.5]</td>
<td>3.2</td>
<td>20</td>
</tr>
<tr>
<td>Electron Mobility (cm(^2)/VS)</td>
<td>1200</td>
<td>800</td>
<td>370</td>
<td>2200</td>
</tr>
<tr>
<td>Hole Mobility (cm(^2)/VS)</td>
<td>490</td>
<td>115</td>
<td>90</td>
<td>1800</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cmK)</td>
<td>1.5</td>
<td>[3.8]</td>
<td>3.8</td>
<td>20</td>
</tr>
<tr>
<td>Maximum Junction Temperature (°C)</td>
<td>150</td>
<td>[600]</td>
<td>600</td>
<td>1927</td>
</tr>
</tbody>
</table>
Wide bandgap (WBG) semiconductors, such as SiC and GaN devices, offer superior electrical and thermal performances compared to silicon.

Status of Commercial WBG Power Devices

• Vertical SiC JBS Power Diodes
  \[ 300 \text{ V} < V_{BR} < 1700 \text{ V} \]

• Lateral Low-Voltage \( (V_{BR} < 650 \text{ V}) \) GaN Power Transistor

• Vertical High-Voltage \( (900 \text{ V} < V_{BR} < 1700 \text{ V}) \) SiC Power MOSFET

Cost of WBG device is 2-3X higher than that of Si device

Circuit design complexities – Gate driver issues

System-level benefits of WBG devices are minimal

WBG device field-reliability is unknown
SiC Wafers – Current & Future

Growth Temperature
- Silicon: < 1000°C
- SiC: > 2000°C

Method
- Silicon: Czochralski
- SiC: PVT

Defect Density
- Silicon: < 1/cm²
- SiC: Very High

Cost
- Silicon: Low
- SiC: Very High
Defect Engineering of 4H-SiC Wafers

BPD Density (cm$^{-2}$)

TSD Density (cm$^{-2}$)

TED Density (cm$^{-2}$)

Dislocation Density (cm$^{-2}$)
Defects in State-of-the-Art Commercial 4H-SiC Wafers

High resolution synchrotron monochromatic X-ray topographs recorded at Argonne’s Advanced Photon Source (APS) facility. (a) Back-reflection X-ray topograph \((g = 0004)\) images of close-core threading screw dislocations (TSDs) and basal plane dislocations (BPDs) in a \((0001)\) 4H SiC wafer; (b) Grazing incidence X-ray topograph \((g = 11-28)\) of 4H-SiC substrate showing TSDs (right and left handed) and TEDs; (c) Transmission X-ray topograph showing the images of BPDs.
Formidable Material Challenge

Growth in the c-axis direction, enabled by screw-dislocations providing steps!

Vertical (c-axis) 4H-SiC boule growth proceeds from top surface of large-area seed via hundreds to thousands of threading screw dislocations (TSDs).


Threading screw dislocation growth spirals (THE sources of steps for c-axis growth) found at top of grown 4H-SiC boule.

Contention: Elimination of screw dislocations from power devices not possible while maintaining commercially viable crystal quality and growth rate and via this approach.

Crystal grown at T > 2200 °C --> High thermal gradient & stress --> More dislocations
Role of Crystal Defects on the Electrical Characteristics of PiN Diode
Avalanche Testing of Power Devices

First proposed by Shenai
C. S. Korman et al, in Dig. Int. High-Frequency Power Conversion, pp. 128-139, 1988
Measured Avalanche Energy ($E_{AVL}$) of Power Diodes

- **600V/8A 4H-SiC JBS diode**
- **600V/6A silicon MPS diode**

Why $E_{AVL}$ of SiC Power Diodes < $E_{AVL}$ of Si Power Diodes?

Most WBG data sheets do not list $E_{AVL}$

First demonstrated by Shenai
Measured $dv/dt$ of SiC Power Diodes

**Why $dv/dt$ Capability of SiC Power Diodes < $dv/dt$ Capability of Si Power Diodes?**

Most WBG data sheets do not provide $dv/dt$ ratings

First demonstrated by Shenai’s group


**Measured $dv/dt$ of SiC Power Diodes**

$T_c = 25^\circ$C

SW2: 600V/6A 4H-SiC JBS diode
PD2: 600V/8A silicon MPS diode

SD1: 300V/10A 4H-SiC JBS diode
SW1: 200V/12A silicon MPS diode
Safe Operating Area (SOA) of Power MOSFETs

**Why SiC SOA is smaller than silicon?**

4H-SiC Material Defects and MOS Gate Oxide Reliability

Commercial SiC JBS Diodes

Measured @ 25°C

- (600 V)
- (1200 V)
- (1700 V)

Reverse Current (A)

Reverse Voltage (kV)

600 V

1200 V

1700 V

Punch-through Design

Silicon

Avalanche breakdown
Minimum on-resistance

SiC

Punch-through (leaky)
Not optimized

Too much fat left in SiC diodes

Field-Induced Lattice Deformation in 600V 4H-SiC JBS Diode

Defect delineation study performed using hard X-rays at Argonne’s Advanced Photon Source (APS).

At 900V reverse bias, TSDs in the vicinity of the metal-semiconductor junction were excited and acted as charge generation centers that led to diode breakdown.

Collaborators:

Stony Brook University
Brookhaven National Labs

K. Shenai – unpublished work, 2014
Lessons from the Past:

Higher chip cost and thermal limitations rendered GaAs chip technology always a technology of the future.
Why Power Electronics Converters Fail in the Field?
Why Power Supplies Failed in the Field?

Output capacitor leakage; reactive charge dumping from transformer leakage inductance; power supply arcing caused by zinc whiskers

Failures in Electronic Systems

What is the Junction Temperature $T_j$?
**Question**: Please indicate which components you consider most important to be addressed by future research to improve the reliability of power electronics converter systems?

Question: Please rank the following options for achieving high reliability for power electronics systems?

Physics of Failures

What is the role of material defects on cost, performance and reliability of a semiconductor power switch?
Power Semiconductor Switch

- **Load is inductive**

- **i_L(t)**, **di_L(t)/dt**

- **v_{AB}(t)**, **dv_{AB}(t)/dt**

- **Low on-state resistance** ($R_{DS(ON)}$)
  - to reduce conduction power loss
    ($I^2 R_{DS(ON)}$)

- **Low capacitances**
  - to reduce switching power losses
    ($CV^2f$)

- **Good reliability**
- **Low chip cost**
Power converters are designed by considering mainly $P_{ON}$
Drift-Region Design

Source (S)

$p$-body

$n^+$ source

$n^-$ epi

$n$ buffer

$n^+$ substrate

Gate (G)

Drain (D)

$C_{GS}$

$R_G$

$R_W$

$C_{GD}$

$R_D$

$C_{DS}$

$E$

$E_c$

$N_{DR}$

$N_{SUB}$

$W_{DR}$

$t_{SUB}$

PN junction

Current flow
On-State Power Dissipation

\[ \Delta T = T_j - T_c = I_{ON}^2 R_{ON} R_{jc} \]

\( T_{jmax} = 150^\circ C \) is “industry standard”

\( > 200^\circ C \) is desired
Thermal Management of WBG Power Devices

Silicon Substrate (~ 200 microns)

GaN (< 1 micron)

2DEG

AlGaN Buffer (a few microns)

Heat Source

SiC Substrate (~ 350 microns)

SiC (few microns)

Lateral GaN Power Transistor

Vertical SiC Power Transistor
Moving Forward: How to design power converters with “built-in” field-reliability?

Industry-Driven Consortium

Major OEMs

- EV
- Grid
- Aerospace
- Computer/Telecom
Need to Account for Material – Device – System Interactions

Top-down systems-driven reliability engineering approach
Systems-Driven Reliability Engineering

OEMs  
Motor Control, Utility Grid, EVs, Power Supplies, etc.

Converter Suppliers  
Inverters & DC-DC Converters

Switch & Module Manufacturers  
Power Semiconductor Chips & Modules

Material Suppliers  
SiC & GaN Wafers

Cost (T<sub>a</sub>, MTBF)

Power Density (Cooling Density)

Current Density (T<sub>jmax</sub> & V<sub>BD</sub>)

Defect Density (Growth Rate & Wafer Size)
QUESTIONS?

Thank You
OPTIONAL SLIDES
What is Reliability?

- Reliability =
  - measure of continuous service accomplishment (or time to failure)
- Metrics
  - Mean Time To Failure (MTTF) measures reliability
  - Failures In Time (FIT) = 1/MTTF, the rate of failures
    - Traditionally reported as failures per $10^9$ hours of operation
    - Ex. MTTF = 1,000,000 hours, FIT = $10^9/10^6 = 1000$
  - Mean Time To Repair (MTTR) measures Service Interruption
  - Mean Time Between Failures (MTBF) = MTTF + MTTR
The Famous “Bathtub” Curve

Quantification of a System’s Reliability

- Probability Density Function
  - $F(x)$ is the probability that the number of failures is ‘$x$’
  - “Smoothed Out” version of a histogram depicting number of failures
- Failure Rate
  - $\lambda$ is the instantaneous failure rate at operating time ‘$t$’
  - A decreasing $\lambda$ indicates improvement with time, while an increasing $\lambda$ indicates wear-out and a reduction in reliability over time
- The Bathtub Curve
- Mean Time to Failure
  - $MTTF = \int_0^\infty R(t)\,dt$
- Failure Rate Units
  - FIT = number of devices failing in a billion hours

Component Failure Rate as a Function of Age
Accelerated HTRB Stress Test

<table>
<thead>
<tr>
<th>Device F1 600V/20A</th>
<th>Operating Voltage</th>
<th>Nominal Life (hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>600</td>
<td>172</td>
</tr>
<tr>
<td>2</td>
<td>550</td>
<td>685</td>
</tr>
<tr>
<td>3</td>
<td>500</td>
<td>1561</td>
</tr>
<tr>
<td>4</td>
<td>450</td>
<td>3643</td>
</tr>
<tr>
<td>5</td>
<td>400</td>
<td>8500</td>
</tr>
</tbody>
</table>

- No failures were reported for the following conditions in 15 days of testing
  - 85% stress at room temperature
  - 90% stress at room temperature
  - 85% stress at 125C
  - 90% stress at 125C

- Failures at over 95% and 100% stress at 125C were few and far in-between

Devices operating at higher temperature can be considered more reliable than devices operating at lower temperatures.
- High temperature acceleration testing would result in “failure rate retardation factor”
Weibull Probability Model

- The Weibull Probability Distribution Function is defined as:
  \[ f(T) = \frac{\beta}{\eta} \left(\frac{T - \gamma}{\eta}\right)^{\beta-1} \exp\left(-\left(\frac{T - \gamma}{\eta}\right)^\beta\right) \]
  \(\beta\): shape parameter
  \(\eta\): scale parameter
  \(\gamma\): location parameter

- Assuming \(\gamma = 0\), \(\beta = C = \text{constant}\):
  \[ f(T) = \frac{C}{\eta} \left(\frac{T}{\eta}\right)^{C-1} \exp\left(-\left(\frac{T}{\eta}\right)^C\right) \]

- MTTF:
  \[ T = \gamma + \eta \Gamma\left(\frac{1}{\beta} + 1\right) \]
  \[ \Gamma(n) = \int_0^\infty e^{-x} x^{n-1} \, dx \]

- Reliability and Reliable Life
  \[ R(T) = \exp\left(-\frac{T - \gamma}{\eta}\right) \]
  \[ T_R = \gamma + \eta \left\{ -\ln\left[R(T_R)\right]\right\}^{1/\beta} \]

Engineers at Pratt & Whitney have shown that Weibull modeling is accurate even with a sample size of 3 failures.
Acceleration Parameters

Acceleration Factors and Failure Rate Calculation

- **Voltage Acceleration**
  - $AF_V = \exp [ \beta^* (V_S - V_U)]$
  - $b = 2.5/V$ (voltage acceleration term)
  - $V_U =$ use environment voltage ($V$)
  - $V_S =$ stress environment voltage ($V$)

- **Temperature Acceleration**
  - $AF_T = \exp [ (E_a / k) * (1/T_U - 1/T_S)]$
  - $E_a = 0.70eV$ (activation energy)
  - $k =$ Boltzmann’s constant = $8.617E-5$ eV/°K
  - $T_U =$ use environment temperature (°K)
  - $T_S =$ stress environment temperature (°K)
MOSFET “Field-Reliability” Model

Predicted Failure Rate = Acceleration Factor (AF) x Acceleration Test Failure Rate
SiC MOSFET Gate Oxide Failures

- Pre-screening or burn-in difficult
  - Extrinsic population is Poisson-distributed in area
  - Can’t predict next failure during useful life of device
- Critical reliability issue

Fig. 9. Uncensored Weibull distribution of $4 \times 10^{-4}$-cm$^2$ 4H-SiC capacitors at a temperature of 230 °C and under electric field of 8.9 MV/cm.


Role of Bulk Material Defects on SiC MOSFET Gate Oxide Reliability

- Matocha (2008)
  - No correlation of breakdown and epilayer defects

- Senzaki (2006, 2009)
  - Most of the oxide breakdowns occurred at basal plane dislocations

- Yamamoto (2012)
  - TEDs degrade lifetimes by 1 order of magnitude
  - TSDs degrade lifetimes by 2 orders of magnitude

- Sameshima (2013)
  - Non-uniform oxide thickness (trapezoid and bar-shaped surface defects)