Extreme Power Density Converters - Fundamental Techniques and Selected Applications

Robert Pilawa-Podgurski
University of Illinois Urbana-Champaign
PELS Bay Area Chapter Seminar
July 13th, 2017
Acknowledgment
The Goals of Power Electronics

High Power Density
High Efficiency

High Performance Power Converters

High Reliability
Low Cost

Integration of power electronics in systems for overall performance improvements
The Tools of Power Electronics

- Active devices
- Passive devices
- Circuit topologies
- Control
- Integration/Packaging
Conventional Path to High Power Density

Power Converter

Source  \[\pm\]  

Load

Switching frequency vs. Size

Power Loss vs. Switching frequency
Hybrid Switched-Capacitor Converters


Hybrid Switched-Capacitor Converters

Efficiency at max power [%]

Power density [W/in^3]

Conventional

MLC Capacitor
Power Inductor

Current rating [A]

Energy density [J/mm^3]

Voltage rating [V]

Control
Integration/Packaging
Circuit topologies
Active devices
Passive devices
DC-AC and AC-DC Power Conversion
The Importance of DC/AC and AC/DC

Grid Integration of Renewables and Storage

Power Electronics: DC/AC & AC/DC

Credit: Tesla
Credit: Nissan
Credit: iStockphoto

Electric Transportation

Power Electronics: DC/AC & AC/DC

Credit: CAT
Credit: GM
Credit: NASA
Credit: Nissan

Google/IEEE $1M Little Box Challenge

- 2 kW, single-phase 240 V, 60 Hz AC
- Example usage: solar inverter, electric car charger, grid storage integration
- Current state-of-the-art: 95% efficiency, 400 in³.
- Target goal: >95% efficiency, 10x smaller (40 in³)
- $1M prize to winning entry

Prior (lack of!) experience
Our Goal

Develop a radically different solution – make significant research contribution to the field of power electronics. May not win competition, but will have long-term impact.
Original Team

- Chris Barth
  - Integration
  - Mechanical
  - Thermal
  - Capacitor evaluation

- Yutian Lei
  - Inverter design
  - Inverter control

- Shibin Qin
  - Twice-line-frequency buffering
  - System control

$30k funding through Google Academic Grant
Key Technical Challenges

\[ I_{DC} \quad I_{AC} \]

\[ V_{DC} \quad + \quad - \quad V_{AC} \]

\[ E_{store} = \frac{P_{dc}}{2\pi f_{line}} \]
Buffer Solutions

Twice-line frequency power decoupling solutions

- Passive buffering
  - Large volume = poor system power density
  - Poor lifetime

- Active buffering
  - Low efficiency
  - Increased system complexity
  - Higher cost

Passive: dc-link capacitor bank

Active: full-ripple port

Passive: series resonant LC
Passive Series Resonant LC Buffer

At resonant frequency:

\[ 2\omega_L = \frac{1}{\sqrt{L_{ab}C_1}} \]

\[ Z_{buf} = 0 \]

Voltage [V]:
- \( v_{bus} = V_{bus} \)

Current [A]:
- \( i_s = i_{inv,dc} \)
Passive Series Resonant LC Buffer

Express the $2\omega L$ voltage and current components in phasor representation:

$$\tilde{I}_{ab} = i_{ab,ac} = I_{ab} \sin(2\omega_L t)$$

Example: If $C = 100 \text{ uF}$ then $L = 18 \text{ mH}$ for resonance at 120 Hz

Can we implement the resonant buffer without such a large physical inductor?
Passive Component Density

Current rating [A]

Energy density [mJ/mm³]

Voltage rating [V]

Energy density [mJ/mm³]

MLC Capacitor

1000x

Power Inductor
Active Series Resonant LC Buffer

- Use a dc-ac converter with capacitive load to emulate an active inductor
  - Vastly improve power density of passive resonant solution
  - Implement resonant impedance behavior with proper control
  - Series-stacked buffer (SSB) architecture

![Diagram showing series-stacked buffer architecture with active inductor at \(2\omega_L\)]
Buffer Solutions – Series-Stacked Buffer

Benefits:
- High efficiency
- Partial power processing
- High power density

Shortcomings:
- Complex non-intuitive control
- Current sensing and control
- Not a two-terminal device

2 kW SSB, Google Little Box\textsuperscript{[1],[2]}

\[ i_s = I_{S,DC} + \Delta i_s \]

Active Series Resonant LC Buffer

- Dc-ac buffer converter: full-bridge buck
- Practical buffer converter is lossy
  - $V_{C2}$ will gradually decay

$$\tilde{S}_{ab} = \tilde{V}_{ab}\tilde{I}_{ab} = j\tilde{Q}_{ab} + \tilde{P}_{ab}$$

additional real power term
Incorporate practical buffer converter loss with a series resistance, $R_{ab}$, in the equivalent impedance model.
Control Architecture with Loss

Characteristic equations:

\[ \tilde{V}_{ab,j} = -\tilde{V}_{C1} \]
\[ \tilde{V}_{ab,i} = R_{ab}\tilde{I}_{ab} = R_{ab}\tilde{I}_{C1} = R_{ab}C_1 \frac{d}{dt}\tilde{V}_{C1} = \beta \frac{d}{dt}\tilde{V}_{C1} \]
\[ \tilde{V}_{ab} = \tilde{V}_{ab,i} + \tilde{V}_{ab,j} \]

Control architecture:

Voltage/current phasor portrait:

\[ \tilde{V}_{ab,j} \quad \tilde{V}_{ab,i} \]

Power phasor portrait:

\[ j\tilde{Q}_{ab} \quad \tilde{P}_{ab} \]
Experimental Results

N. Brooks, S. Qin, R.C.N. Pilawa-Podurski “Design of an Active Power Pulsation Buffer Using an Equivalent Series-Resonant Impedance Model”, COMPEL 2017 [Best Paper Award]
Hardware Prototype – Energy Density

Design requirement:
- 2 kVA (PF = 0.7~1)
- 400 V ~ 450V bus voltage,
- 10 A peak to peak current

<table>
<thead>
<tr>
<th>Way of measurement</th>
<th>Volume</th>
<th>Power density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rectangular box</td>
<td>4.88 inch^3</td>
<td>410 W/inch^3</td>
</tr>
<tr>
<td>passive component</td>
<td>2.01 inch^3</td>
<td>995 W/inch^3</td>
</tr>
</tbody>
</table>

The highest prior active filtering power density reported was 79.4W/inch^3 by component volume, by Chen et al, TPELS 2013 (120 W, metal film capacitors)

> 99% efficiency across load range
Overall Size Reduction

7-10x size reduction
Key Technical Challenges

\[ E_{store} = \frac{P_{dc}}{2\pi f_{line}} \]
Inverter – Today’s Practice

- High switch voltage stress
- High power loss at high frequencies
- Large inductor

Wide band-gap semiconductors alone will not address these challenges. We need to consider new inverter architectures.
Multi-Level Flying-Capacitor Converter

- Reduced switch voltage stress \([V_{DC}/6]\)
  - Can utilize fast, low-voltage transistors
- Inductor ripple frequency \([F_{SW} \times 6]\)
- Reduced ripple magnitude \([V_{DC}/6]\)

T. Meynard and H. Foch, “Multi-level conversion: high voltage choppers and voltage-source inverters,” PESC ‘92
7-level Flying Capacitor Converter

Challenges

- Capacitor voltage balancing
- Gate driving complexity
- Parasitic inductance (especially with GaN devices)

No demonstrated examples of > 4 level flying capacitor multi-level inverter using GaN transistors, and none switching in the 100’s of kHz at kW levels.
Key Challenge: Parasitic Loop Inductance

100% Overshoot

\[ R_g = 5 \text{ Ohm} \]
Modular Switching Cell

20% Overshoot
\( R_g = 15 \text{ Ohm} \)
Digital Control

- Control objective:
  - Generate correct amplitude
  - Switch only minimum inductance loops
  - Maintain capacitor voltage balance
Prototype #1

- 80 W/in$^3$, 98% efficient
- 500 total entries
  - July 23, 2015, 120 submitted final report
  - 18 finalists selected to October 21 NREL testing
Shrinking the Hardware

- 98.0mm
- 58.3mm
- 10.3mm

- EMI filter
- Unfolder
- Soft start circuitry
- GaN transistors
- Flying capacitors
- Inductor
Experimental Results

0.3% THD

Measured EMI (dBuV)

Frequency (Hz)

Efficiency (%) vs Output power (kW)

Buffer Efficiency
Inverter Efficiency
Overall Efficiency
Overall Efficiency including control and fans
NREL Testing Details

[Diagram of a power system with labels such as INVERTER, LOAD BANK, Chassis Ground, and voltage levels.]
Research Impact

- Demonstrated the feasibility of multi-level flying capacitor power converters at kW-scale
- Achieved significant performance improvements compared to state-of-the-art
  - Integration
  - Digital control
  - Device utilization
    - GaN transistors
    - Multi-layer ceramic capacitors

Laid the foundation for several promising future research areas
New Applications

- **Electric vehicles**
  - Bidirectional chargers (6.6 kW)
  - On-board dc-dc (50 kW)
  - Superchargers (150 kW)

- **Consumer electronics**
  - Ultra high efficiency power supplies for datacenters
  - LED lighting
  - Chargers

- **Renewable integration**
  - Grid-scale storage
Specific Example: AC-DC PFC

- Power factor correction (PFC) front-end
  - Datacenter applications (server)
  - EV charging
  - Any high power, single-phase grid connected device

Liu et al., Design of GaN-based mhz totem-pole PFC rectifier, JESTPE 2016
Raggl et al., Comprehensive design and optimization of a high-power-density single-phase boost pfc," TIE 2009.
Biela et al., Optimal design of a 5kw/dm3 98.3% rectifier," ECCE ASIA 2010
Lange et al., Three-level single-phase bridgeless pfc rectifiers," TPELS 2015
DC-AC Power Conversion for Electric Transportation
Aviation is the Last Horizon of Hybridization

Obstacles for Electrifying Aircraft

- Electric and turbo-electric aircraft propulsion requires both very high efficiency and low weight

NASA Roadmap for MEA for 2025 [2]:
- Reduce landing/takeoff NOx emissions by 80%
- Reduce cruise NOx emissions by 80%
- Reduce fuel consumption by 60%
- Develop X-Plane concept aircraft

High Specific Power, Low Inductance Motor

Inverter Requirements:

- Maintain high efficiency & specific power for high fundamental frequency (3 kHz)
- Provide sinusoidal voltage with low distortion since machine is ultra-low inductance (minimal iron)

Conventional Solution

Achieving extreme power density through removal of all iron
-> very low inductance machine
Our approach, 9-level FCML converter

- Each module contains two interleaved inverters.
Modular FCML-based Inverter

- Modular Inverter Configuration

\[ V_{bus} = 1kV \]

3-Phase Motor

\[ I = 92 \text{ A} \]

\[ V_{coher} = 360V \]

Double Interleaved Module

200kW inverter
In: 1000V dc
Out: 345V\textsubscript{rms}, 1.2kW, 750 Hz
98.5% at 120kHz switching frequency
Efficiency – Single FCML Leg

Target: efficiency ≥99.0% at 4.2kW (12 modules @16.7kW)

or at 5.6kW (9 modules @22.2kW)

Performance Evaluation

HiQ Solar, NREL Best Venture Award 2014

Wolfspeed/U. Ark/Toyota, R&D100 2014

NASA minimum goal

NASA target

UIUC 2017

Efficiency (%) vs. Specific Power (kW/kg)
Heatsink Optimization

- Work in collaboration with Ken Goodson at Stanford
Interdisciplinary Research Challenges

5-year, $4M/year NSF-funded Engineering Research Center, with Illinois, University of Arkansas, Stanford, and Howard University
Interdisciplinary Research Examples

Andrew Alleyne

Robert Pilawa

Debbie Senesky

Kenneth Goodson

Simón Ang

Nenad Miljkovic
Conclusions

- Control
- Integration/Packaging
- Circuit topologies
- Active devices
- Passive devices

Diagram showing various components and graphs related to power electronics and energy efficiency.
Acknowledgments