RF ESD Protection Strategies – The Design and Performance Trade-off Challenges


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Outline of Presentation

• Introduction
• Key performance parameters
• Diode protection with Power Clamp
• Inductor protection with Power Clamp
• Full circuit – ESD co-design
• Partial circuit – ESD co-design
• Conclusions
Introduction: RF circuit design

Integrated RF front-ends @ 5.5 GHz
- 90nm CMOS technology
- BiCMOS technology

Typical design for performance:
- Large gain
- Low noise
- Linearity

➤ But ESD protection is often overlooked
Introduction: RF circuit design

Common issues of ESD protection:
• Extra input capacitance
• Gain reduction
• Noise increase
• ...

➢ Comparison of advantages and disadvantages of several ESD protection strategies
Introduction: ESD protection

- Diode protection with power clamp
- Inductor protection with power clamp
- Distributed protection
- Resonant and cancellation
- Co-design
### Key performance parameters

<table>
<thead>
<tr>
<th>Performance figure</th>
<th>Target Value (@ $f_C$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_C$</td>
<td>5.5 GHz</td>
</tr>
<tr>
<td>S11</td>
<td>&lt;-10 dB</td>
</tr>
<tr>
<td>S22</td>
<td>&lt;-10 dB</td>
</tr>
<tr>
<td>S21</td>
<td>&gt;15 dB</td>
</tr>
<tr>
<td>S12</td>
<td>&lt;-30 dB</td>
</tr>
<tr>
<td>NF</td>
<td>&lt; 3 dB</td>
</tr>
<tr>
<td>IIP3</td>
<td>As high as possible</td>
</tr>
<tr>
<td>Ptot</td>
<td>As low as possible</td>
</tr>
<tr>
<td>Area</td>
<td>As small as possible</td>
</tr>
<tr>
<td>ESD protection level</td>
<td>&gt; 2 kV HBM</td>
</tr>
</tbody>
</table>
Key performance parameters

- **Low-power RF Figure-Of-Merit**

\[
FOM_1[mW^{-1}] = \frac{Gain[abs]}{(NF[abs] - 1).P_{DC}[mW]}
\]

- **Brederlow’s RF Figure-Of-Merit**

\[
FOM_2[GHz] = \frac{Gain[abs].IIP3[mW].f_c[GHz]}{(NF[abs] - 1).P_{DC}[mW]}
\]
Diode protection with Power Clamp

BiCMOS LNA

- $F_c = 5.5$ GHz
- $P_n$ and $N_p$ diodes of $71 \mu m^2$ (~100fF)
- $S21$ reduction
- $NF: +0.4$ dB
- $FOM_2$ increase
- $50V \rightarrow 3kV$ HBM
Diode protection with Power Clamp

90nm CMOS LNA
- $F_c = 5$ GHz
- $P_n$ and $N_p$ diodes of $65\mu m^2$ ($\sim 100fF$)
- $S_{21}$ reduction
- $NF$: +0.6 dB
- $FOM_2$ increase
- $<50V \rightarrow 500V$ HBM
- Insufficient: Why?
Diode protection with Power Clamp

Insufficient protection

- ESD current path B
- Parasitic current path A
Diode protection with Power Clamp

Insufficient protection:
• BiCMOS LNA: parasitic ESD current flows through $L_G$, emitter diode and $L_S$ to ground
• 90nm CMOS LNA: parasitic ESD current loads gate capacitor and builds up over-voltage

Solutions:
• On-chip capacitor
• Series resistor
Inductor protection with Power Clamp

\[ I_{\text{BIAS}} \]
\[ M_1 \]
\[ R \]
\[ L_g \]
\[ C_c \]
\[ D_3 \]
\[ D_4 \]
\[ D_5 \]
\[ M_1' \]
\[ I_{\text{BIAS}} \]
\[ M_2 \]
\[ C_1 \]
\[ V_{\text{DD}} \]
\[ C_{\text{DEC}} \]
\[ L_{\text{load}} \]
\[ C_{\text{DEC}} \]
\[ C_{\text{pad}} \]

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Inductor protection with Power Clamp

Addition of inductor as “plug-n-play”
  - Diverts ESD current to ground
  - Is transparent for the RF signal

Inductor selection:
  - S11 input matching
  - **Over-voltage** at the gate during ESD
  - Parasitic **resistance** of the inductor during ESD and in RF operation
Inductor protection with Power Clamp

![Graph showing S11 (dB) vs Frequency (GHz) for different inductor values: no inductor, 1nH inductor, 2nH inductor, 3nH inductor, 5nH inductor. The graph illustrates the impact of adding inductors on the S11 parameter across a frequency range of 2 GHz to 10 GHz.]
Inductor protection with Power Clamp

Vgate (V) vs. Time (s)

- 5nH inductor
- 3nH inductor
- 2nH inductor
- 1nH inductor
Inductor protection with Power Clamp
Inductor protection with Power Clamp

- Measurement results

[Graph showing Gain (S21), Input reflection (S11) vs Frequency [GHz] for ESD protected LNA and Reference LNA, and Noise figure 50 Ω vs Frequency [GHz] for ESD protected LNA and Reference LNA]
Inductor protection with Power Clamp

Gate over-voltage protection

• Add a minimum size reverse diode at the gate to block negative over-voltage

• Add two minimum size forward diodes at the gate, biased at 0.6V to block positive over-voltage

These diodes are placed right in front of the gate
Inductor protection with Power Clamp

Schematic with additional diodes to clamp the voltage at M1
### Inductor protection with Power Clamp

<table>
<thead>
<tr>
<th>Circuit</th>
<th>LNA</th>
<th>ESD-LNA</th>
<th>ESD-LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>no ESD</td>
<td>w/o diodes</td>
<td>with diodes</td>
</tr>
<tr>
<td>Vdd [Volt]</td>
<td>1.2</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>Current [mA]</td>
<td>7.5</td>
<td>7.5</td>
<td>7.5</td>
</tr>
<tr>
<td>Gain [dB]</td>
<td>13.5</td>
<td>12.6</td>
<td>12</td>
</tr>
<tr>
<td>S11 [dB]</td>
<td>-21</td>
<td>-18</td>
<td>-24</td>
</tr>
<tr>
<td>S22 [dB]</td>
<td>-11</td>
<td>-14</td>
<td>-14</td>
</tr>
<tr>
<td>S12 [dB]</td>
<td>-31</td>
<td>-32</td>
<td>-32</td>
</tr>
<tr>
<td>NF [dB]</td>
<td>2.2</td>
<td>3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>1dB CP [dBm]</td>
<td>-11.5</td>
<td>-10.5</td>
<td>-9.6</td>
</tr>
<tr>
<td>IIP3 [dBm]</td>
<td>-1</td>
<td>-0.5</td>
<td>0.4</td>
</tr>
<tr>
<td>TLP [A]</td>
<td>-</td>
<td>2.2</td>
<td>4</td>
</tr>
<tr>
<td>HBM [kV]</td>
<td>0.009</td>
<td>2.5</td>
<td>5.5</td>
</tr>
<tr>
<td>MM [V]</td>
<td>-</td>
<td>225</td>
<td>350</td>
</tr>
</tbody>
</table>
Inductor protection with Power Clamp

- Measurement results
Full circuit – ESD co-design

• ESD protection is integrated into the matching circuit
• Typical matching circuit is extended to include ESD protection
Full circuit – ESD co-design

Schematic including the ESD protection into the matching circuit
# Full circuit – ESD co-design

<table>
<thead>
<tr>
<th>Circuit</th>
<th>LNA no ESD</th>
<th>ESD-LNA Co-design</th>
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<tbody>
<tr>
<td>Vdd [Volt]</td>
<td>1.2</td>
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<tr>
<td>S11 [dB]</td>
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<td>-11.5</td>
</tr>
<tr>
<td>S22 [dB]</td>
<td>-11</td>
<td>-8</td>
</tr>
<tr>
<td>S12 [dB]</td>
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<td>1.9</td>
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Full circuit – ESD co-design

- Measurement results

![Graphs showing Gain (S21) and Noise figure with ESD protected LNA and Reference LNA comparison.](image-url)
Partial circuit – ESD co-design

• Determine **parasitic loading** due to the ESD protection and other parasitics
• Take this value into account for input/output **matching**

Opposite to previous methods
• Determine ESD robustness
• Optimize LNA for this robustness
Partial circuit – ESD co-design

bonding wire
bondpad

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Partial circuit – ESD co-design

- Measurement results for an ultra wideband LNA in 0.35μm BiCMOS technology
Conclusions

• Comparison of 4 RF ESD protection strategies with respect to their respective performance trade-offs
• Discussion of the limiting factors and proposal of solutions for further improvement
• Review of the performance parameters for 90nm CMOS LNA’s at 5 GHz
# Conclusions

<table>
<thead>
<tr>
<th>Circuit</th>
<th>LNA</th>
<th>LNA diodes</th>
<th>ESD-LNA inductor w/o diodes</th>
<th>ESD-LNA inductor with diodes</th>
<th>ESD-LNA co-design</th>
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