High-Precision Low-Voltage Low-Power Analog-to-Digital Conversion

Hyunsik Park
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Center for Integrated Systems
Stanford University
Outline

• Introduction
• Proposed ADC architecture
• Implementation
• Experimental results
• Conclusion
Toward Lower Supply Voltage

2007 ITRS Report

- Reduced voltage headroom: limited circuit topologies
- Reduced dynamic range: higher power for the same DR
Reduced Device Intrinsic Gain

- Difficult to build precision analog blocks
- System robustness becomes important
Research Objectives

• **Goal:** Explore novel architectures and circuits for realizing high-precision, low-voltage, low-power CMOS ADCs

• **Target application:** Portable digital audio devices, sensor, instrumentation

• **Target performance**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>0.7 V</td>
</tr>
<tr>
<td>Technology</td>
<td>CMOS 0.18-μm</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>&gt; 95 dB</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>25 kHz</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Minimize</td>
</tr>
</tbody>
</table>
Analog-to-Digital Conversion

- Sampling in time
- Quantization in amplitude
Nyquist-Rate ADC vs. Oversampling ADC

Nyquist-rate ($f_S = 2 \cdot f_B$)

$$DR = \frac{3}{2} \cdot (2^N - 1)^2$$

Oversampling ($f_S = 2 \cdot f_B \cdot M$)

$$DR = \frac{3}{2} \cdot (2^N - 1)^2 \cdot M$$

$x(t)$

$y[n] = x[n] + e_q[n]$
\[ Y = z^{-1} \cdot X + (1 - z^{-1}) \cdot E_Q \]

- Filtering and feedback → Noise shaping
\[ Y = z^{-1} \cdot X + (1 - z^{-1})^L \cdot E_Q \]

**DR** \( \sim \frac{3}{2} \cdot \frac{2L+1}{\pi^{2L}} \cdot M^{2L+1} \cdot (2^N-1)^2 \)
Quantization

• Single-bit quantization
  (+) Inherent DAC linearity
  (+) Relaxed comparator design constraints (power, loading, offset, complexity, ...)
  (-) Increased integrator swings

• Multi-bit quantization
  (+) Reduced integrator swings
  (+) Higher performance without order or OSR increase
  (-) Feedback DAC linearity issues
  (-) Higher performance comparator needed
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Conventional $\Sigma\Delta$ Modulator

\[ (1-z^{-1}) \cdot X - (1-z^{-1}) \cdot E_Q \]

\[ z^{-1} \cdot X - z^{-1} \cdot E_Q \]

\[ Y = z^{-1} \cdot X + (1-z^{-1}) \cdot E_Q \]

- Integrator swings depend on input
- Large input $\rightarrow$ nonlinear operation of integrator op amp
Input Feedforward $\Sigma \Delta$ Modulator*

\[
Y = X + (1 - z^{-1}) \cdot E_Q
\]

- Input independent integrator swings
- Analog summation and timing overhead issues

* K. Nam, et al., CICC 2004
Oversampling ADC with Multi-bit Quantization

- Reduced integrator swings
- Higher power dissipation
Multi-bit Quantization: Idling Comparators

- Comparator redundancy

Multi-bit Quantizer Output (4-bit, OSR=100)

Horizontal Lines: Comparator Threshold

- $V_{\text{ref}}$
- $-V_{\text{ref}}$
- $0.0$

Time

Signal Level
Tracking Multi-bit Quantizer*

- Multi-bit quantizer with a few comparators
- Tracking difficulty
- Comparator offset mismatch problem

* L. Dorrer, et al., ISSCC 2005
Low-Voltage Low-Power Architecture

Input Feedforward → Timing Overhead Issues

DAC

+ \frac{a_1 \cdot z^{-1}}{1 - z^{-1}} + \frac{a_2 \cdot z^{-1}}{1 - z^{-1}}

Three Comparators

Decision Logic & Counter

Reference Update

Tracking Multi-bit Quantizer (18 Levels)

→ Tracking Difficulty

→ Comparator Offset Mismatch Issues

Fast

DWA

MUX

Slow

MUX

Y
Tracking Difficulty (1 of 2)

\[ V_{\text{ref}} \cdot 2\pi \cdot f_{\text{BWmax}} < \frac{\Delta}{T_{\text{clk}}} \]

\[ \Delta = \frac{V_{\text{FS}}}{2^N} = \frac{V_{\text{ref}}}{2^{N-1}} \]

\[ \text{OSR} > \pi \cdot 2^{N-1} \]

\[ (\text{OSR} = \frac{1}{2 \cdot f_{\text{BWmax}} \cdot T_{\text{clk}}} ) \]

- OSR and number of bits trade-off
  - 4-bit quantization requires minimum OSR of 26
- Quantization error degrades tracking operation
Tracking Difficulty (2 of 2)

Modulator coefficient vs. peak SNDR

- Integrator gain scaling helps tracking operation
Comparator Offset Mismatch

- Offset mismatch increases harmonics and noise floor
- Degraded tracking operation

Modulator Baseband Output Spectrum*

* | 0.4 • Δ | offset mismatch
Comparator Offset Mismatch: Tracking

\( |V_{os}| = 0 \)

\( |V_{os}| = 0.2 \cdot \Delta \)

\( |V_{os}| = 0.4 \cdot \Delta \)

(-1 dB, 24.5 kHz input sinusoid)

\( a_1: 1^{st} \) integrator gain
\( a_2: 2^{nd} \) integrator gain
\( b_1: 1^{st} \) integrator output feedforward gain
Single Comparator Tracking Multi-bit Quantizer

- Timing overhead worse with input feedforward

3 operations / cycle

Timing Diagram

\[ \Phi_{\text{ref2}} \]
\[ \Phi_{\text{ref1}} \]
\[ \Phi_{\text{ref0}} \]
\[ \Phi_{\text{FB}} \]
\[ \Phi_{\text{FF}} \]
Delayed Input Feedforward

\[(1-z^{-1})^{L+1} \cdot X - (1-z^{-1})^L \cdot E_Q\]

\[Y = \frac{z^{-1} + H(z)}{1 + H(z)} \cdot X + \frac{1}{1 + H(z)} \cdot E_Q\]

if \[\frac{1}{1 + H(z)} = (1-z^{-1})^L\]

\[Y = (1-(1-z^{-1})^{L+1}) \cdot X + (1-z^{-1})^L \cdot E_Q\]
Proposed $\Sigma\Delta$ Modulator Architecture

Delayed Input Feedforward

$\frac{0.9 \cdot z^{-1}}{1 - z^{-1}}$

$\frac{z^{-1}}{1 - z^{-1}}$

Single Comparator

Tracking Multi-bit Quantizer

(18 Levels)

Reference Update

Single Comparator

Decision Logic & Counter

Fast

DWA

Slow

MUX

MUX

Y
Integrator Swing Comparison

First Integrator Max. Input Swing

First Integrator Max. Output Swing

- FF (Feedforward), DFB (Distributed Feedback)
- Multi-bit quantization → input swing reduction
- Input feedforward → output swing reduction

* 24.5 kHz input sinusoid, OSR=100, $V_{ref}=0.7V$
System Robustness: Amplifier Gain Nonlinearity

Proposed (\(V_{o1_{\text{max}}} = 0.082\text{V}\))

- Baseband Error
- Distortion Power (dB)

\[ V_{o1} \approx z^{-1}(1-z^{-1})^2 \cdot X - z^{-1}(1-z^{-1}) \cdot E_Q \]

Conventional (\(V_{o1_{\text{max}}} = 1.34\text{V}\))

- Baseband Error
- Distortion Power (dB)

\[ V_{o1} = (1+z^{-1}) \cdot X - z^{-1}(1-z^{-1}) \cdot E_Q \]

* \(-1\) dB, 8 kHz input sinusoid (\(V_{\text{ref}}=0.7\text{V}\))
Flicker Noise Reduction

- Chopper stabilization
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Modulator Architecture*

* Actual implementation is fully differential
Switch at Low Supply Voltage

- Limited switch input range at low supply voltage

*CMOS 0.18μm, L=0.18μm, W=100μm, V_{ov}=0.2V
Low-Voltage Switch: Local Boosting

- Used to process DC signals

\[ V_{DD} = 0.7V \]
Low-Voltage Switch: Local Bootstrapping*

- Used to process dynamic signals with high-precision

* M. Dessouky, JSSC 2001
Input Sampling Network Design*

-113 dB THD with 18pF input sampling capacitor (C_S) @ 0.7-V supply

* Actual implementation is fully differential
**0 dB, 7.328 kHz Input Sinusoid (V_ref = 0.7V)
First Integrator Op Amp

- DC Gain: 48.8 dB
- Power: 350 µW
- $BW_u$: 18.9 MHz (@ 18pF loading)
- $V_{CM}$: 0V (Input), 0.35V (Output)
Op Amp Power Reduction

\[ V(\ t_{\ \text{settle}}\ ) = V_{\ \text{Final}} \cdot \left(1-e^{-\left(\frac{t_{\ \text{settle}}}{\tau}\right)}\right) \]

Fixed Integrator Gain Error

- Reduced integrator input swing $\rightarrow$ op amp never slews
- Incomplete but linear settling op amp $\rightarrow$ low power
- In implementation, $n \sim 3.8$

<table>
<thead>
<tr>
<th>$n$</th>
<th>Gain Error</th>
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<tbody>
<tr>
<td>1</td>
<td>0.632</td>
</tr>
<tr>
<td>2</td>
<td>0.865</td>
</tr>
<tr>
<td>3</td>
<td>0.950</td>
</tr>
<tr>
<td>4</td>
<td>0.982</td>
</tr>
<tr>
<td>5</td>
<td>0.993</td>
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<tr>
<td>6</td>
<td>0.998</td>
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</table>
Chopper Stabilization Circuit

Switch Symbols

- NMOS switch
- NMOS switch with local gate bootstrapping

Timing Diagram

- $\Phi_1$ (Sampling)
- $\Phi_2$ (Integration)
- $S_A, S_{Ad}$
- $S_B, S_{Bd}$
Analog Summation and Quantizer

Delayed Input Feedforward

Updated $V_{\text{ref}}$

$V_{\text{in}}$ $S_{1d_o}$ $S_{1_o}$

$S_{1d_e}$ $S_{1_e}$

$S_{1d_o}$ $S_{1_o}$

$C_{0\_o}$

$C_{0\_e}$

$V_{\text{int1}}$ $S_{2d}$

$V_{\text{int2}}$ $S_{1d}$

$C_1$

$V_{\text{cm}}$ $S_{2d}$

$S_{1d}$

$C_2$

$S_{1}$

$S_{2d}$

$S_{2}$

$S_{2d}$

$C_{os}$

Preamp Reset

Latch Enable

Timing Diagram

$S_1$, $S_{1d}$

$S_2$, $S_{2d}$

$S_{1\_e}$, $S_{1d\_e}$

$S_{1\_o}$, $S_{1d\_o}$

Latch Enable

$S_1$: Integrator Sampling Phase
$S_2$: Integrator Integration Phase

Output
Comparator Preamps

When cascaded,

- **DC Gain**: 6.8
- **Power**: 149 $\mu$W
- **$3-\sigma V_{os}$**: 19 mV
- **BW$_{open-loop}$ 3dB**: 174 MHz
- **BW$_{closed-loop unity}$**: 140 MHz
- **Phase Margin**: 58 Degree

*$S_1, S_2$: Bootstrapped NMOS Switch*
Comparator Latch*

\[ V_{DD} = 0.7V \]

Average Power: \(~14\ \mu W\)

\[ t_{\text{regen}} \@ \ 5\ \text{mV}_{pp} \ \text{input} \sim 2.1\ \text{nsec} \]

\[ 3-\sigma \ V_{os} \ 23\ \text{mV} \]

*S. Limotyrakis, ISSCC 2004
Outline

• Introduction
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- 1 kHz input sinusoid
Measured SNDR (2 of 2)

- 8 kHz input sinusoid
• $-5$ dB, 1 kHz input sinusoid
• DWA provides required linearity

SFDR=106 dB
• -8 dB, 8 kHz input sinusoid

• Chopper stabilization effectively removes flicker noise
## Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>0.7 V</td>
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<tr>
<td>Sampling Rate</td>
<td>5 MHz</td>
</tr>
<tr>
<td>References</td>
<td>0 V, 0.7 V</td>
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<tr>
<td>Signal Bandwidth</td>
<td>25 kHz</td>
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<tr>
<td>Dynamic Range</td>
<td>100 dB</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>100 dB</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>95 dB</td>
</tr>
<tr>
<td>Power: Analog</td>
<td>680 µW</td>
</tr>
<tr>
<td></td>
<td>190 µW</td>
</tr>
<tr>
<td>Area</td>
<td>2.16 mm²</td>
</tr>
<tr>
<td>(excluding decoupling capacitors, pads &amp; output drivers)</td>
<td></td>
</tr>
<tr>
<td>Technology</td>
<td>0.18-µm CMOS</td>
</tr>
</tbody>
</table>
## Comparison

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>G. Ahn, et al., ISSCC 05</th>
<th>K. Poon, et al., ISSCC 06</th>
<th>M. Kim, et al., VLSI 06</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply (V)</td>
<td>0.7</td>
<td>0.6</td>
<td>0.5</td>
<td>0.9</td>
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<tr>
<td>Signal Bandwidth (kHz)</td>
<td>25</td>
<td>24</td>
<td>25</td>
<td>24</td>
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<tr>
<td>Clock Frequency (MHz)</td>
<td>5</td>
<td>3.072</td>
<td>3.2</td>
<td>6.144</td>
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<tr>
<td>OSR</td>
<td>100</td>
<td>64</td>
<td>64</td>
<td>128</td>
</tr>
<tr>
<td>Total Power (µW)</td>
<td>870</td>
<td>1000</td>
<td>300</td>
<td>1500</td>
</tr>
<tr>
<td></td>
<td>(Analog: 680)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Range (Vpp)</td>
<td>1.4</td>
<td>0.8</td>
<td>1</td>
<td>1.1</td>
</tr>
<tr>
<td>Dynamic Range (dB)</td>
<td>100</td>
<td>78</td>
<td>N/A</td>
<td>92</td>
</tr>
<tr>
<td>Peak SNR (dB)</td>
<td>100</td>
<td>77</td>
<td>76</td>
<td>91</td>
</tr>
<tr>
<td>Peak SNDR (dB)</td>
<td>95</td>
<td>77</td>
<td>74</td>
<td>89</td>
</tr>
<tr>
<td>Active Die Area (mm²)</td>
<td>1.8 x 1.2</td>
<td>1.8 x 1.6</td>
<td>0.6</td>
<td>1.6 x 0.9</td>
</tr>
<tr>
<td>Technology</td>
<td>0.18µm CMOS</td>
<td>0.35µm CMOS Low V&lt;sub&gt;th&lt;/sub&gt;</td>
<td>0.18µm CMOS Triple Well</td>
<td>0.13µm CMOS</td>
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<tr>
<td>Type</td>
<td>Switched Cap</td>
<td>Switched Cap</td>
<td>Continuous</td>
<td>Switched Cap</td>
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<td>Order</td>
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<td>2 - 2</td>
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<tr>
<td>Quantization</td>
<td>Multi-bit (18 levels)</td>
<td>1.5-bit</td>
<td>1-bit</td>
<td>1.5-bit</td>
</tr>
</tbody>
</table>
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Conclusion

• Low-voltage strategies
  - Input feedforward + Multi-bit quantization
  - Locally boosted or bootstrapped switches

• Low-power strategies
  - Tracking multi-bit quantization
  - Delayed input feedforward
  - Incomplete but linear op amp settling

• High-precision strategies
  - Input feedforward
  - Single comparator multi-bit quantization scheme
  - Chopper stabilization

• Analog-to-digital interface design challenges imposed by technology scaling can be overcome by architecture level innovation and circuit level solutions