Challenges in A/D Design and Practical Understanding of A/D Specifications

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Topics:

I. Examples of A/D systems and specifications

II. Quantization and SNR

III. THD and SFDR

IV. ENOB and power estimations

V. Practical limitations

VI. Systems and specifications revisited

VII. Summary

Basic Rule: “Ask questions and challenge opinions!”
I. Examples of A/D systems and specifications

I.1 10-bit A/D specifications:

- Resolution $N = 10$ bit
- Signal-to-noise ratio $\text{SNR} = 60$ dB
- Total harmonic distortion $\text{THD} = -62.5$ dB
- Maximum differential non-linearity $\text{DNL} = +/- 0.5$ LSB
- Maximum integral non-linearity $\text{INL} = +/- 1$ LSB
- Input signal frequency $F_{\text{in}} = 200$ MHz
- Sampling rate $F_s = 50$ MS/s (undersampling)
I.2 8-bit A/D specifications:

- Resolution $N = 8$ bit
- Signal-to-noise ratio $\text{SNR} = 43$ dB
- Spurious free dynamic range $\text{SFDR} = 72$ dB
- Maximum differential non-linearity $\text{DNL} = \pm 0.5$ LSB
- Maximum integral non-linearity $\text{INL} = \pm 1$ LSB
- Input signal frequency $\text{Fin} = 5$ MHz
- Sampling rate $\text{Fs} = 50$ MS/s
I.3 Video decoder system
I.4 Audio system
I.5 Receiver IF/baseband

2 Vpp
1 KΩ
16 MHz
Gain = 0 ... 30 dB

VGA
NF = 6 dB

LPF
pass band = 18 MHz
stop band = 42 MHz
stop band attenuation = -60 dB
gain = 0 dB

A/D
60 MHz

10
II. Quantization and SNR

Noise contributors:
- Quantization
- Circuit noise:  - thermal
  - 1/f
  - pick-up noise (digital/substrate etc.)
- Clock jitter
II.1 Ideal quantization

\[ \epsilon(t) \]

+ 1/2 LSB

-1/2 LSB

P(\epsilon)

1/LSB

-1/2 LSB

+ 1/2 LSB
Ideal Quantization (cont’d)

Quantization error power

\[ P_q = \int_{-\frac{1}{2} \text{LSB}}^{\frac{1}{2} \text{LSB}} P(x) \cdot x^2 dx = \frac{\text{LSB}^2}{12} \]  

(1)

Signal power

\[ P_s = \frac{(2^N - 1)^2}{2} \cdot \text{LSB}^2 \]  

(2)

Signal-to-noise ratio

\[ \text{SNR} = \frac{P_s}{P_q} = 10 \cdot \log_{10} \left( \frac{3}{2} \cdot 2^{2N} \right) = 6.02 \cdot N + 1.76 \ \text{dB} \]  

(3)
II.2 Quantization with DNL

- assume DNL max = +/- 1/2 LSB
Quantization with DNL (cont’d)

Quantization error power

\[
P_q = \int_{-1LSB}^{1LSB} P(x) \cdot x^2 \, dx = \frac{LSB^2}{6} \tag{4}
\]

Signal-to-noise ratio

\[
SNR = \frac{P_s}{P_q} = 10 \cdot \log_{10} \left( \frac{3}{4} \cdot 2^{2N} \right) = 6.02 \cdot N - 1.25 \text{ dB} \tag{5}
\]

SNR with thermal noise

\[
SNR = \frac{P_s}{P_q + P_n} \tag{6}
\]

if

\[
P_n \approx P_q \tag{7}
\]

\[
SNR = \frac{P_s}{P_q} = 10 \cdot \log_{10} \left( \frac{3}{8} \cdot 2^{2N} \right) = 6.02 \cdot N - 4.27 \text{ dB} \tag{8}
\]
III. THD and SFDR

Ideal quantization power

\[ P_q = \frac{LSB^2}{12} \]

(9)

- energy distributed at signal harmonics (aliased back in 0 to Fs/2 interval)
- maximum number of harmonics \( \sim \pi \cdot 2^N \)
  (derived from max. amplitude and max. slew rate)

Min. power per harmonic

\[ Ph = \frac{P_q}{\pi \cdot 2^N} = \frac{LSB^2}{12 \cdot \pi \cdot 2^N} \]

(10)

Ideal SFDR

\[ SFDR = \frac{P_s}{Ph} = 10 \cdot \log_{10} \left( \frac{12 \cdot \pi}{8} \cdot 2^{3N} \right) = 9.03 \cdot N + 6 \text{ dB} \]

(11)

Realistic SFDR from ideal quantization only

\[ SFDR = 9.03 \cdot N \text{ dB} \]

(12)
IV. ENOB and power estimation

• signal to noise plus distortion ratio

\[ SNDR = \frac{P_s}{P_q + P_n + P_{thd}} \]  

where \( P_{thd} \) is the power in the first several harmonics

• the effective number of bits is based on ideal quantization SNR

\[ ENOB = \frac{SNDR(dB) - 1.76}{6.02} \]  

(14)

• practical ENOB with \( P_n \approx P_q \)

\[ ENOB = N - 1 \]  

(15)

• energy per effective conversion

\[ E = \frac{P_d}{F_s \cdot 2^{ENOB}} \]  

(16)

where \( P_d \) - power dissipation (W)

\( F_s \) - sampling rate (Hz)

state of the art designs \( E = 1-1.5 \) pJ / effective conversion (scaled pipelines)
ENOB and power estimation (cont’d)

- power dissipation depends strongly on the thermal noise

- power dissipation depends weakly on the quantization noise

- power efficiency if $P_n \gg P_q$ (noise limited by thermal, rather than quantization) implies

\[
ENOB < N - 1
\]  

(17)
V. Practical limitations

V.1 SNR limitations

- thermal noise (limited by power dissipation and silicon area)

- clock jitter determines an equivalent signal noise
  \[
  P_j = (2^{N-1} \cdot 2 \cdot \pi \cdot f_{in})^2 \cdot \Delta t_{jitter}^2
  \]  
  (18)

  that limits the achievable SNR to
  \[
  SNR = \frac{1}{\pi \cdot f_{in} \cdot \Delta t_{jitter}}
  \]  
  (19)

  example: 1 ps rms jitter limits a 50 MHz input signal to 76 dB or 12.3 ENOB

- quantization noise
- calibration quantization and calibration noise
- pick-up/substrate noise
V.2 THD limitations

- input pad non-linear capacitance
  \[ THD = fin \cdot R \cdot \Delta C \]  

- example: \( R = 50 \, \Omega \), \( \Delta C = 1 \, \text{pF} \), \( fin = 20 \, \text{MHz} \), THD = 0.1 % or -60 dB (single ended)

- solutions:
  - fully differential implementations (even order harmonic cancellation);
  - bootstrapping of input node (reduce \( \Delta C \));
  - reduce signal source impedance (R);
  - use a transimpedance amplifier (the input pad is a virtual ground node);
  - calibration and correction of non-linearity;
THD limitations (cont’d)

- sample and hold switch non-linearity
  \[ THD = fin \cdot \Delta R \cdot C \]  

  \[ \text{Vin} \] \[ \Delta R \] \[ C \] \[ R = f(\text{Vin}) \]

- solutions:
  - fully differential implementations (even order harmonic cancellation);
  - bootstrapping of sampling switch (reduce \( \Delta R \) - limited by size and back bias);
  - reduce loading (\( C \) - limited by thermal noise);
  - use a closed loop S/H implementations (slow and high power dissipation);
  - calibration and correction of non-linearity;
THD limitations (cont’d)

• signal dependent residual charge injection

\[ \Delta R = f(V_{in}) \]

\[ R = f(V_{in}) \]

\[ \Delta Q = f(R) \]

• opamp finite loop gain and non-linear transfer function

• stage finite settling

• calibration noise and calibration quantization
VI. Systems and specifications revisited

VI.1 10-bit A/D specifications:

- Resolution N = 10 bit
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- Maximum differential non-linearity $\text{DNL} = +/- 0.5 \text{ LSB}$
- Maximum integral non-linearity $\text{INL} = +/- 1 \text{ LSB}$
- Input signal frequency $\text{Fin} = 200 \text{ MHz}$
- Sampling rate $\text{Fs} = 50 \text{ MS/s} \text{ (undersampling)}$

issues:
- SNR implies $\text{ENOB} = 9.67$
- no margin for thermal noise
- margin for jitter -74.6 dB
- clock jitter $< 0.3 \text{ ps rms}$
I.2 8-bit A/D specifications:

- Resolution N = 8 bit
- Signal-to-noise ratio SNR = 43 dB
- Spurious free dynamic range SFDR = 72 dB
- Maximum differential non-linearity DNL = +/- 0.5 LSB
- Maximum integral non-linearity INL = +/- 1 LSB
- Input signal frequency Fin = 5 MHz
- Sampling rate Fs = 50 MS/s

issues:
- SFDR ~ 9*N dB is limited by ideal quantization
I.3 Video decoder system

input noise:

\[ V_n = \sqrt{4 \cdot k \cdot T \cdot B \cdot R} = 2.7 \ \mu V_{rms} \]  \hspace{1cm} (22)

max. SNR

\[ SNR = \frac{V_{in rms}}{V_n} = 102.4 \ dB \]  \hspace{1cm} (23)
I.4 Audio system

input noise:
\[ V_n = \sqrt{4 \cdot k \cdot T \cdot B \cdot R} = 1.6 \, \mu V_{rms} \] (24)

max. SNR
\[ SNR = \frac{V_{in\,rms}}{V_n} = 116.4 \, dB \] (25)

max. ENOB
\[ ENOB = \frac{SNR - 1.76}{6.02} = 19 \, bit \] (26)
I.5 Receiver IF/baseband

• issues:
  - LPF needs a 7th order Chebyshev or 5th order elliptic;
  - LPF needs tuning within +/- 2%;
Receiver IF/baseband (cont’d)

alternative implementation

LPF: - untuned 3-pole;

Gain = 0 ... 30 dB

pass band = 18 MHz
stop band = 222 MHz
stop band attenuation = -54 dB
gain = 0 dB

2 Vpp
1 KΩ
16 MHz

NF = 6 dB

240 MHz

A/D
VII. Summary

- Fundamental limitations based on ideal quantization can not be violated
- Real limitations are seriously degrading the A/D performance
- There are many limitations outside the A/D design (clock jitter, pad protection non-linearity)
- Best power efficiency is for ENOB < N-1
- Reduce quantization noise (It’s always easier to implement a N+1 bit converter rather than an N-bit converter for same performance)
- Use a system approach and challenge system assumptions for best use of the ADC