CPMT Society Officers
Results of Election

Marsha S. Tickman, Executive Director – CPMT Society

Every two years, Voting Members of the CPMT Society Board of Governors elect a President and five Vice Presidents to serve for a two-year term. A President may serve a maximum of two consecutive two-year terms. There is no limit on consecutive terms for Vice Presidents. The following individuals have been elected to serve for a two-year term as Officers of the CPMT Society starting January 1st, 2006 thru December 31st, 2007:

President:	William T. Chen
Vice President Technical:	N. Rao Bonda
Vice President Publications:	Paul Wesling
Vice President Conferences:	Rolf Aschenbrenner
Vice President Education:	Albert F. Puttlitz
Vice President Finance:	Thomas G. Reynolds III

We congratulate all officers on their election to serve CPMT Society for two years and thank them for their interest and willingness to serve. Please review the new Officers' accomplishments, contributions, and interests in the biographical sketches below, and contact them individually regarding issues and directions you'd like to help us pursue in the CPMT Society.

WILLIAM T. CHEN (M '92, SM '03) received his engineering education at University of London (B.Sc), Brown University (M.Sc) and Cornell University (PhD). He joined IBM Development Laboratory at Endicott New York in 1963. His early assignments were in physical modeling and reliability simulation of electronic components in IBM systems and led the implementation of finite element modeling for microelectronic packaging components in IBM. From the late 70's he worked in a broad range of IBM microelectronic packaging products development ranging from design, materials, manufacturing processes and reliability. In IBM he was a strong proponent in developing university education and research in microelectronic packaging related disciplines. He was elected to the IBM Academy of Technology for his contributions. He retired from IBM in 1997 and joined the Institute of Materials Research and Engineering (IMRE) in Singapore, where he became Principal Research Fellow, and Director of the Institute, contributing to the growth in facilities, resources and facilities of IMRE as a full fledged materials research center for the region. He joined ASE in 2001 where he has the position of Senior Technical Advisor.

He has been a Member-at-Large of the CPMT BoG, and is an active member of the CPMT Santa Clara Valley Chapter. He has served as CPMT Strategic Director for Region 10, supporting the CPMT activities in the Asia Pacific region. He is the Co-Chair of the ITRS Assembly and Packaging Roadmap International Technical Working Group. He had been active in the Electronics Packaging Division of ASME. He is a Fellow of ASME. He has published extensively in the fields of microelectronics packaging and solid mechanics. He has served as an Associate Editor of *ASME Journal of Electronic Packaging*, and IEEE/CPMT Transactions.

In the past years the Society has made giant strides towards achieving the goal of a global professional society. We have CPMT chapters and individual memberships situated in far flung cities and regions around the world. An important step in our globalization focus would be to increase the communication channels between BoG and chapters, and between chapters and chapters. In this way new ideas and new ways to serve the memberships will bubble up. Opportunities for professional programs, and networking between individual professionals in different regions and among diverse disciplines will expand and multiply. The global CPMT Society will continue to grow as the professionals in our industry, wherever they may be, see and appreciate the value proposition in belonging to CPMT.

N. RAO BONDA (M'97, SM'02) is currently a member of research and development staff in Freescale Semiconductor, Inc. (formerly known as Motorola's Semiconductor Products Sector) in Tempe, AZ. He received a Ph.D. in Materials Science and Engineering from the University of Pennsylvania, Philadelphia, PA, in 1985. He has been serving the IEEE CPMT Society since 1997 as the Chair of the Awards Committee.

After receiving Ph.D., Rao continued research in materials science at the Ohio State University, Columbus, OH and the University of Wisconsin, Madison, WI until 1989. From 1989 to 1994, he was a research member at IBM T.J. Watson Research Center, Yorktown Heights, NY, and IBM Microelectronics Division, Endicott, NY. In IBM, he developed electronic packages and processes involving C4 and wire bond chip joining methods, and worked on qualification of several ceramic and plastic packages. His other research work in IBM included failure mechanism studies of Pb/Sn solder alloys to improve the thermal fatigue and reliability of solder joints in electronic packages.

In 1994, Rao joined Motorola's Semiconductor Products Sector in Tempe, AZ, as a team leader for packaging of an optical display module. He developed a fine pitch flip chip bonding process for this display module and improved its yield and reliability through innovative designs. After completion of the display module project, he led new package introductions from design to manufacture implementation and qualified plastic packages for wireless communication and networking systems applications. He currently provides packaging development and technical support for a major wireless communications customer and works with package assembly subcontractors to fulfill the customer's product requirements and packaging roadmaps. He has over 20 technical publications and a US patent.

Rao has been the Chair of the CPMT Awards Committee for the last nine years, and has coordinated the selection process for the awards. Working with the Awards Committee and the Board of Governors, he has facilitated several strategic decisions to align the awards process with the CPMT Society goals. He is the CPMT Chair for the Motorola Graduate Fellowship for Research on Electronic Packaging and is a member of the TC16 committee on RF and Wireless. He has also served on the selection committee for the CPMT Chapter of the Year

award. He is very active in CPMT Phoenix Chapter and IEEE Phoenix Section. He has served as the chair and program chair for the Chapter and as the treasurer for the IEEE Phoenix Section. He is currently the secretary for the Phoenix Section.

Rao has been actively participating in the Electronic Components and Technology Conference (ECTC) for several years. He has served as the chairman of the Components and RF subcommittee and has chaired the sessions at the ECTC. He has chaired the ECTC's Professional Development Courses committee and served on the committee for three years. He was the Web Administrator for the ECTC last year and is currently the assistant program chair.

Rao is a member of the IEEE and the American Society for Materials International (ASM). In addition to a Ph.D., he holds an MS and a BS in Metallurgical Engineering from Indian Institute of Technology, Kanpur, and Regional Engineering College, Warangal (India), respectively. He also received an MBA from the Arizona State University, Tempe, AZ, in 1998.

Action plans as the Technical VP of CPMT Society: Promote the technical interests of our members through Technical Committees (TCs) and policy enhancements in the BoG. Increase the participation and collaboration of TCs in conferences, both in US and abroad. Look for new and emerging technologies and form TCs in those areas. Enhance communication among the TCs to share their activities and opportunities for growth.

PAUL WESLING (M '70, SM '84, F '04) received his BS in

electrical engineering and his MS in materials science from Stanford University. Following assignments at GTE/Lenkurt Electric (component engineering), ISS/Sperry Univac (bubble memory development, reliability, manufacturing engineering), Datapoint Peripheral Products (VP - Product Integrity), and Amdahl (design analysis, mainframe testing, console peripherals), he joined Hewlett Packard (Tandem NonStop Division) in 1985. As a member of the development team for advanced IC packaging, he designed several multi-chip module prototypes, supervised their fabrication, and tested them. In the Education Group he developed courses on reliability, managed the Distinguished Lectures series, and was on the Technology Initiative team. Retired in 2002, he now serves as editor and webmaster for the IEEE S.F. Bay Area Council. He organizes a number of advanced technology and professional skills development courses for engineers and developers in the Santa Clara Valley.

Mr. Wesling has published a number of technical papers and authored a book chapter. As CPMT's current Vice President-Publications, he supervises four archival journals, a newsletter, and the website, oversees authors for IEEE Press books, manages the Special Sections for the Society Transactions, and organizes the electronic publishing initiatives for the Society.

He is a Fellow of IEEE, and received the IEEE Centennial Medal, the CPMT Board's Distinguished Service Award, the Society Contribution Award, and is a CPMT Distinguished Lecturer. He has organized over 240 short courses for the Santa Clara Valley CPMT Chapter, many of them held at Stanford University. As part of his interests in education, he serves as Vice-Chair of TC-Education, is on the ECTC's Packaging Education program committee, administered the joint CPMT/NSF grant program for packaging education, and is on the SCV Section K-12 Education Committee.

He also served 15 years as scoutmaster of a local Boy Scout Troop and is now advisor for a Venturing Crew, webmaster for CPMT and for the Pacific Division of the ARRL, and enjoys backpacking, fly fishing, and amateur radio.

ROLF ASCHENBRENNER (M'97, SM '04) was born in

Buchen, Germany, in 1961. He received the M.S. degree in mechanical engineering from the University for Applied Science, Gießen, Germany, in 1986 and the B.S. degree in physics from the University of Gießen, Germany, in 1991.

From 1991 to 1992 he worked at the University of Gießen in the area of new materials and was engaged in a project for the German Space Lab Mission D2. In 1993 he joined the research center Technologien der Mikroperipherik at the Technical University of Berlin, working in the area of electroless metal deposition. Since March 1994 he has been employed at the Fraunhofer Institute Reliability and Microintegration Berlin (IZM) where he is presently head of the department of Chip Interconnection Technologies. In 2000, he became the Deputy Director of the Fraunhofer Institute IZM.

Rolf Aschenbrenner's research work has spanned from manufacturing process fundamentals in adhesive joining to applied manufacturing problems. Broadening his research contributions beyond those are made in thin and flexible electronic assemblies and development and analysis of innovative process technologies for all aspects of system level packaging.

He has authored and co-authored more than 80 articles in journals or proceedings in the area of electronic packaging and he holds five patents and has eight pending patents in the field of microelectronic packaging. In 1995 he obtained the best paper award from the Surface Mount International Conference (SMI) in San Jose.

In terms of professional services, Rolf Aschenbrenner has taken roles as a member of the Board of Governors for the IEEE CPMT Society. He was General Chair of the first International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics. He was a Program Chair of the IEEE System Packaging Workshop in 2001 and of the European VLSI Packaging Workshop in 2000. He also serves as a member on several technical committees including ISEPT 98, Materials 99, 00 and 01, Adhesives in Electronics 98 and 00, EMAP 2000, EPTC 2000, Interpack 2001 and Electronic Goes Green 2000.

As a member of the IEEE CPMT Society Board of Governors, Rolf has worked as a European representative on the Conference Advisory Committee, and has played an active role in the globalization of IEEE CPMT in terms of Membership and Chapter development. He previously served as Strategic Pro-

gram Director, European Activities, and currently serves as Vice President, Technical.

ALBERT F. PUTTLITZ (M '88, SM '92) received his Ph.D. degree in Engineering Mechanics from Michigan Technological University in 1968. During 36 years with IBMCorp., he has held group leader/engineering assignments in semiconductor process development, reliability, testing, contamination analysis, manufacturing engineering, failure analysis, tooling, mechanical analysis/design and education. He is the recipient of IBM's first level Invention Achievement Award and has been an Invention-Disclosure-Review Board member. He has taught college-level engineering courses at Michigan Tech. and IBM. Dr. Puttlitz retired from IBM in 1992 and now consults. He is also active as a licensed Realtor in the State of Vermont.

Albert has numerous external and internal IBM publications. He is the presenter and/or co-author of papers at four ECTC Components sessions (1985, '86, '89, '92). He received the best CPMT Transactions Paper Award in 1985 (with Sang Kim). He is a 18-year member of the IEEE CPMT Society, served on the ECTC Components and RF Paper Review Committee for the past fifteen years, was the ECTC Components and RF Subcommittee Program Chairman during 1991-1993, and has served as the ECTC Components and RF session Chairman or Co-chairman for nine years. He was the ECTC Professional Development (Short) Course Chairman for eight years, rotates as its chair every three years with other members of the Professional Development Course committee and is a member of the ECTC Professional Development Course Committee for the Y2006 ECTC. Albert introduced "Continuing Education Units" credits for Professional Development Courses (sponsored by the IEEE Education Department) and responsible for the institution of the CPMT "Professional Development Certificate of Achievement".

Dr. Puttlitz was elected to four terms as a Member-at-Large on the CPMT Board of Governors. He has been the CPMT Vice President of Education for the past eight years and currently holds that position.

His accomplishments as CPMT VP of Education for the past five years include:

- As an initiative to promote the CPMT Society worldwide, he lead a delegation to Hong Kong in Y2000 and was a member of the Y2000 Singapore delegation.
- He was a member of the ECTC Electronic Packaging Paper Review Committee and was Chairman of several of the ECTC Electronic Packaging Sessions for 4 years.
- He was a member of the Electronic-Packaging-Education-Faculty Grant-Committee (with Leyla Conrad, Paul Wesling, and Andrew Tay). Over 12 Grants, sponsored by CPMT and PRC of Georgia Tech., have been awarded for developing multimedia/web-based Electronic Packaging Courses for the 21st Century. The last grants were awarded at the Y2003 ECTC.
- He obtained CPMT approval (and money) and arranged for the production of CPMT sponsored CD-ROM Courses by the IEEE Education Department for Y2000 and Y2001. Due to the high IEEE financial debt load, these productions are now on hold and may be done in a less costly manner.
- He is the Chairman of the CPMT Distinguished Lecturer program. To date, the program has 20 Distinguished Lecturers. The program is in wide use with new members being added yearly.
- He is a member of the CPMT-Motorola Fellowship Committee responsible for awarding a yearly fellowship in Electronic Packaging to a Ph.D student at ECTCs. This fellowship is chaired by Dr. Andrew Skipor of Motorola.

My goal for the next two years as VP of Education is to continue to promote CPMT worldwide as the premier packaging society by continuing to offer educational courses, programs and opportunities for its members. I'm ready to lead a delegation to promote CPMT to almost any part of the world. I will continue to be active in all of my current activities which includes attempting to introduce Engineering education at the high school level. Additionally, I will seek to find a less expensive way to produce and market CPMT sponsored courses via CD-ROMs and multi-media/web. And lastly, I will attempt to get at least one more industrial sponsor for an educational program.

Albert holds the IEEE membership grade of Senior Member, is a member of ASME, is a member of the US Power Squadron, and is active in community and church activities.

THOMAS G. REYNOLDS III (M'92, SM '04) Dr. Reynolds received his PHD from Brown University in 1972 where he worked on synthetic inorganic chemistry of electronic materials. His MS (1966) and BS (1964) were from the University of Virginia in Materials Science and Mechanical Engineering respectively. Tom has worked in the field of electronic ceramic materials and other advanced technologies for more than 35 years.

From 1992 to present, Tom has been the Director of Technology at Murata Electronics N.A., Inc. He has worked in the areas of leading edge designs in decoupling capacitors, hard disk drive activation, LTCC modules, and integrated passive components. He has acted as liaison between American designs and Asian development activities, as well as in merger and acquisition analysis. Prior to joining Murata, Dr. Reynolds worked for Philips Electronics for 18 years in both the US and Europe, developing processes and methods for electronic (dielectric) ceramics, and from 1968 to 1973 he was staff scientist at Texas Instruments.

Tom has been involved with CPMT and ECTC (Electronic Components Technology Conference) for more than 13 years. He was General Chair for ECTC in 2000 and continues to be active as Finance Chairman. He is also a Senior Member of IEEE.

Additional activities and responsibilities include Treasurer of the Ft Walton Sail & Power Squadron of the United States

Power Squadron and he is currently the Vice Commodore of the Ft Walton Yacht Club. Tom is also a member of the Institute for Senior Professionals, an association of business, professional, medical and military professionals to advise and serve the local community based on their experience and expertise.

Dr. Reynolds will bring a breadth of experience, both local and international, to the Board. He will enthusiastically offer his efforts to the CPMT vision of continuing globalization and service to the profession.

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CPMT Society Board of Governors
Results of Election

John Segelken, Nominating Committee Chair

The following individuals (in alphabetical order) have been elected to serve for a three-year term as Members-at-Large to the CPMT Society Board of Governors starting January 1st, 2006 thru December, 31st 2008:

Vasudeva P. Atluri, Li Li, Dongkai Shangguan, Patrick Thompson, Klaus-Jürgen Wolter, Kishio Yokouchi

We thank all candidates for their interest and willingness to serve. Please review the new Board members' interests in the biographical sketches below, and contact them individually regarding issues and directions you'd like to help us pursue in the CPMT Society.

VASUDEVA P. ATLURI (M'91, SM'00) is currently a Silicon Integration Manager in Assembly Technology Development, Intel Corporation, Chandler, AZ. He received a Ph.D. in Materials Science and Engineering from University of Arizona in 1998 with a minor in Electrical Engineering and specialization in silicon fabrication.

Vasudeva joined Intel Corporation in 1995, managing a group responsible for ensuring successful interface between silicon and assembly technology development. Earlier he was employed at Motorola and worked on reliability aspects of plastic packages. He has more than thirty technical publications and has filed for six patents.

He has served as CPMT Phoenix Chapter Chair and IEEE Phoenix Section Chair and currently chairs the Awards Committee for IEEE Phoenix Section and the Workshop Committee for the IEEE CPMT Phoenix Chapter. He is also serving as Student Activities Coordinator for IEEE Region 6 Southwest Area. He is a nomination committee member for selecting candidates for IEEE Region 6 Director-Elect. He is on the ECTC program committee, and is the new Newsletter editor. He would like to take already useful and informative newsletter to a higher level. He is serving as editor for Intel Assembly and Test Technology Journal for last eight years of which last four years as chief editor.

Dr. Atluri was presented multiple awards over last seven years by IEEE CPMT Phoenix Chapter and IEEE Phoenix Section for his multiple outstanding contributions to Electronic Packaging and IEEE including organizational and technical leadership. He received Individual Achievement awards from Southwest Area part of IEEE Region 6 during 2004 and from IEEE Region 6 during 2005.

LI LI (S'93, M'95, SM'03) is currently a Distinguished Member of Technical Staff at Freescale Semiconductor (formerly Motorola Semiconductor Products Sector) in Tempe, Arizona, USA. She has received B.S. and M.S. in Material Science and Engineering and a Ph.D. in Electrical Engineering at SUNY-Binghamton. She has done extensive research and development in the field of electronic packaging and has been supporting the IEEE CPMT Society in various roles.

She has worked in various areas of packaging materials and process development, including flip chip interconnect and chip scale package development, underfill materials, Sn-Pb and Pb-free solder wafer bumping, and adhesive interconnects. She is currently working on RF module development, component design libraries for effective RF module design flows, integrated passives design and simulation on ICs and organic substrate, and flip chip in RF modules.

Li Li has published more than 40 technical papers, co-authored a book chapter in Conductive Adhesives in Electronics Packaging, and received four issued patents with one pending. She is the chair of the Components and RF sub-committee of ECTC and has served as a session chair. She also contributes to CPMT Newsletters. In recognition of her significant contributions to both materials and electrical aspects of electronic packaging and for her service to the CPMT Society, Li Li was awarded the CPMT Society "Outstanding Young Engineer Award" for the year 2002. Li Li would like to work on programs to attract and encourage young engineers to pursue this challenging and multi-disciplinary career in electronic packaging.

DONGKAI SHANGGUAN (M'01, SM'02) received his BS degree in Mechanical Engineering from Tsinghua University, China, Ph.D. degree in Materials from the University of Oxford, U.K., and MBA degree from the San Jose State University. He conducted post-doc teaching and research at the University of Cambridge and then at The University of Alabama. He lectured at Wayne State University as Adjunct Faculty, and is currently a guest professor at Shanghai University.

Dongkai worked for 10 years at Ford/Visteon as Senior Technical Specialist and Supervisor of Advanced Electronics Manufacturing, before he joined Flextronics in 2001 where he is currently Senior Director for Advanced Assembly and Environmental Technologies.

He has published 1 book and over 160 papers, and his latest book "Lead-Free Solder Interconnect Reliability" will be published soon. He has 20 U.S. and international patents issued and a number pending.

Dongkai has received a number of recognitions for his contributions to the industry, including the "Total Excellence in Electronics Manufacturing Award" from SME and the "Soldertec Lead-Free Soldering Award". He has given numerous techni-

cal presentations and keynotes at various conferences, and chaired technical sessions and panels including the Advanced Packaging Materials Symposium, ECTC, and HDP. He has also given several seminars at IEEE CPMT chapter meetings.

Dongkai wants to focus on the area of assembly technology to enhance the cross-integration of the assembly technology roadmaps among several professional organizations, including CPMT, SMTA, iNEMI, IPC, etc, as he believes that the global scope of the CPMT membership will add significant value to the roadmapping process, the Roadmap itself, and the global utilization of the Roadmap.

PATRICK THOMPSON (M'87, SM'92) received his BS, MS and Ph. D. degrees in Chemical Engineering from the University of Missouri-Rolla in 1979, 1981 and 1983, respectively.

Pat has spent more than 20 years in the area of advanced packaging research, development and transfer to manufacturing. He has led development teams at Bell Labs, AMI Semiconductors and Motorola (now Freescale), working on technologies ranging from flip chip fabrication and packaging, flip chip on board to chip scale packages, multi-chip packaging, MEMS and opto-electronic packaging. Since 2001, he has been a Senior Member of the Technical Staff at Texas Instruments, where he leads the development of packaging solutions for high performance microprocessors and the conversion to Pb-free bumps for Texas Instrument's flip chip package portfolio.

Pat is active in industry-consortia and industry-university partnerships. He is currently the chair of the Georgia Institute of Technology Packaging Research Center Industrial Advisory Board and a member of the PRC Executive Advisory Board. He is TI's primary representative to the Sematech 3D IC working group, and is also active in TI's 3D IC program with IMEC. Pat is a TI member of the SRC Packaging/Interconnect TAB, and currently mentors two custom packaging research projects.

Pat has five patents and over two dozen publications. He has presented packaging tutorials and given invited talks at leading packaging conferences. He has been a member of the Electronic Components and Technology Conference (ECTC) technical program committee since 1983, where he has held multiple positions. He is currently the General Chair of the 2006 ECTC. He has served at both the local and Society level of the CPMT holding positions including Member at Large, Administrative Vice President, and Technical Vice President of the CPMT. He served as a member of the *IEEE Spectrum* Editorial Advisory board from 1998-2000. In addition to IEEE, Pat is a member of the American Society for Quality.

KLAUS-JÜRGEN WOLTER (A'05) Prof. Dr.-Ing. habil. Wolter's professional experience includes: 2003 Director of the Electronic Packaging Lab at Dresden University of Technology; 2002 Director of the Centre of Microtechnical Manufacturing; 1989 Assistant professor at the Institute of Electronic Technology; 1989-1973 Research and development in the microelectronic industry.

Klaus-Jürgen Wolter's fields of research include substrate technologies; assembly technologies of devices, components, MEMS; joining technologies; reliability of electronic packages; and nondestructive test methods. He is a member of: IEEE CPMT, IMAPS, SMTA, and VDE. He was Chair of the "International Spring Seminar on Electronic Technology", Chair of the 5th and 8th International Academic Conference on Electronic Packaging Education and Training, and Vice Dean of Education for the Department of EE.

His publications include: co-author of the monograph, Scheel: Electronic Assembly Technology Electrochemical Publications LTD, 2004; Wolter, K.-J.; Wiese, St.: Interdisziplinäre Methoden der Aufbau- und Verbindungstechnik der Elektronik, Gdb goldenbogen, Dresden 2003; co-author of the monograph, Sauer: Prozesstechnologie der Elektronik, Carl Hanser Verlag München Wien 2003, and Wolter, K.-J.; Sauer, W. (Editor): Elektronik-Technologie in Forschung und PraxisVerlag Dr. Markus Detert, Templin, Band 1 – 9.

The research activities result in more than 80 conference presentations/proceedings and in 3 patents. He has been an IEEE CPMT member since 2005. He served as a member of Program Committee on Education of the 53rd, 54th and 55th ECTC.

KISHIO YOKOUCHI (M'02) received his bachelor's and master's degrees in applied chemistry from the Yokohama National University in 1977 and 1979, respectively. In 1979, he joined Fujitsu Laboratories Ltd., where he has been mainly engaged in R&D work on microelectronics materials. During this period, he developed the world's first copper conductor co-fired 60-layer 8 inch ceramic circuit board, Low-k polymer thin film circuit boards for MCMs of mainframe computers, and high-density buildup circuit boards. Also, he has been involved with development of direct immersion cooling technologies for high-speed servers, including liquid helium cooling for Josephson devices and liquid nitrogen cooling for HEMT devices.

From 2000 to 2004, he was the director of the Advanced Optoelectronics Technology Dept. of Fujitsu Laboratories of America Inc., where he directed R&D work on optical integrated devices and optical interconnection technologies. He is currently a senior vice president of the Device & Materials Laboratories of Fujitsu Laboratories in Japan.

Mr. Yokouchi is a member of several scientific societies which include IEEE, IMAPS, OSA, and JIEP. He presently serves as a TC-6 committee member of the CPMT Society. Also, he co-chaired the Plenary Seminar of the 54th ETCT and CPMT Seminar at 55th ECTC. He also contributed as a technical committee member of IEMT/IMC in Japan.

He is the author or co-author of 55 technical presentations and publications, and invented or co-invented 29 U.S. and Japanese patents. He co-authored three technical books entitled "Thin Film Metallization for Aluminum Nitride" published by Trans Tech Publications Inc, "CSP/BGA Technologies" and "CSP Packaging Technologies" published by the Nikkan Kogyo Shimbun.

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Save these pages of "profiles"; introduce yourself at the next conference or workshop!