Conference and Workshop Reports

Future Directions in IC and Package Design Workshop

FDIP' 05, Austin, TX

Workshop co-chairs: Alina Deutsch, IBM and
Madhavan Swaminathan, GIT

This year's workshop was held once again on the Sunday afternoon before the start of the EPEP'05 conference, on October 23, 2005. Attendance was very good again with 70 participants. The workshop was sponsored by the TC-EDMS technical committee on electrical design, modeling, and simulation and co-chaired by Prof. Madhavan Swaminathan from Georgia Institute of Technology and Alina Deutsch from IBM Corporation. Prof. Swaminathan is also the chair of the TE-EDMS that sponsors five workshops across the world.

FDIP'05 was divided into three sessions namely, System Design, Modeling and Measurement Methods for Signal Integrity, and Computational Electromagnetics. The three session chairs were Tawfik Arabi from Intel, Anand Haridass from IBM, and Ramesh Abhari from McGill University. The first session started with the presentation made by Carl Anderson from IBM Austin. The title of his talk was Designing Servers in a Commodity World. The key message he tried to convey was the fact that the high-end servers need to provide the high performance using only commodity technologies due to cost measures. The high-volume market of personal computers that are selling for $1,000 is the fastest growing and driving the introduction of low cost technologies. The only solution then for high-end systems is to use multi-core chips (Carl sees 8+ cores on chip by 2010) with on chip switch, use of multi-threading, standard I/O's such as PCI Express, power efficient designs, systems that scale out into blades, with system level reliability delivery, and software that can take advantage of GRID computing for cost competitive solutions.

The second talk entitled Signal Interconnect and Challenges Inside the CEC was delivered by George Katopis from IBM Poughkeepsie The main message he tried to convey was the need to change the industry's focus from chip design to interconnects as the key system performance detractor. He reported on a very detailed analysis of single- versus differential-ended transmission. The study considered power, data bandwidth, bit data rate, and chip area per bit. George predicted that by 2010, interconnect bandwidth requirement will reach 5-10 GHz with a required spectrum of interest up to 25-50 GHz. At a 95 mm node, the single-ended lines can achieve 0.012 mm^2/line, 1.25-2.5 Gbps/line and 104-208 Gbps/mm^2 for 30 inch lengts. The equivalent differential links, for 6 inch lengths, have 0.25 mm^2/line, 5.4 Gbps/line and 22 Gbps/mm^2. Clearly the differential solution is much more extendable. It has 60-70% bandwidth advantage. This advantage comes at a significant cost in power and chip area. The performance advantage is also degraded by packages with large discontinuities such as long via stubs. DE solution is equivalent to SE where loses are dominant but where noise induced jitter is the main concern, DE is preferred. Another important message to the academia was that for 25-50 GHz spectrum, there is a very strong need for better measurement techniques and modeling tools. Both the tools and the characterization need to address the full complexities of product like structures.

Brian Young from Texas Instruments brought forth a new design methodology in his talk entitled High Volume Signal and Power Integrity Design for ASICs. Brian indicated that the ASIC chips of today have clock frequencies of over 500 MHz, power levels as high as 10W, integrated links up to 6 Gbps. In order to design the packages needed for such high-end chips in very short time (around one month), a pre-characterization procedure was developed with separate signal and power integrity analyses. A large data base is created with >18K results that can be looked-up when the selection needs to be made. Superposition is used to sum worst-case conditions of noise for the power supply and interconnects and multiple evaluations are made to explore the design space for number of layers, I/O's, placement, bypass capacitors, interconnect length, etc.

The fourth presentation made by Mizuki Iwanami from NEC, entitled Electro-magnetic Field Visualization System for IC/Package Design Based on Optical Techniques, showed a very novel probing technique. A magneto-optic/electro-optic (MO/EO) crystal glued at a fiber edge was used for very small LSI circuit probing. An incident light in the MO/EO crystal is reflected by a dielectric mirror on the bottom surface and re-enters the fiber. During one round trip, the light responds to the magnetic/electric field surrounding the DUT and thus near-field distribution can be scanned over the DUT. Examples were shown for the field distribution scanning of 20 μm meander micro-strip lines over the frequency range 10 MHz to 2.46 GHz. Magnetic field was also scanned in LSI package and EMI around the decoupling capacitors was detected. The probe is considered very useful for both signal and power integrity analysis. The probe position height could vary in the range of 3-15 μm above the DUT.

The last two talks covered two approaches in computational electromagnetics. Prof. Raj Mittra from Pennsylvania State University talked about harnessing the power of Parallel Computation on the IBM Blue Gene/L to analyze complex digital and RF systems. Due to the increasing complexity and problem size requirements for electrical modeling, the development of techniques that allow the use of parallel platforms has been gaining momentum. Raj introduced the Parallel Finite Difference Time Domain full-wave solver that takes full advantage of the very efficient processor-to-processor communication of the Blue Gene supercomputer. Efficiency close to 90% was shown on up to 256 processors due to the only near-neighbor interactions needed by PFDTD. Both the CBMOM and PFDTD solvers were used on very large problems with close to 10B unknowns and simulation examples were shown.

The last talk in the workshop was given by Prof. Weng Cho Chew from University of Illinois. Prof. Chew showed examples of 20 million unknowns using integral equation solutions on SP type clusters . The equivalence principal algorithm, EPAL, developed at UIUC allows the mixing of circuits and wave physics as needed by practical packaging structures. While quasi-static solvers can handle billion unknowns, full-wave problems can only reach millions due to the need for far-neighbor interaction capturing. He talked about the recently developed mixed-form fast multi-pole algorithm that can work seamlessly from static to the microwave regime. It is both ac-

curate and error controllable, as well as being memory efficient.

In the case where both wave physics and circuit physics are important, such as a large structure with many small details as found in a computer system, it is more expedient to put Huygens' equivalence boxes around each region with fine details, and decouple the exterior problem from the interior problem. This can be regarded as having replaced a region with fine details with an N-port representation. Inside the Huygens' boxes, low-frequency techniques can be used to solve the problem so that low-frequency physics is correctly captured, with the ensuing geometry details. Outside the Huygens' boxes, when wave-like interactions are computed, less number of unknowns are needed to capture the wave physics, but meanwhile, the ability to model fine details is not foregone.

Low-frequency breakdown is encountered for numerical solvers when structures are smaller < λ. For integral equation solvers, low-frequency breakdown is prevented by using quasi-Helmholtz decomposition, while for fast algorithm, low-frequency multi-level fast multi-pole algorithm LF-MLFMA and low-frequency multi-level inhomogeneous plane wave LF-FIPWA have been developed to overcome this problem. Furthermore, a mixed form fast multi-pole algorithm MF-FMA has been developed to realize the broad frequency range modeling. Solution speed is accelerated and workload and memory requirements are decreased from $O(N^2)$ to $O(N)$. Very large problem sites with < 1 GB memory needed were shown to run on typical personal computer platform with the use of such advanced numerical techniques.

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Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications

Submitted by Vasudeva P. Atluri, Ph.D., Workshop Chair and Charles E. Weitzel, Ph.D., Workshop Co-Chair

The IEEE Phoenix Section's CPMT Chapter with the Waves and Devices Chapter jointly held an all-day Workshop on Thursday, November 10th, 2005, at Arizona State University, Tempe, Arizona. The workshop was very well attended with about 196 registrants. The breakdown of registrants included 27 organizing committee members, 12 speakers, 22 vendor representatives, 72 IEEE members (included 5 student members), and 63 non-members (including 1 student). The workshop agenda included these talks: (PDFs of the slides will soon be available in the CPMT Members-Only web area: www.cpmt.org/mem).

1. "*Keynote Presentation: Moore's Law Redux: Research in the Age of On-Chip, Converged Communication and Computing*", Dr. Krishnamurthy Soumyanath, Intel Corp.
2. "*A 2005 Perspective on MOSFET Scaling Challenges and Technology Innovations Through the End of the Roadmap*",. Peter Zeitzoff, SEMATECH International
3. "*Advanced Devices for Future CMOS Nodes*", Dr. Suresh Venkatesan, Freescale Semiconductor, Inc.
4. "*Challenges for TCAD for Advanced Devices*", Dr. Mark Law, Univ of Florida.
5. "*Opportunities and Challenges of III-Nitride Semiconductors*", Dr. Zlatko Sitar, North Carolina State Univ.
6. "*Wireless Integrated MicroSystems (WIMS): Coming Revolution in the Gathering of Information*", Dr. Kensall Wise, Univ of Michigan
7. "*Flip Chip Packaging Technology for Next Generation Computing Applications*", Raj Master, AMD
8. "*Future Decoupling Technology for High-Speed Integrated Circuits*", Richard Ulrich, Univ of Arkansas
9. "*Electromagnetic and Circuit Co-Simulation – The Key to Next Generation Interconnect Design*", Dr. Zoltan Cendes, Ansoft Corp.
10. "*Hot-Spot Driven Thermal Management for Next Generation Computing and Communication Technology*", Dr. Avram Bar-Cohen, Univ of Maryland
11. "*Pb Free Interconnect: Industry Status & Trends*", Tim Olson, Ahmer Syed, and Jeff Cannis, Amkor Technology
12. "*3D Integration Technologies – Motivation and Status*", Dr. Rajen Chanchani,
13. Panel Discussion "*Future of Computing and Communications.*"

The morning session with a focus on Moore's Law Redux, A 2005 Perspective, Advanced Devices, Challenges, Opportunities and Future was very received by the workshop audience. Dr. Krishnamurthy Soumyanath suggested that the availability of low cost and power efficient MIPS (a direct consequence of Moore's law) makes ubiquitous mobile communications possible. The talk described a "digitally assisted analog" chip design methodology for on-chip, converged, communications and computations. Dr. Peter Zeitzoff summarized the overall scaling trends and issues for logic MOSFETs from the perspective of the 2005 International Technology Roadmap for Semiconductors (ITRS). Critical challenges with scaling include unacceptable increases in gate leakage current, increasing impact of polysilicon gate depletion, difficulty in obtaining adequate control of short channel effects, as well as others. Key technological innovations (referred to as "potential solutions" in the ITRS) to address these challenges include high-k gate dielectric, metal gate electrode, strained silicon channel to enhance the carrier mobility, and eventually, non-classical CMOS devices such as fully depleted, ultra-thin body, multiple-gate MOSFETs (e.g., FinFETs). Dr. Suresh Venkatesan covered the advanced device requirements and challenges for future CMOS nodes. With the non-scaling of gate oxides over the past few technology nodes, innovations in mobility scaling have been paramount to maintain performance requirements (different market segments having different power/performance operating points). Dr. Mark Law asserted that as Moore's Law drives device scaling, TCAD becomes both important and difficult. TCAD often becomes the only way to debug a problem or investigate an issue. His talk discussed modeling frameworks for making progress and covered recent experimental work that sheds light on the directions that need to be pursued for model development for future technologies. Dr. Zlatko Sitar indicated that unique properties of III-Nitrides (AlN, GaN, InN) make them superior for high power and high frequency applications. High current values in III-Nitride FETs can be combined with very high breakdown voltages, resulting in high power outputs. These devices have potential to replace traditional GaAs based microwave power FETs used in wireless communications. In

his talk, a completely new approach was offered by the ability to grow controllably polar domains of different orientations side-by-side. These structures make use of the crystal polarity as a new degree of freedom for novel device structures that will be insensitive to surface charge. Dr. Ken Wise suggested that wireless integrated microsystems promise to become pervasive during the coming decade in applications ranging from health care and environmental monitoring to homeland security. Merging low-power embedded computing, wireless interfaces, and wafer-level packaging with microelectromechanical systems (MEMS), the resulting button-sized modules will serve as smart information-gathering nodes that will effectively wire the planet, extending communication networks to a wide range of new information-gathering applications. This talk highlighted two emerging microsystems – an implantable neural microsystem and a wristwatch-size environmental monitor.

The afternoon session focused on packaging technology, decoupling technology, electromagnetics and circuit simulations, thermal management, lead free, 3D integration, and panel discussion. Mr. Raj Master's talk included an overview of flip chip technology and challenges, package technology and manufacturability / design challenges, assembly technology and challenges, thermal issues and solutions, and overview / challenges of low K. Dr. Richard Ulrich explained that decoupling is the practice of bridging the power and ground planes of interconnect substrates with capacitors, which are distributed in location and value between the power supply and the IC. These caps provide the power to run the chip; the power supply just recharges the caps between clock cycles. The presentation reviewed the decoupling problem in general, the limits of using discrete capacitors, and the family of proposed future approaches that utilize embedded capacitance, including ferroelectric and paraelectric dielectrics, their possible inclusion into PWB's, their electrical performance and manufacturing issues. Dr. Zolton Cendes stated that engineers designing servers, storage devices, multimedia PCs, entertainment systems, and telecom systems that have driven an industry trend to replace legacy shared parallel buses with high-speed point-to-point serial buses. His talk presented a new reference design flow for high-speed serial interconnect simulation. The new flow included electromagnetic models for interconnects combined with advanced circuit simulation technology to model modern multi-gigabit transmission. Recent work on PCI Express backplane design, the Xilinx 10 Gb/s Backplane Design Kit, ultra-wideband radio design, and RFIC full chip extraction with on-chip spiral inductors was presented as application examples. Dr. Avram Bar-Cohen suggested that as Moore's Law progresses into the domain of nano-scale electronic, RF, and photonic features, steep increases in die heat flux and power dissipation results with the emergence of on-chip hot spots as the primary driver for advanced thermal packaging techniques. Following a brief review of the iNEMI thermal management roadmap for IC technology and the primary thermally-driven failure mechanisms, he talked about the thermal packaging "frontier" and the research required to address these emerging challenges. Mr. Tim Olson mentioned that with the July 1, 2006 European RoHS (Reduction of Hazardous Substances) directive deadline approaching, the electronic production supply chain is facing an unprecedented challenge in conversion to Pb free interconnect materials. His talk addressed the technical merits and existing concerns with respect to the implementation of the various RoHS compliant solutions. Dr. Rajen Chanchani provided an overview of 3D integration technologies including the motivation, description of the key technologies, and status of the technologies. The main motivating factors are 3D integration that enables miniaturization of Microsystems, a wider variety of technologies can be integrated with 3D integration, and electrical performance of 3D technology will be better. Various 3D technologies were described including issues associated with each category of technologies.

The day ended with an hour long panel discussion consisting of nine speakers and moderated by Dr. Stephen M. Goodnick. The topic was "Future of Computing and Communications". About 40 people were in audience for the panel discussion.

The Premier Sponsors included Freescale Semiconductor, IEEE Phoenix Section, and Intel Corporation. The Standard Sponsors included Arizona State University Department of Electrical Engineering and Connection One Center, the local chapters of APS, CPMT, MTT, Motorola, and RF Micro Devices. Many workshop attendees, including both IEEE and non-IEEE members, stopped by the IEEE display and were impressed by the information about local chapters, literature, and membership forms. This sparked quite a bit interest among non IEEE members for joining IEEE. Total of 18 vendors displayed at the workshop. Vendors included 3M Electronics, Advanced Packaging & Systems Technology Laboratories, Ameriprise Financial Services, Ansoft Corporation, Cadence Design Systems, CMC Interconnect Technologies, Fluent, GE Silicones, Jacket Micro Devices, Namics Technologies, Optimal Corporation, Phoenix Analysis & Design Technologies, Rogers Corporation, SONNET Software, Tango Systems, Techsearch International, Tektronix, and Zeland Software.

By bringing renowned speakers to address the most relevant topics, the workshop once again provided an excellent learning opportunity for professionals in valley. In addition to raising funds for IEEE's Phoenix Section, CPMT chapter and WAD chapter, one of the goals of the workshop is to help increase the IEEE Phoenix Section Scholarship Endowment at the Arizona State University Foundation. Continuing with the tradition from the previous three years, 50% of the surplus was donated to the Endowment. This year US$11,000 was donated, bringing the total contributions from the last four workshops to about $28,000. This endowment is helping IEEE Phoenix Section give awards to undergraduate IEEE student members. The students from Arizona State University, Devry Institute, Embry-Riddle Aeronautical University, and Northern Arizona State University are eligible to apply for these scholarships. Additional information about the workshop including organizing committee and logistics can be obtained at www.ieee.org/phoenix.

Picture of organizing committee members and volunteers in front of IEEE Phoenix Section display at the workshop

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EDAPS 2005: A workshop on Electrical Design of Advanced Packaging and Systems

Submitted by K. Raghunathan, Chair, IEEE CPMT Bangalore Chapter

The EDAPS 2005 conference was held at Bangalore India on Dec 12th & 13th coinciding with the first anniversary of the launching of the local CPMT chapter. The conference sponsored by CPMT technical committee and mentored by Prof. Madhavan Swaminathan of PRC, Georgia Tech. The response to the conference was very positive with nearly 100 attendees and 14 invited speakers from Japan, Korea, China, India, Canada and USA. The participants were from 3 diverse groups: Practicing engineers from semiconductor industry, government/ public sector companies and academia. The feedback has been very positive with request for more in-depth presentations and also addressing practical issues encountered. The previous chairs from EDAPS (2002 - 2004: Dr. Mahadevan Iyer, Singapore; Prof. Joungho Kim, Korea; Dr. Toshio Sudo, Japan) graced the occasion to make it successful through their presentations and participation.

Day 1 tutorials covered issues in Power Delivery and Signal Integrity for high speed Design; it was followed by RF and microwave packaging. Earlier in the key note Bill McCaffrey of Cadence highlighted the acceptance of SiP as a solution; he went on to elaborate and indicated uniform extraction capability for accurate modeling and mixed technology simulation are being addressed at the tool level.

Day 2 started with a keynote from Rao Tummala from Georgia Tech PRC; he outlined in his talk that embedding extra elements in substrate (especially lossless) could lead to minimizing the size; the future holds promise for bio and nano devices; the Mantra is SoP. P. R. Patel of Intel eloquently explained the multi-disciplinary nature and the intrigues of the interdependencies. Limitations in packaging performance due to thermal, reliability and material issues compared to electrical issues was highlighted. The invited papers were grouped into Power Delivery, High speed signal integrity, RF & Microwave packaging and System design challenges. The topics varied from small form factor for DDR2 interface to tuning the impedance for ultra high speed designs with high power dissipation.

A glimpse of the audience at the workshop

The next EDAPS 2006 is planned to be held at Shanghai, China under the chairman ship of Wen-Yan Yin. EDAPS 2005 Program committee chairman Suresh Subramanyam (Intel) with the volunteers has done an outstanding job of hosting the conference in Bangalore. The Chief Guest at the inauguration of the conference K. Ramachandra Kini, Director, SAMEER (Society for Applied Microwave Electronic Engineering & Research) emphasized the need for developing indigenous packaging capability soon. IEEE Fellow and IEEE Bangalore section President Surendra Pal highlighted the benefit of micro-miniaturization in the launch of satellites especially the pico satellites. Overall this has been a very useful workshop to the participants and appreciates the support from all over the globe.

A photograph of speakers who presented at the workshop

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14th Topical Meeting on the Electrical Performance of Electronic Packaging

Robert W. Jackson,
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The 14th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP) was held October 24-26, 2005 at the Radisson Hotel, in Austin Texas. EPEP provides a forum for the presentation and discussion of the latest advances in the electrical design, analysis and characterization of on chip and off chip package interconnections and structures. One of the key objectives of this meeting is to bring together researchers and practicing engineers from industry, universities, and government laboratories from around the world to address all current and future issues affecting the electrical performance of high speed electronic systems. The meeting is jointly sponsored

by the IEEE Microwave Theory and Techniques Society, and the IEEE Components, Packaging and Manufacturing Society.

The conference was organized into eleven sessions of oral presentations and one open forum (poster) session spread over the three days. The meeting began with a keynote speech entitled "The Role of System Integration and Packaging in Future Computing Systems," by Mark Papermaster, VP, Microprocessor Technology Development, IBM Corporation. This was followed by sessions dedicated to System Design and Technology, Power Distribution and Noise, Electromagnetic Issues, Transmission Lines, Measurements, On-Chip Issues and Interconnection Macro-modeling. The open forum was held in the afternoon of the second day (Tuesday) and the open bar with hor d'oeurvres encouraged relaxed technical discussions. A technical highlight of the conference was a special session entitled, "Accurate Full Wave Interconnect EM Modeling from DC to 100 GHz" organized by Professors A. Cangellaris and W. C. Chew of University of Illinois. Three short courses were offered on the Sunday prior to the start of the meeting. These tutorials were given by well-known experts in their fields and covered important topics in the design of high-speed interconnect, power distribution networks and I/O circuits.

A total of 20 student authors competed in the prestigious Best Student Paper contest. The two award winners were announced on the last day of the meeting. The best student paper award sponsored by IBM Corporation was presented to Satoshi Aoyama, Shizuoka University for her paper entitled, "A High-sensitivity Active Magnetic Probe Using CMOS Integrated Circuit Technology". The best student paper award sponsored by Intel Corporation was given to Lei Luo, North Carolina State University for his paper entitled "Signal Integrity Robustness of ACCI Packaged Systems." On behalf of the entire Technical Program Committee, the chairs of the 14th EPEP want to extend their thanks to Intel Corporation and IBM Corporation for sponsoring these awards. They really add a lot to the conference.

Keynote speaker Mark Papermaster, Vice President, Microprocessor Technology Development, IBM Corporation

The 15th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP) will be held at the Radisson Fort McDowell Resort in beautiful Scottsdale, Arizona on October 23 – 25, 2006. Moises Cases of IBM and Paul Franzon of North Carolina State University will be co-chairs. Mark your calendars and keep an eye on **www.epep.org** for the latest developments.

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7th Electronics Packaging Technology Conference (EPTC 2005)

7th – 9th December 2005

Grand Copthorne Waterfront, Singapore

Report by Singapore REL/CPMT/ED Chapter

The 7th Electronics Packaging Technology Conference (EPTC 2005) was successfully organized on 7th -9th December at the Grand Copthorne Waterfront Singapore. The conference was well attended over the 3 days. A total of 87 delegates participated in the short courses on 7th December 2005. This is by far the best turn-out for any EPTC-organized short course.
The conference on 8th-9th December was attended by a total of 265 delegates from over some 19 countries. EPTC 2005 was organized by IEEE Reliability/CPMT/ED Singapore Chapter, sponsored by IEEE CPMT Society with technical sponsorship from IMAPS. EPTC 2005 also enjoyed corporate conference sponsorship from Advanced Micro Devices Singapore, Agency for Science, Technology and Research Singapore (A-Star), Micron Semiconductor Asia and United Test & Assembly Center (UTAC).

The conference was inaugurated by Dr William Chen, IEEE CPMT Region 10 Strategic Director and CPMT President Elect, who endorsed EPTC as "a premier Asian Conference with global participation" and encouraged delegates to maximize their time at the conference through interaction, learning and sharing. He also sealed the commitment from CPMT to the EPTC series for many years to come.

In the plenary session, Dr Robert Darveaux from Amkor Technology discussed the "Current Trends and Critical Issues in Flip Chip Packaging" and Dr Chiang Shiuh-Kao from Prismark, to gave an insight on "The Global Packaging Business and Technology". An invited talk "CPMT and EPTC: A study in Symbiosis" was delivered by the CPMT representatives Dr William Chen, Prof Klaus-Jürgen Wolter and Dr Ricky Lee during the conference day 1 luncheon.

The EPTC series ran into its seventh year and has enjoyed a steady growth in terms of attendance and technical paper submissions. It has also attracted all aspects associated with the packaging of high performance electronics. EPTC 2005 featured 159 presentations in 34 sessions from experts coming from some 21 countries and dealt with advancements in core technologies such as interconnect technologies, electrical and thermal design, materials and processes, mechanical modeling and characterization, assembly and reliability assessment methodologies; as well as state-of-the-art packaging platforms in System-in-Package & MEMs packaging.

Three pre-conference short courses were offered to provide learning avenues from leading experts in specific technical fields. Dr George Harman conducted a wire bond interconnection course covering all aspects of wire bond technology as well as its application for copper low-k. The second course was a comprehensive lead-free reliability class that dealt with material, reliability & modeling aspects to lead-free implementation and development. Its course instructors included, Dr John HL Pang, Dr Rainer Dudek, Dr Tee Tong Yan, Dr Lim Chwee Teck and Dr Jason Wu. Lastly, the wafer level packaging course instructed by Dr V. Kripesh and Dr Luu T. Nguyen, dealt with process, technology, materials and applications for

WL-CSPs. In conjunction, the conference also featured a table-top exhibition where about 12 exhibitors showcased their technical products and services.

The EPTC conference banquet had become a trademark of EPTC and so in continuing this tradition, a river taxi cruise from the hotel to the Marina Bay area was organized. Delegates traveled along the Singapore River in bumboats and were treated to the sights and sounds of the Singapore's financial and entertainment district. They also caught a close-up of the Merlion statue and the grandeur of the Esplanade by the Bay. The banquet dinner held at the Colors-by-the-Bay treated the delegates to local delicacies such as chilli crabs, satay, kueh tutu, etc.

Contribute an abstract for EPTC'06; visit our website:
www.eptc-ieee.net