Call for Titles & Abstracts

Deadlines:
Titles: **May 19, 2006**
Abstracts: **June 23, 2006**
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Second International Workshop on SOP • SIP • SOC (3S) Electronics Technologies

September 21 & 22, 2006
Global Learning & Conference Center at Technology Square (Georgia Institute of Technology)
84 Fifth Street, Atlanta, GA, 30308 USA

Sponsors: Georgia Tech's Packaging Research Center, IEEE-CPMT Society
General Chair: Rao R. Tummala, Director, Packaging Research Center, Georgia Institute of Technology
Technical Chair: Dr. Mahadevan Iyer, Director of Research, PRC, Georgia Tech
Program Coordinator: Boyd Wiedenman, PRC, Georgia Tech

Fees, Program Updates and Online Registration: www.prc.gatech.edu/3s

The first 3S workshop, held at Georgia Tech in September 2005, was highly successful with industry keynote talks from TI, IBM, Intel, Philips and Skyworks. More than 80 people attended the workshop from Japan, Korea, Europe and the U.S.

The focus of the second workshop will add missing elements such as automotive and manufacturing as well as the tradeoffs between “on-chip” SOC, “on-module” SIP and “on system” SOP. Since package integration is taking place by means of either on-wafer or on-ceramic LTCC or organic laminate technologies. The tradeoffs between these are also of interest.

The SOP paradigm is beginning to take place around the globe particularly in Japan as it changes the current chip-centric SOC methodology to a cheaper, faster-to-market IC-package-system co-design flow. The advantages of the SOP paradigm over SOC appear overwhelming due to SOP’s design simplicity, lower cost and higher system function integration, electrical performance, without the intellectual property issues that dominate SOC. The SOP is also different from, yet complimentary to, 3D packaging and SIP. 3D packaging is typically the stacking of similar, or dissimilar, chips such as DRAMS. The SIP goes beyond to embed both actives and passives but the passives are discrete, thick and bulky components. The SOP goes one step further in the ultimate 3D integration of components in thin film form at microscale, in the short term, and nanoscale in the long term. The SOP focuses on integrating both single function as well as heterogeneous system functions, optimizing ICs for transistors and package for integration of digital, RF, optical, sensor and others. It accomplishes this by build-up SOP, similar to ICs and stacked SOP, and is similar to parallel board fabrication.

To summarize, this workshop will review the latest design, R & D and manufacturing status as well as applications of each of the three electronic packaging technologies currently being used around the world. It will also attempt to compare and contrast SOC, 3D stacking, SIP, SOP and MCM.

Topics

Mixed Signal Design and design tools
Embedded Digital integration and modules
Embedded Optical integration and modules
Embedded RF integration and modules
Multifunction integration and modules
Materials, processes, fabrication and assembly
Embedded LTC, organic laminate and Si wafer technologies
Mixed Signal Test
Mixed Signal Reliability
Stacked ICs and packages
Manufacturing
Applications and Products in automotive, computing, consumer and wireless