

meeting the minimum required number of valid signatures. Submit your petition by no later than Friday, 21 July 2006

to:

CPMT Society Nominations Committee
c/o Marsha Tickman
IEEE CPMT Society Executive Office
445 Hoes Lane, PO Box 1331
Piscataway, NJ 08855-1331 USA
or FAX to 732-981-1769.

If you have questions or need additional information, contact Marsha Tickman at the above address, by phone at 732-562-5529, or by e-mail at m.tickman@ieee.org.

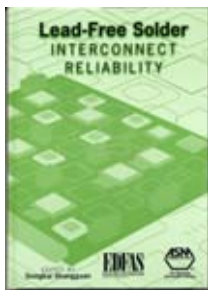
Book Reviews

The Summer the World went Lead-Free

We are reviewing two comprehensive books that are references to the large scale conversion of our industry from its 63% Sn 37% Pb roots to more legislative acceptable alternative solders. This transformation first surfaced in the late 70s in Europe and studies have slowly convinced engineers company-by-company that change is possible without dropping the high performance of their products. There are only a few blessed materials in electronics: crystal silicon, copper wire, and eutectic Sn/Pb. There is one less now.

I suspect that only old engineers remember the magic at their father's or teacher's workbench in discovering a hot iron with the smell of rosin could take a stick of metal and induce smooth silver flow onto copper wire. Frank Howland of AT&T was fond of lamenting that at first we only asked solder to protect our twisted wire from the ravages of gas diffusion caused corrosion but now we ask it to often solely perform mechanical, thermal, and electrical functions. "Never has so much been asked of so little." Although these books can not provide the same eye-opening solder magic to a new generation of "electronikers", they do reassure the experienced engineer that there is lots of support in their continual struggle to produce high quality assemblies. We applaud all the writers for their major effort in supporting this transformation.

This switch in baseline solder is massive for each individual company as well as for our industry. The characteristics of which solder is used effect the components, the mother boards, the flame retardants acceptable in encapsulates, and every detail of the manufacturing processes. These books provide the common wisdom but also alert the engineer of the danger signs to look for even when keeping on the safe path.

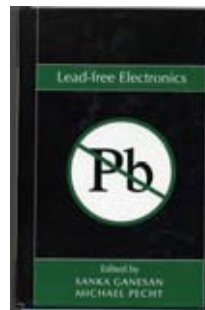


Lead-Free Solder: Interconnect Reliability -- Dongkai Shangguan, editor. ASM International 292 pages, \$195 (US).

As editor, Dongkai Shangguan provides an introductory perspective and a summary of points for continued concentration. This book is excellent for a researcher trying to decide who/what

has been done in the area and what still needs to be attacked. This book does not directly address aiding a production engineer to switch over a process line. However, the owner of a line in trouble would find plenty of aid in root cause determination in this book. This book is also excellent for a weekend study by a manager not on the production floor but faced with helping decide the transformation of production.

Highlights include the clear pictures and graphs on fatigue and creep by P. Vianco. The clear comparisons between lead and lead-free in joint reliability by J. Clech which discusses the practical considerations of assemblies with both solders. A good discussion on flux residue and its often 5 dB effect on pagers and cellular phone assemblies is included in a chapter by L. Turbini. A good tutorial on accelerated testing (and shortcomings) is cast by G. Grossmann toward Pb-free assemblies. R. Ghaffarian gives great aid to the beleaguered failure analysis engineers pitted against the new solders.



Lead-Free Electronics -- Sanka Ganesan and Michael Pecht, editors. Wiley-IEEE, 766 pages, \$100 (US), 2006 edition.

This book is excellent for the manufacturing practitioner and their MBA support. At first the size of the book evokes fear of a CALCE shovel job but, in fact, the pages are needed for the extensive review of the many alloy options and the many reliability studies. There is a slight legacy of the original edition in that all possibilities are still discussed with only moderate emphasis on the alloy path currently being taken by most of industry. This may prove the best long range approach to presenting the material since only one major long term failure mode will have many in industry and academia scurrying to back-up alloys.

Highlights include the extensive alloy review by Y. Fukuda and S. Ganesan; the in-depth treatment of surface mount process options for both reflow and wave soldering by S. Rao, J. Bath, and H. Ladhar; a complete review of reliability research by S. Ganesan; a great tutorial on Separable contacts and connectors by J. Wu and M. Pecht (Sn-Ag-Cu is worse at aging but more resistant to fretting); the tangled IP web we have woven by P. Casey and M. Pecht; and the Guidelines for production change presented as answers to frequently asked questions by V. Evely and a gang of co-authors.

For the low price, everyone with electronics assembly responsibilities should have access to this book.

Workshop Reports

EMAP 2005

Mami Yamashita, Secretary

Dear Participants of EMAP 2005,

Thank you for joining the Conference once again. I have uploaded some of the pictures taken during the conference and the tour. Please take a look at the album and if you have any additions, please feel free to send me. I will be happy to work with them.

www.sms.titech.ac.jp/emap2005/album/album.html

The pictures of the general sessions are not in the order of the session program. I am sorry but I was just incapable of doing that! Please look for and find yourself.

Season's greetings and best wishes for a prosperous New Year!!

With best regards,

Mami Yamashita, Secretary
EMAP 2005 Secretariat

(See the Call for Papers for EMAP'06 in Hong Kong,
December 11-14, 2006, [later in this Newsletter](#))

Chapter News

Region 10 Chapter Activity Round-up

By **Dr. P.B. Parikh**, Region 10 News Coordinator

Malaysia Chapter:

Dr. Ch Chew –Chairman of CPMT Chapter, Malaysia has reported having planned a number of Technical activities for this Chapter including IEMT 2006 which scheduled at Kuala Lumpur from 8th -10th November 2006. This event will feature 4 Distinguished Lecture Programs, 3 parallel technical sessions (paper presentation), and exhibition. A number of distinguished members of IEEE and Leading experts in the IC packaging have confirmed short courses and keynotes talks as under:

- **Bernie Siegal** - Short Course on “Thermal Test Methods for Integrated Circuits”.
- **Dr. Rolf Aschenbrenner** - Short Course on “Emerging Technology In IC Packaging”.
- **Dr. Annette Teng Cheung** - Short Course on “Wafer Dicing Technology”.
- **Dr. John H. Lau** - Short Course on “Design, Material, Process and Reliability of Pb Free Packaging and Assembly”.
- **Carlo Cognetti** – Keynote talk on “Packaging and Manufacturing Evolution”.
- **Dr. Dongkai Shangguan** - Keynote talk on “Packaging and Board Assembly Technology Trend and Impact on the Supply Chain”.
- **Charles Vath** – Keynote talk on “Interconnect Technology”.
- **Kin Gan** - Keynote talk on “Assembly Technology and Challenges”.
- **Yee Eh Horng** - Keynote talk on “Test Challenges and Trends”.

The new Committee of the Chapter has launched a special membership drive inviting membership to leading industries in IC packaging including material suppliers and government bodies. The Chapter is targeting to increase the total membership by 30 % by year end.

The Chapter also aims to provide good coverage and knowledge sharing on technological developments in all areas of electronics packaging and manufacturing technology.

The chapter has announced that one of their Chapter CPMT members, **Dr. Teck Joo Goh** has been awarded the “Outstanding Young Engineer” for 2006 for his significant con-

tributions to the growth of Malaysia IEEE CPMT Chapter and semiconductor packaging community. The CPMT Chapter was also awarded as one of the most active IEEE Malaysia Chapters during 2005 IEEE Malaysia Section dinner.

The Chapter Officers and the Committee members for 2006 have been announced as under:

Chair: **Dr. CH Chew**, ON Semiconductor

Vice Chair: **Dr. Ishak Abdul Azid**, University Science Malaysia

Treasurer: **Azhar Aripin**

Committee Members: **Dr. Chee Choong Kooi**, Intel

Wee Teck Lim, ON Semiconductor

Fuaida Harun, Infineon

Shutesh Krishnan, ON Semiconductor

L.C. Tan, Freescale

Taipei Chapter:

Prof. Lih-Shan Chen- Chairman of Taipei Chapter had reported that the Chapter will co-organize with IMAPS Taiwan Chapter for the “2006 International Symposium on Advanced Packaging and Green Packaging Technology”, as 4 day event to be held from June 28th to July 1st, 2006 at the Taipei World Trade Center, Taipei, Taiwan. More than 100 papers are likely to be presented in the Technical Sessions and a combined Ferro Technical Session. Topics will cover the latest developments on advanced packaging and green packaging technology.

Invited keynote speakers are:

- a) **Dr. C. Robert Kao** - Institute of Materials Science & Engineering, National Central University, Taiwan.
- b) **Dr. Kyung W. Paik** - Korea Advanced Institute of Science and Technology, Korea.

Besides, a short course entitled “Accelerated Testing; Ways to Understand Reliability Quickly and Accurately” will be given by **Dr. Michael Pecht** (Director of the CALCE Electronic Products and Systems Center at the University of Maryland).

China Chapter:

CPMT Shanghai, China

Dr. Wen-Yan Yin of CPMT Shanghai China has reported that the Chapter has planned an International work shop on EDAPS 2006 on December 17th and 18th with an objective to enhance the technical awareness in the area of packaging and on-chip system electrical design concepts. The event will focus on issues and challenges ahead for next generation electronic products.

The following topics are proposed to be covered-

- Computer-Aided Design Issues for SoC and SiP/SoP Modeling and Design;
- EM and Thermal Modeling for SoC and SiP/SoP, Electrical Design and Modeling, with Experimental Verification;
- Field-Circuit Interactions and Simulations;
- Interconnect Modeling, Design, and Testing for System-on-Chip (SoC Mixed Technology Modules Nanotube and Nanowire);
- Interconnects Optical Approaches to Packaging;
- On-Chip High-Power and Ultra-Wideband EMC and EMI;
- Power Delivery and Low Power Consumption;